CHOICE OF CAPACITORS

Spartan IR Camera for the SOAR Telescope

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For the detector board, we use metallized polyphenylene sulfide (PPS) film capacitors (Cornell-Dubilier FCP1210C104J-G3); tantalum, X5R ceramic, and X7R ceramic capacitors have increased series resistance at 77K. For the umbilical board and controller board, the default filtering capacitor is a 4.7-µF ceramic capacitor (Panasonic ECJ-2FB1C475K). The filter for the FPGA is unconventional, in that it uses a single value rather than a spread of values.

1 Detector Board

The capacitors on the detector board must operate near 77 K.

The capacitors on the detector board filter +5 for the analog circuits (VDDA), +5 for the digital circuits (VDD), biasGate, and vReset. We consider the requirements, which are a guess.

vReset absorbs all of the charge on a column. Its load is 1024 times 40,000 electrons, which is saturation. For a 100-nF capacitor, the voltage is 0.06mV, which is equivalent to 10 electrons. Furthermore, correlated sampling removes noise on vReset.

biasGate drives a single point (not a column) internal to the detector. Therefore its load is negligible compared with that of VDDA.

VDDA is the supply for the output transistor, which drives a 10-kOhm load and a 40-pF cable. The capacitor must prevent the load in one quadrant from affecting another quadrant. Assume the power-supply rejection of the output transistor is unity. For a 100-nF capacitor, the impedance at the

pixel frequency, 100kHz, is 16Ohm. The capacitor filters by a factor of 600, which couples 40,000/600=60 electrons from a saturated quadrant.

At 1 MHz, the impedance of the 100-nF capacitor is 1.6 Ohm.

The external capacitors do also filter but through the 1.3-Ohm resistance of the 20mil×0.7mil×28in flexible cable. (The width of the traces for signals is 5 mil.)

For PPS film and NP0 capacitors, the capacitance and series resistance at 77 K is close to that at room temperature. For ceramic capacitors with either X5R or X7R temperature characteristic, the capacitance drops by a factor of 4–5 and the series resistance increases by a factor of 20 at 77 K. For a 2.2-μF tantalum capacitor (AVX TAJB225K016R), the capacitance is 0.6 μF and the series resistance is 13 Ω at 77 K.

The plan is to use 100-nF metallized polyphenylene sulfide (PPS) film capacitors (Cornell-Dubilier FCP1210C104J-G3) on the detector board and to use a 4.7-μF ceramic capacitor with X5R temperature characteristic (Panasonic ECJ-2FB1C475K) on the controller board. The expected impedance is case 3 in Figure 1. For case 2, which uses a PPS capacitor, the narrow trace has a high series resistance.

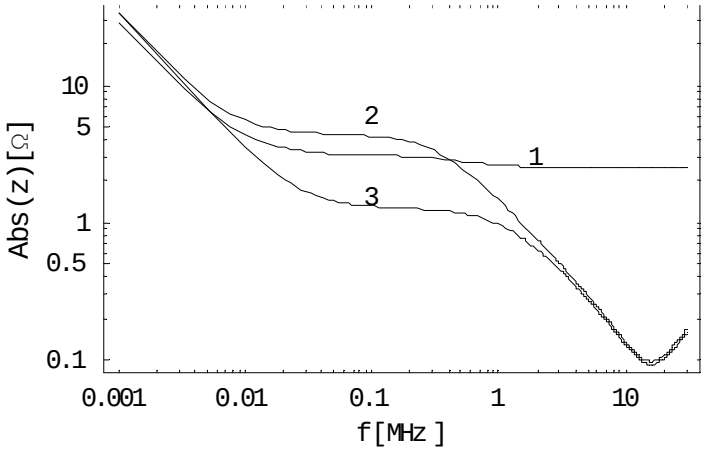

Figure 1 Impedance between VDD and ground at the detector with 2.2-μF tantalum and 100-nF XR7 capacitors on the board and a 4.7-μF XR5 capacitor on the outside (case 1), with 100-nF PPS capacitor and 4.7-μF XR5 capacitor on the outside connected by a 5-mil trace (case 2), and with 100-nF PPS capacitor and 4.7-μF XR5 capacitor on the outside connected by a 20-mil trace (case 3).

With case 1, which uses X7R ceramic and tantalum capacitors on the detector board, the noise at low spatial frequency is large. We found a large low-frequency noise with case 1. Apparently the correlated noise is a manifestation of the large series resistance at high frequency.

2 Umbilical Board

2.1 For the Field-Programmable Gate Array (FPGA)

The field-programmable-gate-array (FPGA) has two power nets, VCCInt (1.8 V) for internal circuits and VCCO (3.3 V) for driving external circuits.

For the internal circuits, the capacitors must supply charge only to switch the internal capacitors. Using the Xilinx Power Estimator, we find that the load is 43 mW on VCCInt and 70 mW on the VCCO. The internal capacitance is 1.7 nF; half of the circuits run at 100 MHz and half at 6 MHz. Each of the 12 VCCInt pads requires a 7 nF capacitor to suppress the ripple by a factor of 50. With 1-nH capacitors, the resonant angular frequency is 2.6 GHz, and the rise time is 1.2ns.

The main load on the external circuit is 18 lines to the computer, which amount to 1.8 nF. Each of the 8 VCCO pads requires a 12 nF capacitor to suppress the ripple by a factor of 50.

2.1.1 Filter for 1.8V

Xilinx[1] recommends using a range of capacitors for VCCInt to keep the impedance nearly independent of frequency.

For filtering VCCInt, we use 12 4.7-µF ceramic capacitors (Panasonic ECJ-2FB1C475K). The geometry is 0805 (2.0×1.2×1.3mm). The temperature classification is X5R, which means 15% change from -55 to 85 C.

Our filter has lower impedance than Xilinx's recommendation (Figure 2). The impedance above 100 MHz is the same, since the

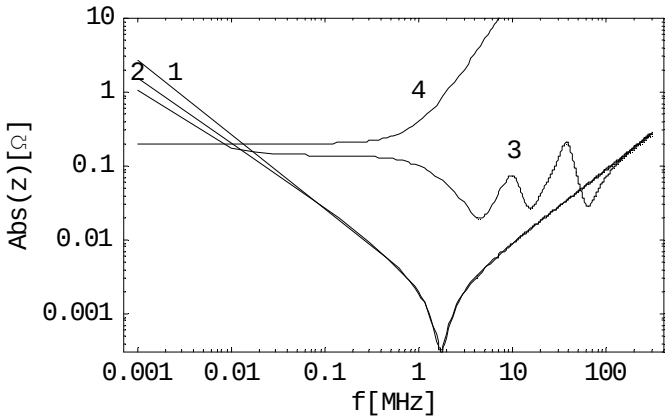

Figure 2 Impedance vs. frequency for (1) the filters actually used (12 4.7-µF X5R 0805 capacitors), (2) case 1 with an additional 47-µF tantalum capacitor, (3) filters recommended by Xilinx (6 4.7-nF X7R, 3 47-nF X7R, 2 470-nF X7R, and one 150-µF tantalum capacitors), and (4) the 1.8-V section of the TPS70151 voltage regulator. The circuit board adds 1.2 nH to each capacitor.

[1] Alexander, M., 2003, "XAPP623, Power Distribution System (PDS) Design: Using Bypass/Decoupling Capacitors," www.xilinx.com

inductance of the pads determines it. Below 10 kHz, the voltage regulator dominates, although the recommended filter has somewhat lower impedance. In between, our filter has lower impedance.

Xilinx recommends that the impedance be flat with frequency, but I can see no reason for that. Xilinx does comment on keeping antiresonance spikes low. Their recommended filter has antiresonance spikes, whereas ours does not.

There is a resonance at 1.5 MHz, but it is unlikely to cause oscillation since its Q is 0.14.

We minimize the inductance of the filters. Each pad on the FPGA has one R0.13-mm via. (There is no space for more.) There are three vias for each pad of the capacitors.

2.1.2 Filter for 3.3V

Eight 4.7-µF X5R capacitors filter the 3.3V supply.

2.2 For the Fiber-Optic Transceiver

The filter is made with a 1-µH choke and a 4.7-µF capacitor. At the 1.6-ns fall time and the 8 MHz data rate, the filter rejection is 10^6 and 10^4 respectively.

3 Controller Board

3.1 General Considerations

The fastest time possible for an analog signal is 40 ns, the rise time on the flexible cable. The pixel time is 10 µs.

The characteristic inductance of the power plane and ground planes is 0.6 nH. (The current runs through a via with a radius 0.25 mm, the power plane, a path 10 mm away, and the ground plane 0.8 mm from the power plane.

For filtering we use 4.7-µF ceramic capacitors (Panasonic ECJ-2FB1C475K). The geometry is 0805 (2.0×1.2×1.3mm). The temperature classification is X5R, which means the capacitance changes less than 15% from -55 to 85 C.

The inductance of a 0.25-mm wide, 3-mm long trace 0.8 mm above the ground plane is 2.3nH.

3.2 Analog Circuits

For the analog-to-digital converter (ADC), we use a single 4.7-µF ceramic capacitor. Analog Devices recommends a 100-nF capacitor adjacent to the device and a 10-µF capacitor nearby.

For each op-amp, we use a single 4.7-µF ceramic capacitor.

3.3 FPGA

We adopt the requirements for the umbilical board, even though the FPGA on the umbilical board uses more current.

3.4 For the Fiber-Optic Transceiver

The requirements are the same as that of the umbilical board.