DES 12 Channel Transition Board - Functional Tests: Revision 2.0

Stage 1. Preparation of documentation and configuration settings - Table 1.

Board Part Number	P43		Board Serial Number	#
Date Of Tests	Aug. 26 , 2010		Name Of Person Testing	S. Holm
Suggested Filename To Save	CCDTransition_12Ch_REPORT_BOARD#.xls			

Stage 2. Board Dimensions and Grounding Options - Table 2.

Board Length	OK		J5 connection	**(-15v)** or (-5v)
Board Width	OK		J6 connettion	**(+15v)** or (+5v)
Board Thickness	OK		J1, J3, J4, J8, J9, J11 Connection	**(Front Panel Ground)** or Agnd
Board Outline	OK		Video Channel Options	Straight through

Stage 4. Power plane short test - Table 3.

	Short test to ground	
Supply Name	Impedance to ground	Test Point
+5VA' in	84k	F11
-5VA' in	25k	F12
+15VA' in	84k	F13
-15VA' in	25k	F14
-28VA' in	73k	F16
+48VA' in	330k	F15
+5VA' out	50k	F6
-5VA' out	50k	F7
+15VA' out	32k	F9
-15VA' out	40k	F8
-28VA' out	4M	F10
+48VA' onboard	40K	F5
Neg. Preamp Power	33K	F1
Neg. Preamp Power	33k	F2
Pos. Preamp Power	38k	F3
Pos. Preamp Power	38k	F4

Stage 6. Power Consumption - Table 4.

	Power Supply Consumption	
Supply Name	Measured Voltage on PCB	Measured Current on power supply
+5VA' in	5.00	0.003
-5VA' in	-5.00	0.003
+15VA' in	15.00	0.011
-15VA' in	-15.00	0.031
-28VA' in	-28.00	0.007
+48VA' in	48.00	0.037
+5VA' out	5.00	N/A
-5VA' out	-5.00	N/A
+15VA' out	15.00	N/A
-15VA' out	-15.00	N/A
-28VA' out	-28.00	N/A
+48VA' out	48.00	N/A

Power Dissipation:
2.6 Watts

~2.5 watts +/- 5%

Stage 8. Bias Voltage testing - Table 5.

Bias Voltage Test Data

DAC Value 50%

Signal	volts	Fanout Brd
Vru 0	-5.71	BIAS 3
Vru 1	-5.71	BIAS 4
Vru 2	-5.71	BIAS 5
Vru 3	-5.71	BIAS 6
Vru 4	-5.71	BIAS 7
Vru 5	-5.71	BIAS 8
Vru 6	xxx	BIAS 9
Vru 7	xxx	BIAS 10
Vrl 0	-5.71	BIAS 11
Vrl 1	-5.71	BIAS 12
Vrl 2	-5.71	BIAS 13
Vrl 3	-5.71	BIAS 14
Vrl 4	-5.71	BIAS 15
Vrl 5	-5.71	BIAS 16
Vrl 6	xxx	BIAS 17
Vrl 7	xxx	BIAS 18
Vog 0	1.24	BIAS 19
Vog 1	1.24	BIAS 20
Vog 2	1.24	BIAS 21
Vog 3	1.24	BIAS 22
Vog 4	1.24	BIAS 23
Vog 5	1.24	BIAS 24
Vog 6	xxx	BIAS 25
Vog 7	xxx	BIAS 26
Vdd 0	-9.57	BIAS 27
Vdd 1	-9.57	BIAS 28
Vdd 2	-9.57	BIAS 29
Vdd 3	-9.57	BIAS 30
Vdd 4	-9.57	BIAS 21
Vdd 5	-9.57	BIAS 32
Vdd 6	xxx	BIAS 33
Vdd 7	xxx	BIAS 34

Notes and Observations

Checked for oscillations using a Agilent Oscilloscpe on AC. **OK**

Stage 9. Vsub and Heater Control testing - Table 6.

Vsub Testing
DAC Value 50%

Signal	volts
Vsub1	15.02
Vsub2	15.13
Vsub3	14.96
Vsub4	14.99
Vsub5	14.99
Vsub6	15.06

RTD Testing
DAC Value 50%

Signal	Readback
RTD1	221
RTD2	248
RTD3	275
RTD4	302
RTD5	327
RTD6	350
Reference 4096	836
Reference buffered	836

Notes and Observations

RTD values within range.

Stage 10. CDS Video Channel Testing - Table 7.

TEST #1: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels. The purpose of this test is to verify the correct operation of the ADC devices and measure the noise of the ADC channels while the inputs are grounded.

Noise Test 4				
	Min Pix Value	**Max Pix**	**Mean Pix**	**Std. Dev.**
CH 0				
CH 1				
CH 2				
CH 3				
CH 4				
CH 5	~76k	~76k	~76k	<3.2
CH 6				
CH 7				
CH 8				
CH 9				
CH 10				
CH 11				

TEST #2: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels. The purpose of this test is to verify the path of the video signal to the correct operational Front Panel output port.

	ok
CH 0	**ok**
CH 1	**ok**
CH 2	**ok**
CH 3	**ok**
CH 4	**ok**
CH 5	**ok**
CH 6	**ok**
CH 7	**ok**
CH 8	**ok**
CH 9	**ok**
CH 10	**ok**
CH 11	**ok**

Stage 11.Hot Swap Controller tests - Table 8.

Supply Name	HOT Swap testing			
	FB pin	On pin	Typical voltage value	
+5VA' in	R426	R430		
	1.4	3.1	1.4v	3.1v
-5VA' in	R424	R425		
	-1.4	-3.1	neg 1.4v	neg 3.1v
+15VA' in	R407	R414		
	1.4	9.4	1.4v	9.4v
-15VA' in	R401	R403		
	-1.4	-9.4	neg 1.4v	neg 9.4v
-28VA' in	R392	R393	R394	
	-27.1	-26.3	-26.5	
	R383	R385		
+48VA' in	4.70	5.30	4.7	5.3