

## DES 12 Channel Transition Board - Functional Tests: Revision 2.0

## Stage 1. Preparation of documentation and configuration settings - Table 1.

|                            |                                      |                        |         |
|----------------------------|--------------------------------------|------------------------|---------|
| Board Part Number          | P47                                  | Board Serial Number    | #       |
| Date Of Tests              | Aug. 25 , 2010                       | Name Of Person Testing | S. Holm |
| Suggested Filename To Save | CCDTransition_12Ch_REPORT_BOARD#.xls |                        |         |

## Stage 2. Board Dimensions and Grounding Options - Table 2.

|                 |    |                                    |                              |
|-----------------|----|------------------------------------|------------------------------|
| Board Length    | OK | J5 connection                      | (-15v) or (-5v)              |
| Board Width     | OK | J6 connection                      | (+15v) or (+5v)              |
| Board Thickness | OK | J1, J3, J4, J8, J9, J11 Connection | (Front Panel Ground) or Agnd |
| Board Outline   | OK | Video Channel Options              | Straight through             |

## Stage 4. Power plane short test - Table 3.

| Short test to ground |                     |            |
|----------------------|---------------------|------------|
| Supply Name          | Impedance to ground | Test Point |
| +5VA' in             | 85k                 | F11        |
| -5VA' in             | 27k                 | F12        |
| +15VA' in            | 85k                 | F13        |
| -15VA' in            | 26k                 | F14        |
| -28VA' in            | 73k                 | F16        |
| +48VA' in            | 330k                | F15        |
| +5VA' out            | 50k                 | F6         |
| -5VA' out            | 50k                 | F7         |
| +15VA' out           | 32k                 | F9         |
| -15VA' out           | 32k                 | F8         |
| -28VA' out           | 500k                | F10        |
| +48VA' onboard       | 37k                 | F5         |
| Neg. Preamp Power    | 33k                 | F1         |
| Neg. Preamp Power    | 33k                 | F2         |
| Pos. Preamp Power    | 39k                 | F3         |
| Pos. Preamp Power    | 39k                 | F4         |

## Stage 6. Power Consumption - Table 4.

| Supply Name | Power Supply Consumption |                                  |
|-------------|--------------------------|----------------------------------|
|             | Measured Voltage on PCB  | Measured Current on power supply |
| +5VA' in    | 5.00                     | 0.003                            |
| -5VA' in    | -5.00                    | 0.003                            |
| +15VA' in   | 15.00                    | 0.011                            |
| -15VA' in   | -15.00                   | 0.031                            |
| -28VA' in   | -28.00                   | 0.007                            |
| +48VA' in   | 48.00                    | 0.037                            |
| +5VA' out   | 5.00                     | N/A                              |
| -5VA' out   | -5.00                    | N/A                              |
| +15VA' out  | 15.00                    | N/A                              |
| -15VA' out  | -15.00                   | N/A                              |
| -28VA' out  | -28.00                   | N/A                              |
| +48VA' out  | 48.00                    | N/A                              |

Power Dissipation:  
2.6 Watts  
~2.5 watts +/- 5%

## Stage 8. Bias Voltage testing - Table 5.

| Bias Voltage Test Data<br>DAC Value 50% |       |            |
|---|-------|------------|
| Signal                                  | volts | Fanout Brd |
| Vru 0                                   | -5.71 | BIAS 3     |
| Vru 1                                   | -5.71 | BIAS 4     |
| Vru 2                                   | -5.71 | BIAS 5     |
| Vru 3                                   | -5.71 | BIAS 6     |
| Vru 4                                   | -5.71 | BIAS 7     |
| Vru 5                                   | -5.71 | BIAS 8     |
| Vru 6                                   | xxx   | BIAS 9     |
| Vru 7                                   | xxx   | BIAS 10    |
| Vri 0                                   | -5.71 | BIAS 11    |
| Vri 1                                   | -5.71 | BIAS 12    |
| Vri 2                                   | -5.71 | BIAS 13    |
| Vri 3                                   | -5.71 | BIAS 14    |
| Vri 4                                   | -5.71 | BIAS 15    |
| Vri 5                                   | -5.71 | BIAS 16    |
| Vri 6                                   | xxx   | BIAS 17    |
| Vri 7                                   | xxx   | BIAS 18    |
| Vog 0                                   | 1.24  | BIAS 19    |
| Vog 1                                   | 1.24  | BIAS 20    |
| Vog 2                                   | 1.24  | BIAS 21    |
| Vog 3                                   | 1.24  | BIAS 22    |
| Vog 4                                   | 1.24  | BIAS 23    |
| Vog 5                                   | 1.24  | BIAS 24    |
| Vog 6                                   | xxx   | BIAS 25    |
| Vog 7                                   | xxx   | BIAS 26    |
| Vdd 0                                   | -9.57 | BIAS 27    |
| Vdd 1                                   | -9.57 | BIAS 28    |
| Vdd 2                                   | -9.57 | BIAS 29    |
| Vdd 3                                   | -9.57 | BIAS 30    |
| Vdd 4                                   | -9.57 | BIAS 21    |
| Vdd 5                                   | -9.57 | BIAS 32    |
| Vdd 6                                   | xxx   | BIAS 33    |
| Vdd 7                                   | xxx   | BIAS 34    |

## Notes and Observations

Checked for oscillations using a Agilent Oscilloscope on AC. **OK**

## Stage 9. Vsub and Heater Control testing - Table 6.

Vsub Testing  
DAC Value 50%

| Signal | volts |
|--------|-------|
| Vsub1  | 15.01 |
| Vsub2  | 15.08 |
| Vsub3  | 15.22 |
| Vsub4  | 15.08 |
| Vsub5  | 15.12 |
| Vsub6  | 15.09 |

RTD Testing  
DAC Value 50%

| Signal             | Readback |
|--------------------|----------|
| RTD1               | 221      |
| RTD2               | 248      |
| RTD3               | 275      |
| RTD4               | 301      |
| RTD5               | 327      |
| RTD6               | 350      |
| Reference 4096     | 836      |
| Reference buffered | 836      |

## Notes and Observations

RTD values within range.

## Stage 10. CDS Video Channel Testing - Table 7.

## TEST #1: ccdBrdTest\_Setup01.mod

This setup acquires data from the ADC channels. The purpose of this test is to verify the correct operation of the ADC devices and measure the noise of the ADC channels while the inputs are grounded.

## Noise Test 4

|       | Min Pix Value | Max Pix | Mean Pix | Std. Dev. |
|-------|---------------|---------|----------|-----------|
| CH 0  |               |         |          |           |
| CH 1  |               |         |          |           |
| CH 2  |               |         |          |           |
| CH 3  |               |         |          |           |
| CH 4  |               |         |          |           |
| CH 5  | ~76k          | ~76k    | ~76k     | <3.2      |
| CH 6  |               |         |          |           |
| CH 7  |               |         |          |           |
| CH 8  |               |         |          |           |
| CH 9  |               |         |          |           |
| CH 10 |               |         |          |           |
| CH 11 |               |         |          |           |

## TEST #2: ccdBrdTest\_Setup01.mod

This setup acquires data from the ADC channels. The purpose of this test is to verify the path of the video signal to the correct operational Front Panel output port.

|       |    |
|-------|----|
|       | ok |
| CH 0  | ok |
| CH 1  | ok |
| CH 2  | ok |
| CH 3  | ok |
| CH 4  | ok |
| CH 5  | ok |
| CH 6  | ok |
| CH 7  | ok |
| CH 8  | ok |
| CH 9  | ok |
| CH 10 | ok |
| CH 11 | ok |

## Stage 11. Hot Swap Controller tests - Table 8.

## HOT Swap testing

| Supply Name | HOT Swap testing |        | Typical voltage value |          |
|-------------|------------------|--------|-----------------------|----------|
|             | FB pin           | On pin |                       |          |
| +5VA' in    | R426             | R430   |                       |          |
|             | 1.4              | 3.1    | 1.4v                  | 3.1v     |
| -5VA' in    | R424             | R425   |                       |          |
|             | -1.4             | -3.1   | neg 1.4v              | neg 3.1v |
| +15VA' in   | R407             | R414   |                       |          |
|             | 1.4              | 9.4    | 1.4v                  | 9.4v     |
| -15VA' in   | R401             | R403   |                       |          |
|             | -1.4             | -9.4   | neg 1.4v              | neg 9.4v |
| -28VA' in   | R392             | R393   | R394                  |          |
|             | -27.1            | -26.3  | -26.5                 |          |
| +48VA' in   | R383             | R385   |                       |          |
|             | 4.70             | 5.30   | 4.7                   | 5.3      |