DES 12 Channel Board - Functional Tests: CCD Acquisition Board Revision 1.0

Stage 1. Preparation of documentation and configuration settings - Table 1.

Board Part Number	14	Board Serial Number	14
Date Of Tests	May 2010	Name Of Person Testing	S. Holm
Suggested Filename To Save	CCDACQ_12Ch_REPORT_BOARD14.xl	Sequence number: Test	

Stage 3. Power plane short test - Table 2.

Supply Name	Short test to ground: Impedance to ground	Test Point	
+1.2VD	50.40	TP43	~50 ohms
+1.8VD	2M	TPB12	> 1K ohm
+2.5VD	19k	TPB11	> 1K ohm
+3.3VD	6k	D13	> 1K ohm
+5VD	19k	D14	> 1K ohm
+5VA	4M	C267	> 1K ohm
-5VA	300k	C270	> 1K ohm
+15VA	400k	C288	> 1K ohm
-15VA	400k	C282	> 1K ohm
-28VA	2.5M	C307	> 1K ohm

Stage 4. Firmware programming tests - Table 3.

JTAG Order	Designator	Device	Load File	Check Sum or User Code
1	U122	XCF08PFS48C PROM	CcdAcqFpgaV41.mcs	0014ef670
2	U114	Spartan3 XC3S2000 FPGA	ccdacqfpgav41.bit	5102801

Stage 5. Power Consumption - Table 4.

Supply Name	Power Supply Consumption: Measured Voltage at test point	Measured Current on power supply	Test Point	
+1.2VD	1.20	N/A	TP43	
+1.8VD	1.80	N/A	TPB12	
+2.5VD	2.50	N/A	TPB11	
+3.3VD	3.30	0.119	D13	
+5VD	5.20	0.15	D14	
+5VA	4.95	0.581	C267	
-5VA	-4.95	0.433	C270	
+15VA	14.92	0.649	C288	
-15VA	-15.05	0.494	C282	
-28VA	-27.88	0.218	C307	
Vref 0+	10.05	N/A	R534	Vsub+ Reference(+10v)
Vref 0-	-2.50	N/A	R525	Vsub - Reference(-2.5v)
Vref Offset	2.50	N/A	R573	ADC Offset Reference(+2.5v)
Vclamp	1.87	N/A	VIA	ADC Clamp Voltage(+1.8v)
ADC Ref.	2.50	N/A	VIA	ADC Reference Voltage(+2.5v)
Vref 1+	2.50	N/A	R537	Vru and Vrl + Reference(+2.5v)
Vref 1-	-10.13	N/A	R535	Vru and Vrl - Reference(-10v)
Vref 2+	5.00	N/A	R563	Vog + Reference(+5v)
Vref 2-	-2.52	N/A	R555	Vog - Reference(-2.5v)
Vref 3+	2.50	N/A	R543	Vdd + Reference(+2.5v)
Vref 3-	-10.15	N/A	R571	Vdd - Reference(-10v)

Power Dissipation:
29.4 Watts

~27 watts +/- 5%

Stage 7. Basic Bus Transactions - **D**igital **Register** Tests - Table 5.

Register name	Put an X on any bit that has an error: 31-24	23-16	15-08	07-00	Function	Test name: Pattern	Walking 0's	Walking 1's
CDS Control			00000000	00000000	16 bit R/W			
Digital Output	00000000	00000000	00000000	00000000	32 bit R/W			
ADC Config.			0000	00000000	12 bit R/W			
Offset DAC			0000	00000000	12 bit R/W			
Bias DAC			0000	00000000	12 bit R/W			
Telemetry Config.				0000	4 bit R/W			
Auxilary Config.				00 00000000	10 bit R/W			
Redirect				0000	4 bit R/W			
Pixel Transfer				00000000	8 bit R/W			
Micro SEQ			00000000	00000000	16 bit R/W			
RAM Buffer			00000000	00000000	16 bit R/W			
LED Control				0000	4 bit R/W			
Control			00000000	00000000	16 bit R/W			
All Register Test	00000000	00000000	00000000	00000000	16 bit R/W	**Passed**	**Passed**	**Passed**

Stage 8. Bias Voltage settings and output enables testing - Table 8

DAC Value	410	Bias Voltage Test Data 2048	3686	50% rms Noise	10-90% Rise Time			
Signal	volts	volts	volts	uV	millisec.	Fanout Brd	Slope	Offset
Vru 0	-13.31	-5.73	1.85	<10	2	BIAS 3	216.09	3286.22
Vru 1	-13.31	-5.73	1.85	<10	2	BIAS 4	216.09	3286.22
Vru 2	-13.31	-5.73	1.85	<10	2	BIAS 5	216.09	3286.22
Vru 3	-13.31	-5.73	1.85	<10	2	BIAS 6	216.09	3286.22
Vru 4	-13.31	-5.73	1.85	<10	2	BIAS 7	216.09	3286.22
Vru 5	-13.31	-5.73	1.85	<10	2	BIAS 8	216.09	3286.22
Vru 6	-13.31	-5.73	1.85	NA	NA	BIAS 9	216.09	3286.22
Vru 7	-13.31	-5.73	1.85	NA	NA	BIAS 10	216.09	3286.22
Vrl 0	-13.31	-5.73	1.85	<10	2	BIAS 11	216.09	3286.22
Vrl 1	-13.31	-5.73	1.85	<10	2	BIAS 12	216.09	3286.22
Vrl 2	-13.31	-5.73	1.85	<10	2	BIAS 13	216.09	3286.22
Vrl 3	-13.31	-5.73	1.85	<10	2	BIAS 14	216.09	3286.22
Vrl 4	-13.31	-5.73	1.85	<10	2	BIAS 15	216.09	3286.22
Vrl 5	-13.31	-5.73	1.85	<10	2	BIAS 16	216.09	3286.22
Vrl 6	-13.31	-5.73	1.86	NA	NA	BIAS 17	215.95	3284.69
Vrl 7	-13.31	-5.73	1.86	NA	NA	BIAS 18	215.95	3284.69
Vog 0	-1.77	1.24	4.24	<10	2	BIAS 19	545.09	1373.90
Vog 1	-1.77	1.24	4.24	<10	2	BIAS 20	545.09	1373.90
Vog 2	-1.77	1.24	4.24	<10	2	BIAS 21	545.09	1373.90
Vog 3	-1.77	1.24	4.24	<10	2	BIAS 22	545.09	1373.90
Vog 4	-1.77	1.24	4.24	<10	2	BIAS 23	545.09	1373.90
Vog 5	-1.77	1.24	4.24	<10	2	BIAS 24	545.09	1373.90
Vog 6	-1.77	1.24	4.24	NA	NA	BIAS 25	545.09	1373.90
Vog 7	-1.77	1.24	4.24	NA	NA	BIAS 26	545.09	1373.90
Vdd 0	-22.22	-9.57	3.06	<10	20	BIAS 27	129.59	3289.03
Vdd 1	-22.29	-9.60	3.08	<10	20	BIAS 28	129.13	3288.07
Vdd 2	-22.25	-9.59	3.08	<10	20	BIAS 29	129.33	3287.87
Vdd 3	-22.22	-9.57	3.08	<10	20	BIAS 30	129.49	3287.18
Vdd 4	-22.09	-9.51	3.07	<10	20	BIAS 21	130.21	3286.27
Vdd 5	-22.20	-9.56	3.08	<10	20	BIAS 32	129.59	3286.87
Vdd 6	-22.18	-9.55	3.08	NA	NA	BIAS 33	129.69	3286.55
Vdd 7	-22.23	-9.58	3.08	NA	NA	BIAS 34	129.43	3287.56

Vru	Slope		Offset
Mean	216.09	Mean	3286.22
Stdev	0	Stdev	4.54747E-13
Average	216.09499	Average	3286.224274
	Dac #	Average voltage	
	0	-15.0	
	4095	3.7	

Vrl	Slope		Offset
Mean	216.06	Mean	3285.84
Stdev	0.0616957	Stdev	0.665217123
Average	216.05937	Average	3285.840211
	Dac #	Average voltage	
	0	-15.2	
	4095	3.7	

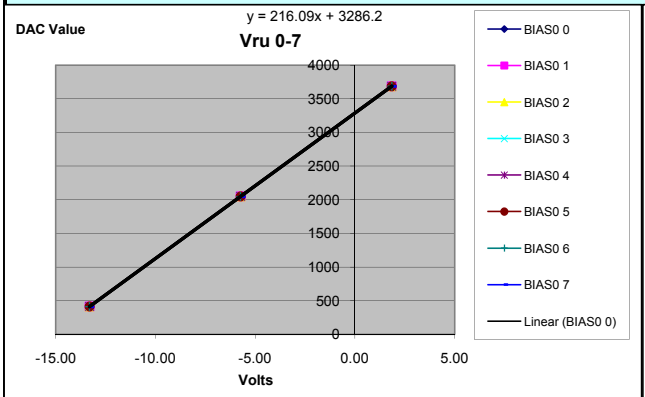
Vog	Slope		Offset
Mean	545.09	Mean	1373.90
Stdev	0	Stdev	0
Average	545.09101	Average	1373.904116
	Dac #	Average voltage	
	0	-2.5	
	4095	5.0	

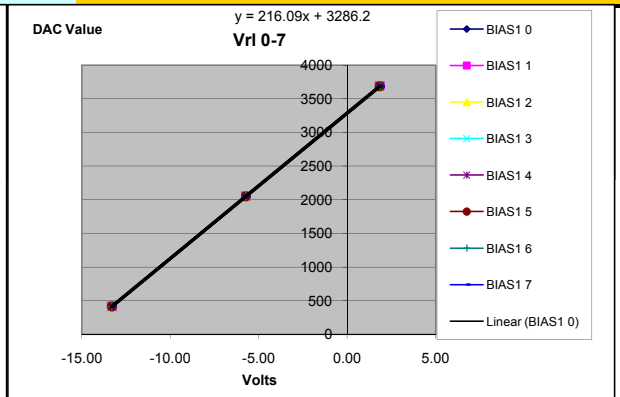
Vdd	Slope		Offset
Mean	129.56	Mean	3287.42
Stdev	0.2948598	Stdev	0.842027846
Average	129.55724	Average	3287.423366
	Dac #	Average voltage	
	0	-25.4	
	4095	6.2	

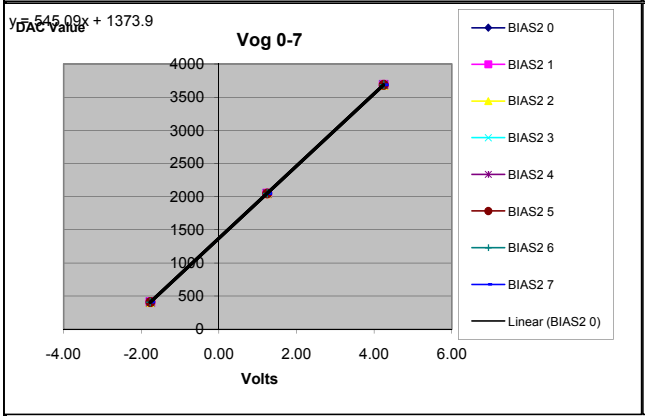
Notes and Observations

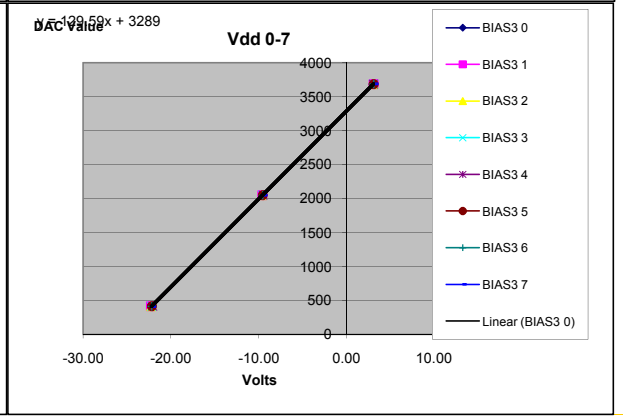
Checked for oscillations using a Agilent Oscilloscpe on AC.OK

average min & max voltages
(dac# -offset)/slope=voltage









Stage 8B. Telemetry System Tests - Table 7 (Bias Telemetry Tests)

DAC Value: 410 / 3686

Signal	Telemetry Return Values 10%	90%	Bias Signals Set Volts 10%	90%	Resolved Values for Telemetry Channel Slope	Offset
Vru 0	-1763	420	-13.31	1.85	143.9974	153.60
Vru 1	-1764	420	-13.31	1.85	144.0633	153.48
Vru 2	-1763	421	-13.31	1.85	144.0633	154.48
Vru 3	-1758	420	-13.31	1.85	143.6675	154.22
Vru 4	-1764	420	-13.31	1.85	144.0633	153.48
Vru 5	-1761	420	-13.31	1.85	143.8654	153.85
Vru 6	-1766	420	-13.31	1.85	144.1953	153.24
Vru 7	-1763	420	-13.31	1.85	143.9974	153.60
Vrl 0	-1763	421	-13.31	1.85	144.0633	154.48
Vrl 1	-1764	421	-13.31	1.85	144.1293	154.36
Vrl 2	-1766	421	-13.31	1.85	144.2612	154.12
Vrl 3	-1761	421	-13.31	1.85	143.9314	154.73
Vrl 4	-1765	421	-13.31	1.85	144.1953	154.24
Vrl 5	-1764	421	-13.31	1.85	144.1293	154.36
Vrl 6	-1767	421	-13.31	1.86	144.2320	152.73
Vrl 7	-1762	421	-13.31	1.86	143.9024	153.34
Vog 0	-366	866	-1.77	4.24	204.9917	-3.16
Vog 1	-366	866	-1.77	4.24	204.9917	-3.16
Vog 2	-366	866	-1.77	4.24	204.9917	-3.16
Vog 3	-366	866	-1.77	4.24	204.9917	-3.16
Vog 4	-365	866	-1.77	4.24	204.8253	-2.46
Vog 5	-366	866	-1.77	4.24	204.9917	-3.16
Vog 6	-366	866	-1.77	4.24	204.9917	-3.16
Vog 7	-366	866	-1.77	4.24	204.9917	-3.16
Vdd 0	-1729	570	-22.22	3.06	90.9415	291.72
Vdd 1	-1739	572	-22.29	3.08	91.0918	291.44
Vdd 2	-1739	571	-22.25	3.08	91.1962	290.12
Vdd 3	-1730	570	-22.22	3.08	90.9091	290.00
Vdd 4	-1730	569	-22.09	3.07	91.3752	288.48
Vdd 5	-1735	571	-22.20	3.08	91.2184	290.05
Vdd 6	-1735	570	-22.18	3.08	91.2510	288.95
Vdd 7	-1736	571	-22.23	3.08	91.1497	290.26

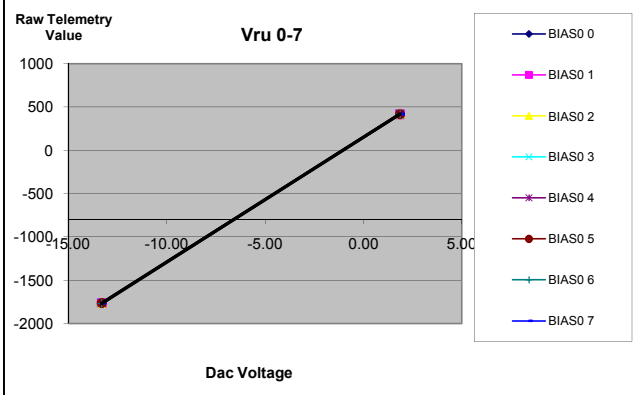
AVERAGE

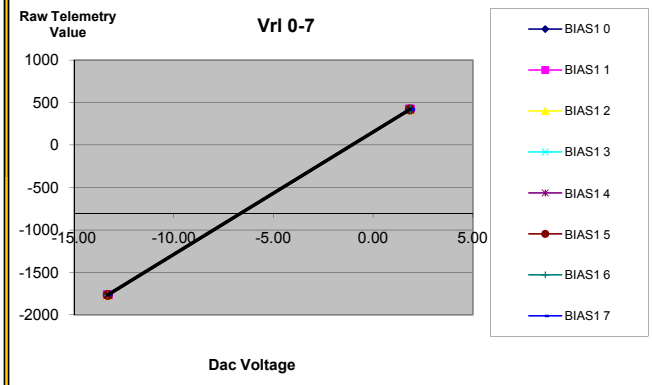
Vru	Slope		Offset
Mean	143.99	Mean	153.75
Stdev	0.1491024	Stdev	0.3887686

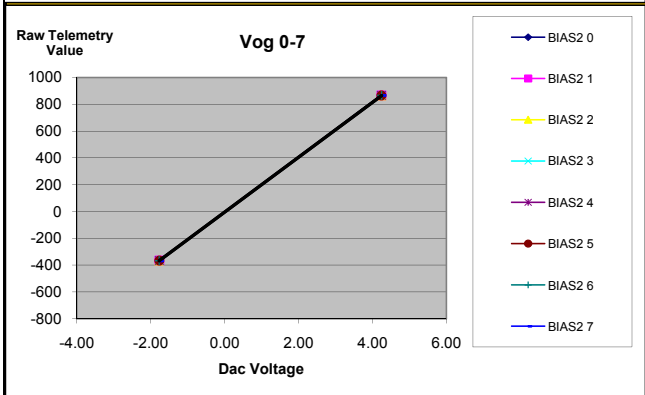
Vrl	Slope		Offset
Mean	144.11	Mean	154.04
Stdev	0.1238795	Stdev	0.6252269

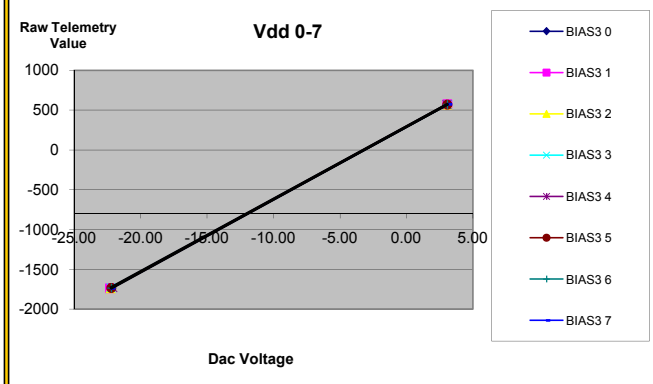
Vog	Slope		Offset
Mean	204.97	Mean	-3.08
Stdev	0.0550281	Stdev	0.2333192

Vdd	Slope		Offset
Mean	91.14	Mean	290.13
Stdev	0.146658	Stdev	1.0248509









Stage 8C. Bias Voltage output enables testing - Table 8

Place a line through Bias Voltage name if enable/disable switch works

Vru 0	Vru 1	Vru 2	Vru 3	Vru 4	Vru 5
Vrl 0	Vrl 1	Vrl 2	Vrl 3	Vrl 4	Vrl 5
Vog 0	Vog 1	Vog 2	Vog 3	Vog 4	Vog 5
Vdd 0	Vdd 1	Vdd 2	Vdd 3	Vdd 4	Vdd 5

Stage 9. Vsub and Heater Control testing - Table 9

DAC Value	Vsub Measured Voltage Test Data 10%	50%	90%
Signal	volts	volts	volts
Vsub - rate	-1.27	3.76	8.79
Vsub - Limit	-1.27	3.75	8.79
Vsub0	0.00	3.75	8.75
	Vsub Enable Bit - pass		

DAC Value	Telemetery Readback Test Data 10%	50%	90%
Signal	dec	dec	dec
Vbias 0	154	296	100
Vbias 1	-29	696	1420
RTD1	220	NA	NA
RTD2	248	NA	NA
RTD3	275	NA	NA
RTD4	303	NA	NA
RTD5	326	NA	NA
RTD6	353	NA	NA
Reference 4096	837	NA	NA
eference buffere	837	NA	NA

Stage 10. Video Offset DAC Tests - Table 10.

	DAC Value 410				DAC Value 2048				DAC Value 3686			
ADC	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU
0	0.250	NA	NA	17166	1.250		NA	81134	2.250	NA	500ms	145100
1	0.250	NA	NA	17024	1.250		NA	81059	2.250	NA	500ms	145103
2	0.250	NA	NA	17168	1.250		NA	81154	2.250	NA	500ms	1451144
3	0.250	NA	NA	16786	1.250		NA	80886	2.250	NA	500ms	144990
4	0.250	NA	NA	17090	1.250		NA	81140	2.250	NA	500ms	145189
5	0.250	NA	NA	17060	1.250		NA	81101	2.250	NA	500ms	145136
6	0.250	NA	NA	17056	1.250		NA	81070	2.250	NA	500ms	145079
7	0.250	NA	NA	17089	1.250		NA	81193	2.250	NA	500ms	145306
8	0.250	NA	NA	17070	1.250		NA	81127	2.250	NA	500ms	145181
9	0.250	NA	NA	17081	1.250		NA	81146	2.250	NA	500ms	145203
10	0.250	NA	NA	17162	1.250		NA	81187	2.250	NA	500ms	145218
11	0.250	NA	NA	17132	1.250		NA	81188	2.250	NA	500ms	145242

ADC	DC Volts		Data Set		
Channel	Slope	Offset	410	2048	3686
0	1638.000	0.500	0.250	1.250	2.250
1	1638.000	0.500	0.250	1.250	2.250
2	1638.000	0.500	0.250	1.250	2.250
3	1638.000	0.500	0.250	1.250	2.250
4	1638.000	0.500	0.250	1.250	2.250
5	1638.000	0.500	0.250	1.250	2.250
6	1638.000	0.500	0.250	1.250	2.250
7	1638.000	0.500	0.250	1.250	2.250
8	1638.000	0.500	0.250	1.250	2.250
9	1638.000	0.500	0.250	1.250	2.250
10	1638.000	0.500	0.250	1.250	2.250
11	1638.000	0.500	0.250	1.250	2.250

(dac# -offset)/slope=Voltage

ADC	ADU's		Data Set		
Channel	Slope	Offset	410	2048	3686
0	0.026	-29.58	17166	81134	145100
1	0.026	-25.40	17024	81059	145103
2	0.002	1123.63	17168	81154	1451144
3	0.026	-18.92	16786	80886	144990
4	0.026	-27.06	17090	81140	145189
5	0.026	-26.40	17060	81101	145136
6	0.026	-26.47	17056	81070	145079
7	0.026	-26.59	17089	81193	145306
8	0.026	-26.52	17070	81127	145181
9	0.026	-26.78	17081	81146	145203
10	0.026	-29.02	17162	81187	145218
11	0.026	-28.10	17132	81188	145242

(dac# -offset)/slope=ADU

Notes and Observations

Checked for oscillations using a Agilent Oscilloscope on AC. OK

Stage 11. CDS Control Functions and Video Channel Performanc

TEST #1: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit is held static. The purpose of this test is to verify the correct operation of the ADC devices and measure the noise of the Offset voltage generators, ADC buffer amplifiers and ADC devices

Noise Test 1

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	81123	81139	81131.2	2.24875
CH 1	81052	81070	81060.5	2.21042
CH 2	81146	81163	81154.3	2.16502
CH 3	80876	80894	80884.5	2.2671
CH 4	81131	81147	81139	2.25408
CH 5	81092	81108	81099.4	2.34068
CH 6	81063	81078	81071	2.31149
CH 7	81187	81204	81195.6	2.38549
CH 8	81121	81137	81129.3	2.27541
CH 9	81133	81152	81143.2	2.36532
CH 10	81180	81195	81187.6	2.34577
CH 11	81179	81196	81187.1	2.3496

TEST #2: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the invert/non-invert and the DC Restore switches are held static.

Noise Test 2

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76527	76547	76537.7	2.6934
CH 1	76872	76895	76881.4	2.84809
CH 2	76752	76774	76763.3	2.89131
CH 3	76693	76716	76703.8	2.86534
CH 4	76449	76470	76460.5	2.76634
CH 5	76843	76863	76852.5	2.89098
CH 6	76792	76814	76802.9	2.63364
CH 7	77269	77290	77280.5	2.75314
CH 8	76870	76889	76879.6	2.76121
CH 9	77045	77065	77055	2.84151
CH 10	76922	76942	76931.2	2.83067
CH 11	77156	77176	77165.6	2.88827

TEST #3: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the DC Restore switch is held static.

Noise Test 3

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76505	76528	76514.6	3.01488
CH 1	76876	76898	76886.9	3.05878
CH 2	76751	76774	76763.7	3.10697
CH 3	76685	76706	76694.2	2.94303
CH 4	76452	76473	76462.7	2.98582
CH 5	76844	76868	76855.9	2.98394
CH 6	76789	76812	76801	2.93094
CH 7	77273	77296	77285.1	2.96287
CH 8	76858	76883	76870.2	2.80625
CH 9	77041	77063	77051.6	3.02983
CH 10	76923	76945	76934.8	3.09115
CH 11	77151	77173	77162.6	3.08421

TEST #4: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition.

Noise Test 4

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76492	76514	76503.4	3.01487
CH 1	76878	76901	76889.5	3.21966
CH 2	76755	76778	76766.1	3.23096
CH 3	76681	76706	76693.5	2.99842
CH 4	76488	76510	76498.4	3.07826
CH 5	76833	76856	76844.2	3.17075
CH 6	76795	76817	76805.8	3.02697
CH 7	77242	77266	77254	3.26289
CH 8	76897	76922	76910.4	3.12433
CH 9	76960	76984	76971.1	3.15336
CH 10	76942	76965	76953.2	3.16313
CH 11	77110	77132	77121.9	3.05521

TEST #5: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the circuitry set to high GAIN.

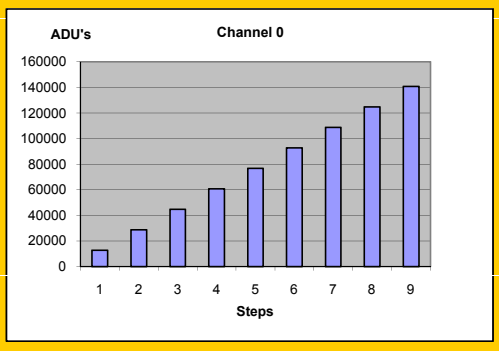
Noise Test 5

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76498	76525	76511.3	3.63184
CH 1	76887	76915	76901.7	3.58024
CH 2	76768	76797	76781.8	3.68456
CH 3	76685	76713	76700	3.68488
CH 4	76489	76514	76501.8	3.62128
CH 5	76829	76856	76842.6	3.656
CH 6	76795	76820	76807.9	3.55489
CH 7	77243	77267	77255.3	3.70485
CH 8	76946	76973	76959.5	3.6484
CH 9	76956	76983	76969.5	3.64841
CH 10	76997	77024	77011.1	3.4974
CH 11	77109	77134	77122.2	3.5617

TEST #6A: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

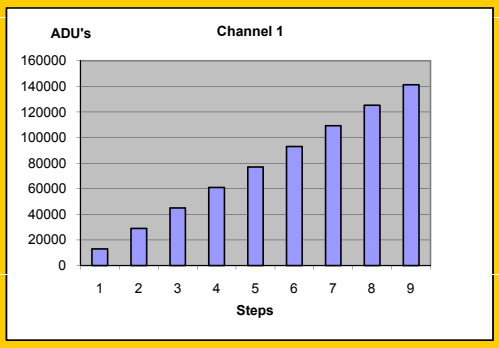
BrdTst6_006 / Channel 0					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12821	12846	12832	3.20681	10%
0x333	28795	28815	28805.1	3.10583	20%
0x4cc	44764	44787	44776.4	3.10669	30%
0x666	60776	60798	60787.8	3.14343	40%
0x800	76788	76808	76798.6	3.00688	50%
0x999	92759	92782	92770.5	3.15506	60%
0xb33	108770	108793	108782	3.11433	70%
0xccc	124746	124771	124758	3.11923	80%
0xe66	140759	140782	140770	3.01964	90%



TEST #6B: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

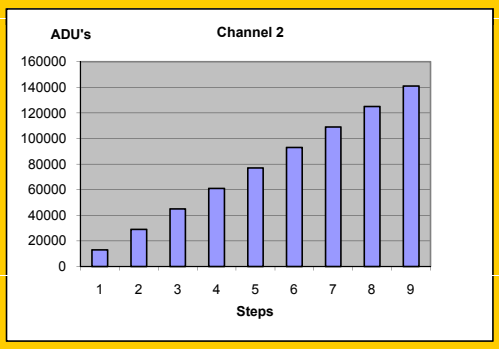
BrdTst6_006 / Channel 1					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13084	13105	13093.6	3.00409	10%
0x333	29074	29097	29085.3	3.11281	20%
0x4cc	45060	45083	45072.2	3.21175	30%
0x666	61091	61114	61102.5	3.22072	40%
0x800	77118	77142	77129.6	3.17984	50%
0x999	93110	93134	93120.8	3.24575	60%
0xb33	109140	109162	109151	3.23461	70%
0xccc	125130	125152	125141	3.15474	80%
0xe66	141160	141184	141171	3.29654	90%



TEST #6C: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

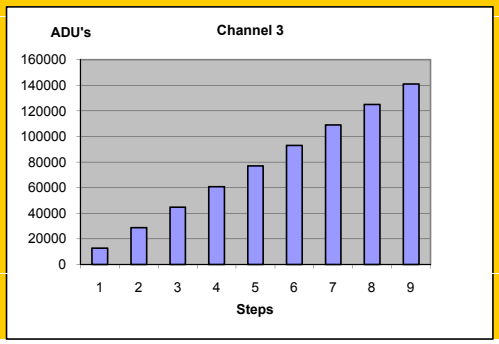
BrdTst6_006 / Channel 2					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13058	13080	13069	3.17869	10%
0x333	29034	29055	29045.2	3.12104	20%
0x4cc	45013	45035	45024.6	3.20953	30%
0x666	61029	61053	61040.2	3.18972	40%
0x800	77043	77068	77056	3.22788	50%
0x999	93025	93046	93035.3	3.21585	60%
0xb33	109041	109065	109051	3.27723	70%
0xccc	125022	125044	125034	3.22948	80%
0xe66	141040	141064	141051	3.3025	90%



TEST #6D: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

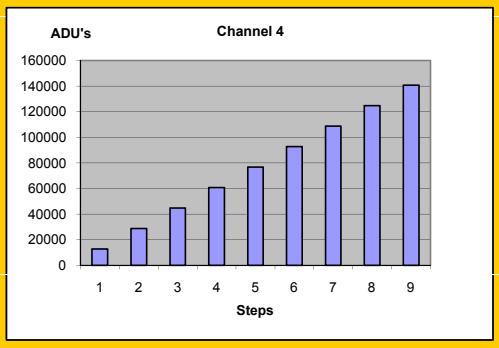
BrdTst6_006 / Channel 3					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12812	12835	12823.8	3.19471	10%
0x333	28817	28841	28830.2	3.10812	20%
0x4cc	44819	44844	44832.3	3.21726	30%
0x666	60866	60888	60877.6	3.15416	40%
0x800	76910	76933	76921.2	3.1342	50%
0x999	92913	92941	92926.9	3.21216	60%
0xb33	108959	108982	108972	3.12866	70%
0xccc	124965	124989	124977	3.27326	80%
0xe66	141012	141034	141023	3.21402	90%



TEST #6E: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

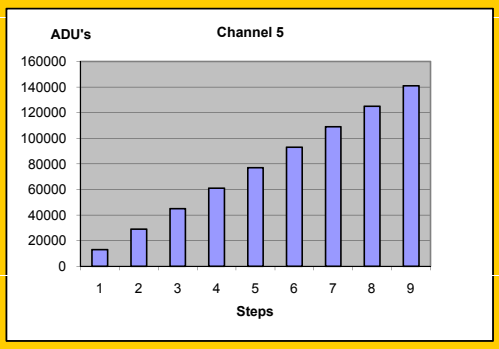
BrdTst6_006 / Channel 4					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12746	12768	12757	3.11942	10%
0x333	28740	28762	28750.6	3.17353	20%
0x4cc	44726	44751	44739.1	3.22181	30%
0x666	60758	60782	60770.7	3.21254	40%
0x800	76790	76818	76802.7	3.24905	50%
0x999	92785	92808	92796.3	3.20489	60%
0xb33	108816	108840	108829	3.17101	70%
0xccc	124809	124833	124822	3.07786	80%
0xe66	140845	140868	140856	3.26397	90%



TEST #6F: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

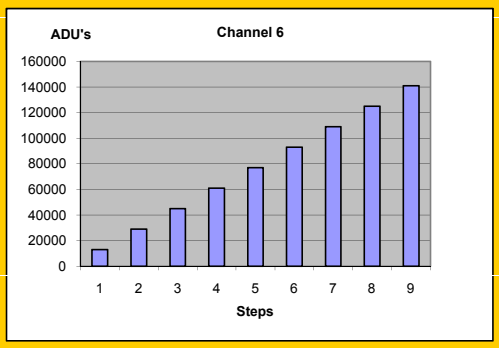
BrdTst6_006 / Channel 5					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13043	13065	13054.5	3.10759	10%
0x333	29034	29056	29044.2	2.98209	20%
0x4cc	45020	45044	45032	3.17352	30%
0x666	61051	61072	61061.7	3.11495	40%
0x800	77073	77098	77086.1	3.14938	50%
0x999	93066	93089	93077.5	3.17968	60%
0xb33	109096	109117	109106	3.09175	70%
0xccc	125086	125113	125097	3.28545	80%
0xe66	141114	141139	141127	3.22632	90%



TEST #6G: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

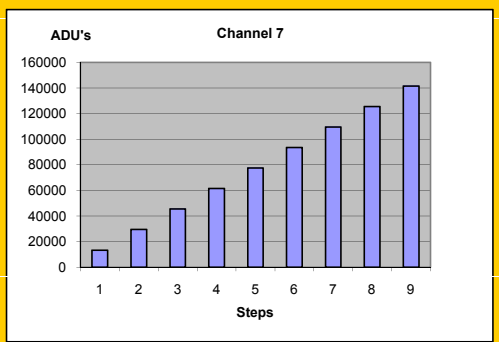
BrdTst6_006 / Channel 6					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13018	13040	13029.2	2.9982	10%
0x333	29000	29024	29011.4	3.19543	20%
0x4cc	44983	45005	44993.7	3.13242	30%
0x666	61002	61025	61014.8	3.12643	40%
0x800	77021	77044	77032.5	3.13874	50%
0x999	93002	93026	93014.9	3.19135	60%
0xb33	109026	109047	109036	3.16729	70%
0xccc	125007	125031	125020	3.18743	80%
0xe66	141029	141055	141042	3.1189	90%



TEST #6H: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

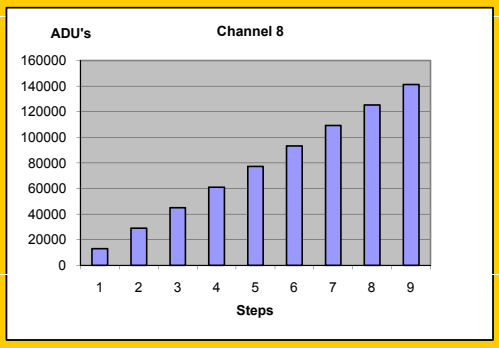
BrdTst6_006 / Channel 7					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13367	13390	13378.5	3.11723	10%
0x333	29375	29398	29387.2	3.23463	20%
0x4cc	45382	45405	45393.2	3.22493	30%
0x666	61427	61451	61440.1	3.13651	40%
0x800	77473	77497	77485.8	3.22517	50%
0x999	93482	93503	93492.4	3.25487	60%
0xb33	109528	109551	109539	3.22962	70%
0xccc	125537	125560	125548	3.24944	80%
0xe66	141583	141605	141595	3.26578	90%



TEST #6I: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

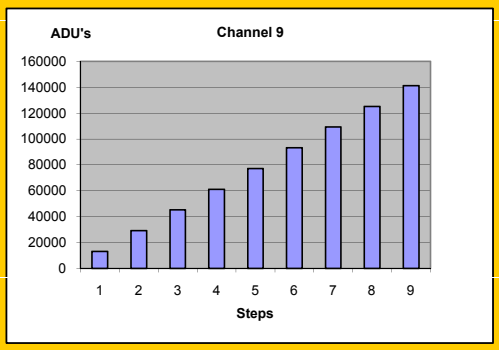
BrdTst6_006 / Channel 8					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13095	13120	13107.7	3.09418	10%
0x333	29089	29111	29100.7	3.1001	20%
0x4cc	45081	45106	45094.5	3.10847	30%
0x666	61115	61136	61126.8	3.13223	40%
0x800	77149	77170	77158.7	3.13007	50%
0x999	93145	93169	93156.4	3.04298	60%
0xb33	109177	109199	109188	3.04644	70%
0xccc	125173	125197	125185	3.16104	80%
0xe66	141208	141230	141219	3.11487	90%



TEST #6J: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

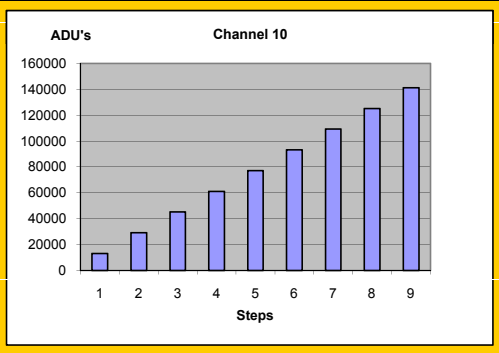
BrdTst6_006 / Channel 9					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13158	13182	13170.5	3.02033	10%
0x333	29156	29179	29166.5	3.171	20%
0x4cc	45150	45173	45161.8	3.12491	30%
0x666	61186	61207	61196.8	3.09784	40%
0x800	77216	77239	77225.7	3.18677	50%
0x999	93210	93233	93221.2	3.13234	60%
0xb33	109244	109267	109255	3.2022	70%
0xccc	125242	125267	125253	3.22549	80%
0xe66	141277	141301	141289	3.28094	90%



TEST #6K: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

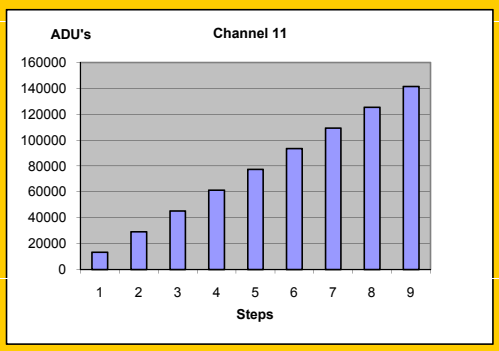
BrdTst6_006 / Channel 10					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13177	13203	13190.2	3.08559	10%
0x333	29166	29190	29177.6	3.15594	20%
0x4cc	45152	45177	45163.4	3.15018	30%
0x666	61180	61201	61190.2	3.05179	40%
0x800	77202	77228	77214.2	3.16429	50%
0x999	93191	93213	93203	3.06874	60%
0xb33	109217	109241	109229	3.20899	70%
0xccc	125208	125229	125219	3.03754	80%
0xe66	141234	141256	141245	3.1956	90%



TEST #6L: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

BrdTst6_006 / Channel 11					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13312	13335	13322.2	3.21704	10%
0x333	29303	29326	29315.6	3.30699	20%
0x4cc	45298	45321	45309.1	3.15164	30%
0x666	61330	61353	61341.4	3.24365	40%
0x800	77363	77387	77374.5	3.28422	50%
0x999	93360	93380	93370.1	3.2637	60%
0xb33	109391	109415	109403	3.27662	70%
0xccc	125387	125410	125399	3.15872	80%
0xe66	141421	141444	141432	3.2513	90%



Stage 13. Other Bit Tests. Table 11

Electronic Serial Number	0xDB8EC9		Board Serial Number	14
Firmware Version	0x193		Name Of Person Testing	S. Holm
Ident Register	0x502		Board passed Functional Tests	YES