DES 12 Channel Board - Functional Tests: CCD Acquisition Board Revision 1.0

Stage 1. Preparation of documentation and configuration settings - Table 1.

Board Part Number	20		Board Serial Number	0xDB8F82
Date Of Tests	August 2010		Name Of Person Testing	S. Holm
Suggested Filename To Save	CCDACQ_12Ch_REPORT_BOARD12.xl		Sequence number: Test	

Stage 3. Power plane short test - Table 2.

Supply Name	Short test to ground: Impedance to ground	Test Point	
+1.2VD	44.00	TP43	~50 ohms
+1.8VD	1.2M	TPB12	> 1K ohm
+2.5VD	20k	TPB11	> 1K ohm
+3.3VD	6k	D13	> 1K ohm
+5VD	20k	D14	> 1K ohm
+5VA	4M	C267	> 1K ohm
-5VA	37K	C270	> 1K ohm
+15VA	2.4M	C288	> 1K ohm
-15VA	2.4M	C282	> 1K ohm
-28VA	2.7M	C307	> 1K ohm

Stage 4. Firmware programming tests - Table 3.

JTAG Order	Designator	Device	Load File	Check Sum or User Code
1	U122	XCF08PFS48C PROM	CcdAcqFpgaV41.mcs	0014ef670
2	U114	Spartan3 XC3S2000 FPGA	ccdacqfpgav41.bit	5102801

Stage 5. Power Consumption - Table 4.

Supply Name	Power Supply Consumption: Measured Voltage at test point	Measured Current on power supply	Test Point	
+1.2VD	1.20	N/A	TP43	
+1.8VD	1.80	N/A	TPB12	
+2.5VD	2.50	N/A	TPB11	
+3.3VD	3.30	0.129	D13	
+5VD	5.20	0.15	D14	
+5VA	5.04	0.6	C267	
-5VA	-5.00	0.44	C270	
+15VA	14.97	0.567	C288	
-15VA	-15.07	0.408	C282	
-28VA	-27.70	0.22	C307	
Vref 0+	10.07	N/A	R534	Vsub+ Reference(+10v)
Vref 0-	-2.48	N/A	R525	Vsub - Reference(-2.5v)
Vref Offset	2.50	N/A	R573	ADC Offset Reference(+2.5v)
Vclamp	1.88	N/A	VIA	ADC Clamp Voltage(+1.8v)
ADC Ref.	2.50	N/A	VIA	ADC Reference Voltage(+2.5v)
Vref 1+	2.50	N/A	R537	Vru and Vrl + Reference(+2.5v)
Vref 1-	-9.94	N/A	R535	Vru and Vrl - Reference(-10v)
Vref 2+	5.00	N/A	R563	Vog + Reference(+5v)
Vref 2-	-2.48	N/A	R555	Vog - Reference(-2.5v)
Vref 3+	2.50	N/A	R543	Vdd + Reference(+2.5v)
Vref 3-	-10.00	N/A	R571	Vdd - Reference(-10v)

Power Dissipation:
27.2 Watts

~27 watts +/- 5%

Stage 7. Basic Bus Transactions - **D**igital **Register** Tests - Table 5.

Register name	Put an X on any bit that has an error: 31-24	23-16	15-08	07-00	Function	Test name: Pattern	Walking 0's	Walking 1's
CDS Control			00000000	00000000	16 bit R/W			
Digital Output	00000000	00000000	00000000	00000000	32 bit R/W			
ADC Config.			0000	00000000	12 bit R/W			
Offset DAC			0000	00000000	12 bit R/W			
Bias DAC			0000	00000000	12 bit R/W			
Telemetry Config.				0000	4 bit R/W			
Auxilary Config.			00	00000000	10 bit R/W			
Redirect				0000	4 bit R/W			
Pixel Transfer				00000000	8 bit R/W			
Micro SEQ			00000000	00000000	16 bit R/W			
RAM Buffer			00000000	00000000	16 bit R/W			
LED Control				0000	4 bit R/W			
Control			00000000	00000000	16 bit R/W			
All Register Test	00000000	00000000	00000000	00000000	16 bit R/W	**Passed**	**Passed**	**Passed**

Stage 8. Bias Voltage settings and output enables testing - Table 8

DAC Value	410	Bias Voltage Test Data 2048	3686	50% rms Noise	10-90% Rise Time			
Signal	volts	volts	volts	uV	millisec.	Fanout Brd	Slope	Offset
Vru 0	-13.06	-5.59	1.88	<10	1	BIAS 3	219.28	3273.76
Vru 1	-13.04	-5.58	1.88	<10	1	BIAS 4	219.57	3273.21
Vru 2	-13.02	-5.57	1.88	<10	1	BIAS 5	219.87	3272.65
Vru 3	-13.05	-5.58	1.88	<10	1	BIAS 6	219.42	3273.12
Vru 4	-13.04	-5.58	1.88	<10	1	BIAS 7	219.57	3273.21
Vru 5	-13.06	-5.59	1.88	<10	1	BIAS 8	219.28	3273.76
Vru 6	-13.05	-5.58	1.88	NA	NA	BIAS 9	219.42	3273.12
Vru 7	-13.05	-5.58	1.88	NA	NA	BIAS 10	219.42	3273.12
Vrl 0	-13.04	-5.58	1.88	<10	1	BIAS 11	219.57	3273.21
Vrl 1	-13.05	-5.58	1.88	<10	1	BIAS 12	219.42	3273.12
Vrl 2	-13.07	-5.59	1.88	<10	1	BIAS 13	219.13	3273.67
Vrl 3	-13.05	-5.58	1.88	<10	1	BIAS 14	219.42	3273.12
Vrl 4	-13.05	-5.58	1.88	<10	1	BIAS 15	219.42	3273.12
Vrl 5	-13.04	-5.58	1.88	<10	1	BIAS 16	219.57	3273.21
Vrl 6	-13.04	-5.58	1.88	NA	NA	BIAS 17	219.57	3273.21
Vrl 7	-13.06	-5.59	1.88	NA	NA	BIAS 18	219.28	3273.76
Vog 0	-1.73	1.26	4.25	<10	1	BIAS 19	547.83	1357.74
Vog 1	-1.73	1.26	4.25	<10	1	BIAS 20	547.83	1357.74
Vog 2	-1.73	1.26	4.25	<10	1	BIAS 21	547.83	1357.74
Vog 3	-1.73	1.26	4.25	<10	1	BIAS 22	547.83	1357.74
Vog 4	-1.73	1.26	4.25	<10	1	BIAS 23	547.83	1357.74
Vog 5	-1.73	1.26	4.25	<10	1	BIAS 24	547.83	1357.74
Vog 6	-1.73	1.26	4.25	NA	NA	BIAS 25	547.83	1357.74
Vog 7	-1.73	1.26	4.25	NA	NA	BIAS 26	547.83	1357.74
Vdd 0	-21.91	-9.39	3.12	<10	20	BIAS 27	130.88	3277.43
Vdd 1	-21.85	-9.37	3.12	<10	20	BIAS 28	131.20	3276.88
Vdd 2	-21.93	-9.41	3.12	<10	20	BIAS 29	130.78	3278.19
Vdd 3	-21.88	-9.38	3.12	<10	20	BIAS 30	131.04	3277.16
Vdd 4	-21.88	-9.38	3.12	<10	20	BIAS 21	131.04	3277.16
Vdd 5	-21.87	-9.38	3.12	<10	20	BIAS 32	131.09	3277.21
Vdd 6	-21.95	-9.41	3.13	NA	NA	BIAS 33	130.62	3277.15
Vdd 7	-21.94	-9.41	3.13	NA	NA	BIAS 34	130.67	3277.21

Vru	Slope		Offset
Mean	219.48	Mean	3273.24
Stdev	0.1792868	Stdev	0.341270187
Average	219.47924	Average	3273.241798
	Dac #	Average voltage	
	0	-14.0	
	4095	3.7	

Vrl	Slope		Offset
Mean	219.42	Mean	3273.30
Stdev	0.146903	Stdev	0.243375879
Average	219.42406	Average	3273.299852
	Dac #	Average voltage	
	0	-14.9	
	4095	3.7	

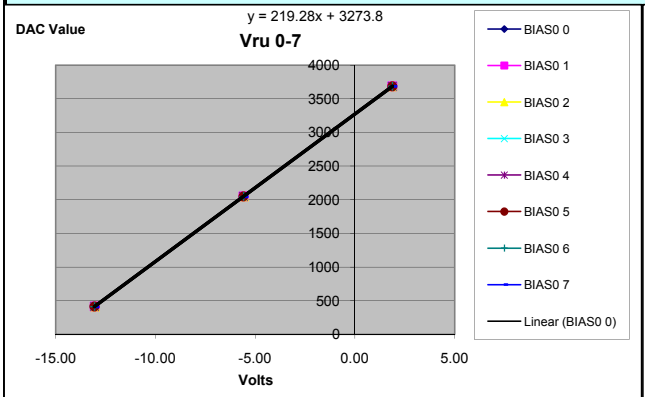
Vog	Slope		Offset
Mean	547.83	Mean	1357.74
Stdev	0	Stdev	0
Average	547.82609	Average	1357.73913
	Dac #	Average voltage	
	0	-2.5	
	4095	5.0	

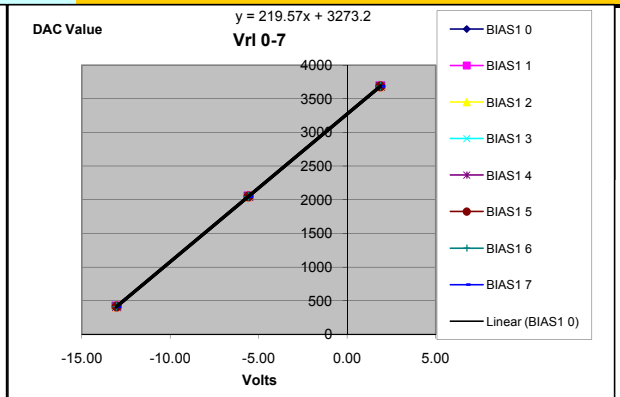
Vdd	Slope		Offset
Mean	130.92	Mean	3277.30
Stdev	0.1955897	Stdev	0.364182093
Average	130.91592	Average	3277.297507
	Dac #	Average voltage	
	0	-25.0	
	4095	6.3	

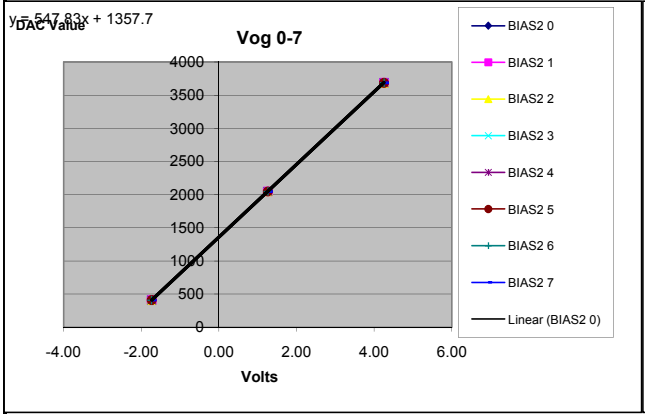
Notes and Observations

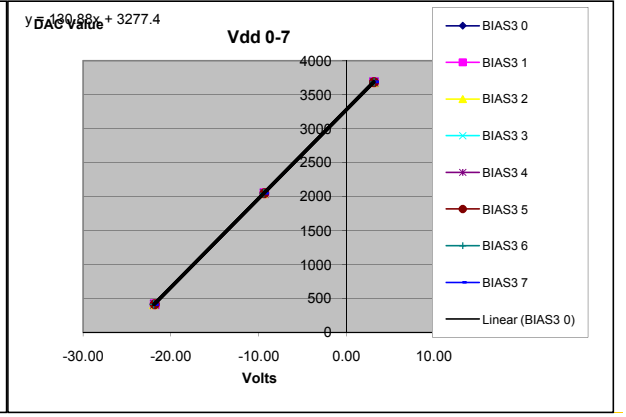
Checked for oscillations using a Agilent Oscilloscpe on AC.**OK**

average min & max voltages
(dac# -offset)/slope=voltage









Stage 8B. Telemetry System Tests - Table 7 (Bias Telemetry Tests)

DAC Value	410	3686	Bias Signals Set Volts		Resolved Values for Telemetry Channel	
	Telemetry Return Values					
Signal	10%	90%	10%	90%	Slope	Offset
Vru 0	-1750	424	-13.06	1.88	145.5154	150.43
Vru 1	-1746	424	-13.04	1.88	145.4424	150.57
Vru 2	-1744	424	-13.02	1.88	145.5034	150.45
Vru 3	-1747	424	-13.05	1.88	145.4119	150.63
Vru 4	-1747	424	-13.04	1.88	145.5094	150.44
Vru 5	-1749	424	-13.06	1.88	145.4485	150.56
Vru 6	-1752	424	-13.05	1.88	145.7468	150.00
Vru 7	-1748	424	-13.05	1.88	145.4789	150.50
Vrl 0	-1729	424	-13.04	1.88	144.3029	152.71
Vrl 1	-1728	424	-13.05	1.88	144.1393	153.02
Vrl 2	-1731	424	-13.07	1.88	144.1472	153.00
Vrl 3	-1733	424	-13.05	1.88	144.4742	152.39
Vrl 4	-1729	424	-13.05	1.88	144.2063	152.89
Vrl 5	-1730	425	-13.04	1.88	144.4370	153.46
Vrl 6	-1732	424	-13.04	1.88	144.5040	152.33
Vrl 7	-1733	424	-13.06	1.88	144.3775	152.57
Vog 0	-358	867	-1.73	4.25	204.8495	-3.61
Vog 1	-358	867	-1.73	4.25	204.8495	-3.61
Vog 2	-357	867	-1.73	4.25	204.6823	-2.90
Vog 3	-358	867	-1.73	4.25	204.8495	-3.61
Vog 4	-358	867	-1.73	4.25	204.8495	-3.61
Vog 5	-358	867	-1.73	4.25	204.8495	-3.61
Vog 6	-358	867	-1.73	4.25	204.8495	-3.61
Vog 7	-358	867	-1.73	4.25	204.8495	-3.61
Vdd 0	-1707	574	-21.91	3.12	91.1306	289.67
Vdd 1	-1700	574	-21.85	3.12	91.0693	289.86
Vdd 2	-1705	575	-21.93	3.12	91.0180	291.02
Vdd 3	-1704	574	-21.88	3.12	91.1200	289.71
Vdd 4	-1700	574	-21.88	3.12	90.9600	290.20
Vdd 5	-1700	574	-21.87	3.12	90.9964	290.09
Vdd 6	-1711	575	-21.95	3.13	91.1483	289.71
Vdd 7	-1713	575	-21.94	3.13	91.2645	289.34

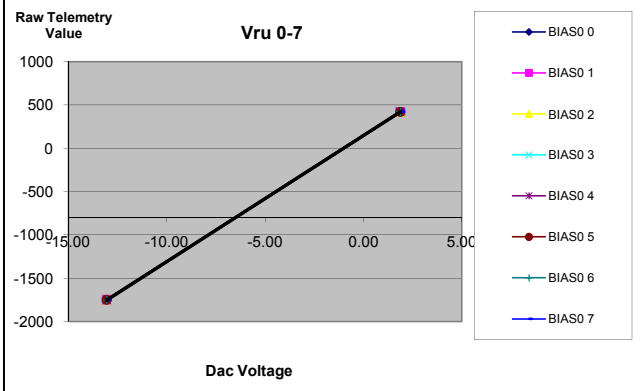
AVERAGE

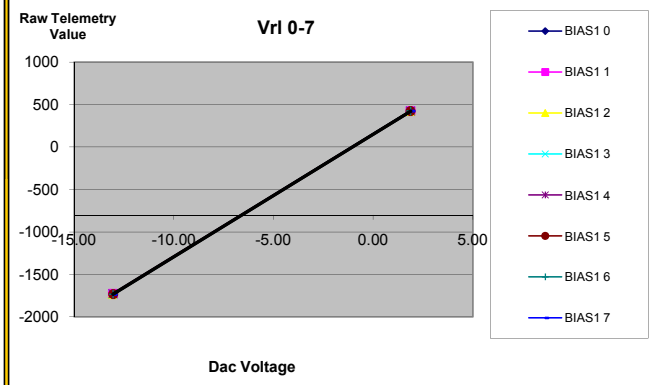
Vru	Slope		Offset
Mean	145.51	Mean	150.45
Stdev	0.0968484	Stdev	0.182075

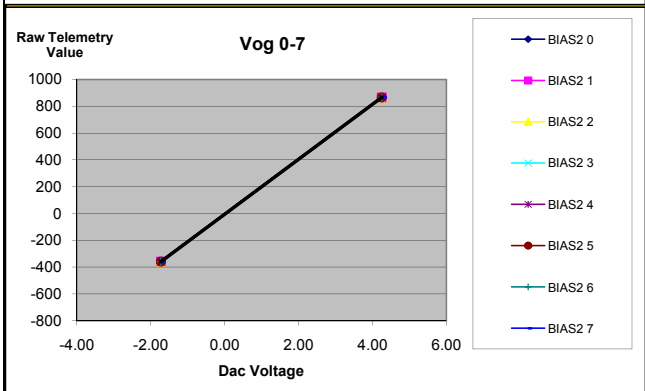
Vrl	Slope		Offset
Mean	144.32	Mean	152.80
Stdev	0.1370586	Stdev	0.3499318

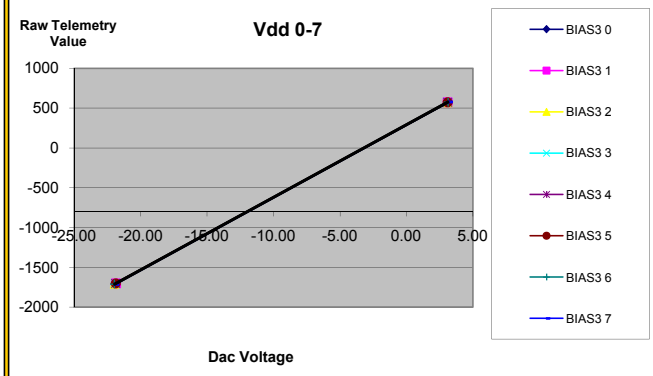
Vog	Slope		Offset
Mean	204.83	Mean	-3.52
Stdev	0.0553042	Stdev	0.2350427

Vdd	Slope		Offset
Mean	91.09	Mean	289.95
Stdev	0.0919569	Stdev	0.4758526









Stage 8C. Bias Voltage output enables testing - Table 8

Place a line through Bias Voltage name if enable/disable switch works

Vru 0	Vru 1	Vru 2	Vru 3	Vru 4	Vru 5
Vrl 0	Vrl 1	Vrl 2	Vrl 3	Vrl 4	Vrl 5
Vog 0	Vog 1	Vog 2	Vog 3	Vog 4	Vog 5
Vdd 0	Vdd 1	Vdd 2	Vdd 3	Vdd 4	Vdd 5

Stage 9. Vsub and Heater Control testing - Table 9

DAC Value	Vsub Measured Voltage Test Data 10%	50%	90%
Signal	volts	volts	volts
Vsub - rate	-1.22	3.79	8.81
Vsub - Limit	-1.22	3.79	8.81
Vsub0	0.00	0.00	0.00
	Vsub Enable Bit - pass		

DAC Value	Telemetery Readback Test Data 10%	50%	90%
Signal	dec	dec	dec
Vbias 0	152	265	407
Vbias 1	-29	702	1433
RTD1	219	NA	NA
RTD2	248	NA	NA
RTD3	274	NA	NA
RTD4	303	NA	NA
RTD5	323	NA	NA
RTD6	351	NA	NA
Reference 4096	836	NA	NA
eference buffere	836	NA	NA

Stage 10. Video Offset DAC Tests - Table 10.

	DAC Value 410				DAC Value 2048				DAC Value 3686			
ADC	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU
0	0.250	NA	NA	17050	1.250		NA	81112	2.250	NA	500ms	145182
1	0.250	NA	NA	17174	1.250		NA	81188	2.250	NA	500ms	145206
2	0.250	NA	NA	17148	1.250		NA	81169	2.250	NA	500ms	145188
3	0.250	NA	NA	17125	1.250		NA	81234	2.250	NA	500ms	145335
4	0.250	NA	NA	17024	1.250		NA	81078	2.250	NA	500ms	145134
5	0.250	NA	NA	17302	1.250		NA	81269	2.250	NA	500ms	145242
6	0.250	NA	NA	17259	1.250		NA	81234	2.250	NA	500ms	145214
7	0.250	NA	NA	17150	1.250		NA	81179	2.250	NA	500ms	145200
8	0.250	NA	NA	17114	1.250		NA	81141	2.250	NA	500ms	145161
9	0.250	NA	NA	17100	1.250		NA	81169	2.250	NA	500ms	145245
10	0.250	NA	NA	17070	1.250		NA	81060	2.250	NA	500ms	145048
11	0.250	NA	NA	17164	1.250		NA	81204	2.250	NA	500ms	145239

ADC	DC Volts		Data Set		
Channel	Slope	Offset	410	2048	3686
0	1638.000	0.500	0.250	1.250	2.250
1	1638.000	0.500	0.250	1.250	2.250
2	1638.000	0.500	0.250	1.250	2.250
3	1638.000	0.500	0.250	1.250	2.250
4	1638.000	0.500	0.250	1.250	2.250
5	1638.000	0.500	0.250	1.250	2.250
6	1638.000	0.500	0.250	1.250	2.250
7	1638.000	0.500	0.250	1.250	2.250
8	1638.000	0.500	0.250	1.250	2.250
9	1638.000	0.500	0.250	1.250	2.250
10	1638.000	0.500	0.250	1.250	2.250
11	1638.000	0.500	0.250	1.250	2.250

(dac# -offset)/slope=Voltage

ADC	ADU's		Data Set		
Channel	Slope	Offset	410	2048	3686
0	0.026	-25.89	17050	81112	145182
1	0.026	-29.42	17174	81188	145206
2	0.026	-28.75	17148	81169	145188
3	0.026	-27.61	17125	81234	145335
4	0.026	-25.33	17024	81078	145134
5	0.026	-33.01	17302	81269	145242
6	0.026	-30.96	17259	81234	145330
7	0.026	-29.54	17150	81179	145103
8	0.026	-28.21	17114	81141	145118
9	0.026	-27.23	17100	81169	145232
10	0.026	-26.10	17070	81060	145161
11	0.026	-29.77	17164	81204	145146

(dac# -offset)/slope=ADU

Notes and Observations

Checked for oscillations using a Agilent Oscilloscope on AC. OK

Stage 11. CDS Control Functions and Video Channel Performanc

TEST #1: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit is held static. The purpose of this test is to verify the correct operation of the ADC devices and measure the noise of the Offset voltage generators, ADC buffer amplifiers and ADC devices

Noise Test 1

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	81109	8.11E+04	81116.2	2.20589
CH 1	81183	8.12E+04	81192.4	2.27332
CH 2	81158	8.12E+04	81168	2.24924
CH 3	81225	8.12E+04	81234.7	2.35678
CH 4	81070	8.11E+04	81078.2	2.22234
CH 5	81264	8.13E+04	81272.4	2.32958
CH 6	81230	8.12E+04	81238.8	2.28436
CH 7	81170	8.12E+04	81177.5	2.38898
CH 8	81134	8.11E+04	81141.3	2.26826
CH 9	81166	81182	81173.6	2.37209
CH 10	81055	81070	81062.3	2.22669
CH 11	81195	81211	81203.3	2.20108

TEST #2: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the invert/non-invert and the DC Restore switches are held static.

Noise Test 2

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76499	7.65E+04	76510.5	2.72098
CH 1	76962	7.70E+04	76971	2.77694
CH 2	76570	7.66E+04	76581.6	2.73467
CH 3	77290	7.73E+04	77300.5	2.80682
CH 4	76279	7.63E+04	76288.6	2.66982
CH 5	77216	7.72E+04	77225.2	2.82957
CH 6	77157	7.72E+04	77166.8	2.77259
CH 7	77094	7.71E+04	77105.2	2.86413
CH 8	76584	7.66E+04	76592.8	2.73215
CH 9	77169	77189	77179.4	2.84122
CH 10	76745	76765	76755.7	2.69907
CH 11	77046	77065	77055.9	2.82954

TEST #3: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the DC Restore switch is held static.

Noise Test 3

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76499	7.65E+04	76509	2.9658
CH 1	76947	7.70E+04	76956.6	2.93113
CH 2	76567	7.66E+04	76576.9	2.91256
CH 3	77286	7.73E+04	77297.9	3.08469
CH 4	76280	7.63E+04	76290.5	2.88473
CH 5	77214	7.72E+04	77225.8	3.04659
CH 6	77145	7.72E+04	77155.8	2.84509
CH 7	77094	7.71E+04	77105.3	3.10266
CH 8	76580	7.66E+04	76590.7	2.9802
CH 9	77172	77194	77182.6	3.0176
CH 10	76747	76770	76757.9	2.95169
CH 11	77035	77057	77046.4	3.10105

TEST #4: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition.

Noise Test 4

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76489	7.65E+04	76499.9	3.05605
CH 1	76948	7.70E+04	76959	3.10155
CH 2	76569	7.66E+04	76579.8	3.00276
CH 3	77288	7.73E+04	77298.2	3.11981
CH 4	76314	7.63E+04	76326	3.06493
CH 5	77205	7.72E+04	77216.3	3.1629
CH 6	77151	7.72E+04	77161.4	3.10402
CH 7	77062	7.71E+04	77074.1	3.21669
CH 8	76620	7.66E+04	76633.9	3.06498
CH 9	77092	77117	77104.9	3.12062
CH 10	76766	76788	76776.9	3.09339
CH 11	76993	77018	77008	3.2177

TEST #5: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the circuitry set to high GAIN.

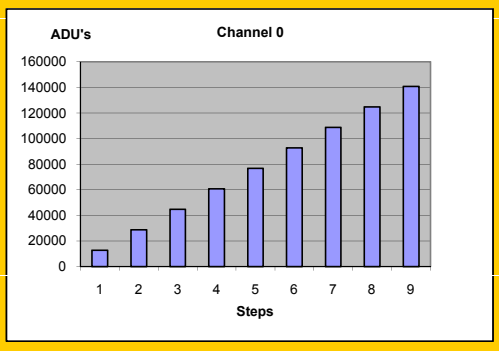
Noise Test 5

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76496	7.65E+04	76509.8	3.6456
CH 1	76958	7.70E+04	76970.1	3.6083
CH 2	76582	7.66E+04	76594.4	3.58398
CH 3	77292	7.73E+04	77304	3.61899
CH 4	76312	7.63E+04	76328.1	3.62878
CH 5	77200	7.72E+04	77214.3	3.60482
CH 6	77150	7.72E+04	77162.4	3.62349
CH 7	77059	7.71E+04	77073.9	3.70562
CH 8	76673	7.67E+04	76685	3.65337
CH 9	77089	77116	77104.2	3.63477
CH 10	76822	76846	76835.2	3.28845
CH 11	76994	77024	77006.8	3.65965

TEST #6A: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

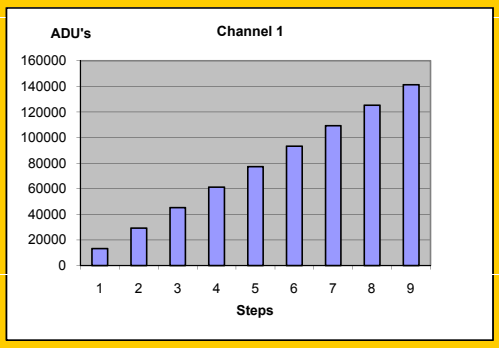
BrdTst6_006 / Channel 0					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12724	12748	12735.7	3.13317	10%
0x333	28720	28743	28732.7	3.04999	20%
0x4cc	44719	44741	44729.9	3.04888	30%
0x666	60754	60775	60765.1	3.08315	40%
0x800	76791	76814	76802.1	2.94685	50%
0x999	92787	92809	92797.7	3.05546	60%
0xb33	108824	108844	108833	3.0819	70%
0xccc	124821	124846	124833	3.01088	80%
0xe66	140859	140880	140870	3.14397	90%



TEST #6B: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

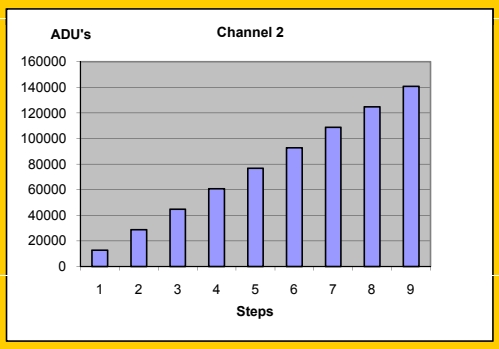
BrdTst6_006 / Channel 1					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13172	13195	13182.8	3.0567	10%
0x333	29159	29180	29169.8	3.16012	20%
0x4cc	45136	45161	45146.9	3.06459	30%
0x666	61161	61184	61173.6	3.06673	40%
0x800	77179	77201	77189.8	3.07855	50%
0x999	93164	93186	93174.8	3.10975	60%
0xb33	109191	109213	109202	3.14096	70%
0xccc	125169	125191	125180	3.12316	80%
0xe66	141197	141220	141208	3.1076	90%



TEST #6C: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

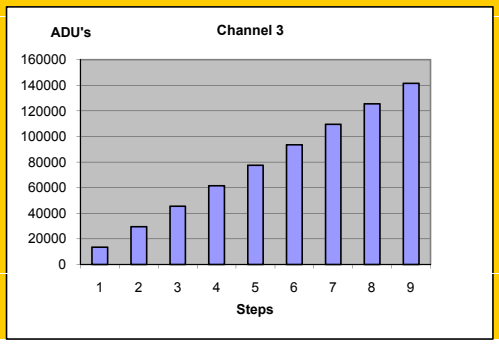
BrdTst6_006 / Channel 2					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12837	12860	12848	3.13633	10%
0x333	28820	28842	28831.8	3.1341	20%
0x4cc	44806	44826	44816.6	3.0508	30%
0x666	60828	60849	60839.2	3.09634	40%
0x800	76848	76872	76862.6	3.0953	50%
0x999	92837	92861	92849.7	3.00983	60%
0xb33	108862	108885	108873	3.12121	70%
0xccc	124848	124873	124861	3.11806	80%
0xe66	140872	140895	140884	2.99885	90%



TEST #6D: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

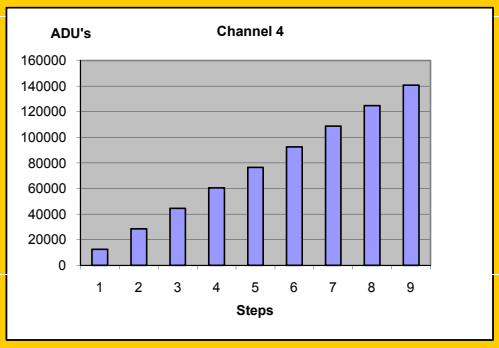
BrdTst6_006 / Channel 3					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13412	13434	13422.1	3.11418	10%
0x333	29421	29444	29431.2	3.05047	20%
0x4cc	45424	45446	45435.3	3.18551	30%
0x666	61470	61494	61482.3	3.12421	40%
0x800	77511	77536	77523.1	3.11563	50%
0x999	93519	93541	93530.4	3.10448	60%
0xb33	109566	109589	109578	3.16343	70%
0xccc	125574	125599	125585	3.14334	80%
0xe66	141623	141645	141633	3.18939	90%



TEST #6E: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

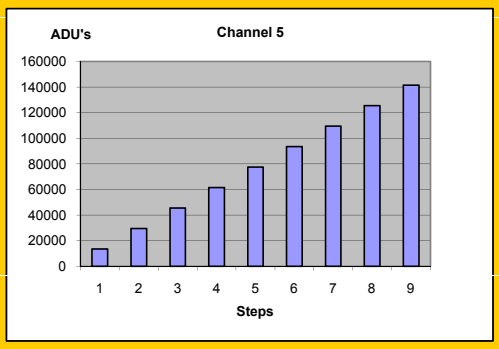
BrdTst6_006 / Channel 4					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12550	12574	12561	3.04539	10%
0x333	28544	28566	28555.9	3.04412	20%
0x4cc	44538	44560	44547.8	2.93849	30%
0x666	60571	60594	60582.2	3.06869	40%
0x800	76606	76629	76617.2	3.07601	50%
0x999	92601	92623	92611.3	3.12922	60%
0xb33	108635	108658	108646	3.03296	70%
0xccc	124629	124652	124641	3.13011	80%
0xe66	140662	140687	140676	3.03043	90%



TEST #6F: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

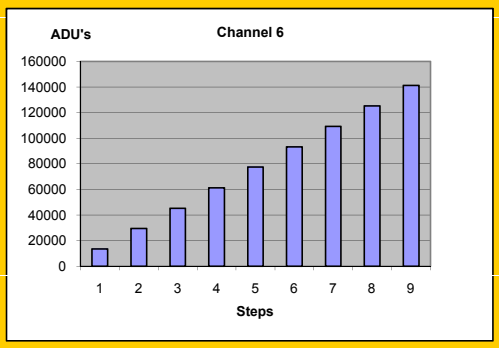
BrdTst6_006 / Channel 5					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13487	13510	13497.8	3.22248	10%
0x333	29458	29481	29469.5	3.12676	20%
0x4cc	45428	45452	45440	3.16709	30%
0x666	61440	61460	61450.1	3.17996	40%
0x800	77449	77474	77462.3	3.15305	50%
0x999	93424	93446	93435.8	3.16873	60%
0xb33	109435	109457	109446	3.08146	70%
0xccc	125411	125432	125421	3.19732	80%
0xe66	141419	141442	141432	3.16644	90%



TEST #6G: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

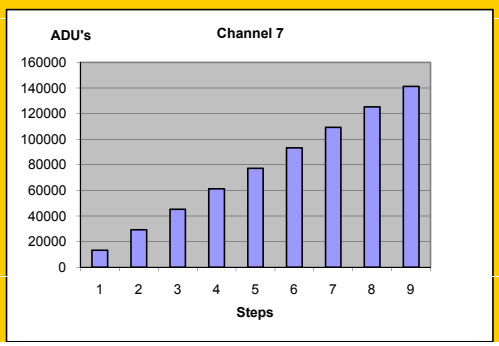
BrdTst6_006 / Channel 6					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13407	13429	13417.2	3.10829	10%
0x333	29381	29403	29391.7	3.13587	20%
0x4cc	45357	45379	45367.3	3.16507	30%
0x666	61368	61389	61379.2	3.16317	40%
0x800	77376	77398	77387.4	3.12865	50%
0x999	93352	93375	93363.3	3.14644	60%
0xb33	109364	109388	109377	3.04529	70%
0xccc	125344	125368	125355	3.13359	80%
0xe66	141356	141380	141368	3.23266	90%



TEST #6H: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

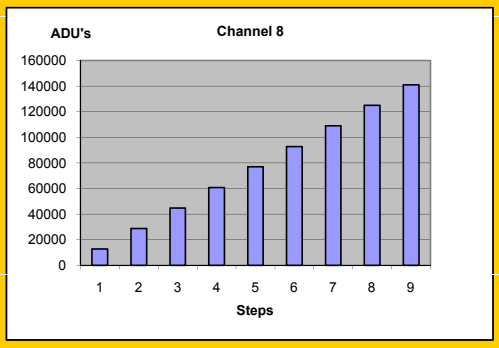
BrdTst6_006 / Channel 7					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13266	13291	13278.5	3.21852	10%
0x333	29254	29274	29264.6	3.12255	20%
0x4cc	45240	45264	45252.1	3.17241	30%
0x666	61267	61290	61278	3.18045	40%
0x800	77290	77313	77301	3.08602	50%
0x999	93277	93300	93288	3.14294	60%
0xb33	109301	109327	109314	3.17375	70%
0xccc	125292	125316	125304	3.14496	80%
0xe66	141319	141344	141330	3.19211	90%



TEST #6I: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

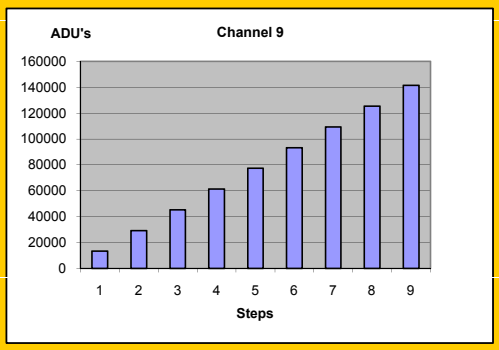
BrdTst6_006 / Channel 8					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12864	12888	12876.6	3.09883	10%
0x333	28851	28875	28864.6	3.15254	20%
0x4cc	44839	44860	44849.4	3.07189	30%
0x666	60865	60887	60875.1	3.07085	40%
0x800	76885	76911	76896.8	2.97564	50%
0x999	92872	92894	92882.8	2.89629	60%
0xb33	108898	108920	108909	3.08677	70%
0xccc	124886	124909	124897	3.12851	80%
0xe66	140913	140935	140923	3.05494	90%



TEST #6J: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

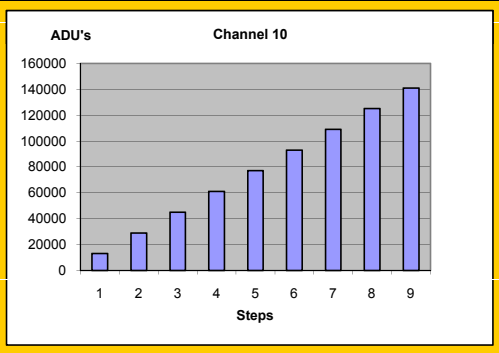
BrdTst6_006 / Channel 9					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13281	13304	13291.2	3.1572	10%
0x333	29278	29300	29288.1	3.17305	20%
0x4cc	45276	45299	45286.6	3.05668	30%
0x666	61314	61336	61324.6	3.20381	40%
0x800	77346	77369	77357.5	3.11068	50%
0x999	93343	93367	93355.2	3.1778	60%
0xb33	109380	109403	109392	3.07914	70%
0xccc	125382	125404	125393	3.16913	80%
0xe66	141419	141444	141431	3.16262	90%



TEST #6K: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

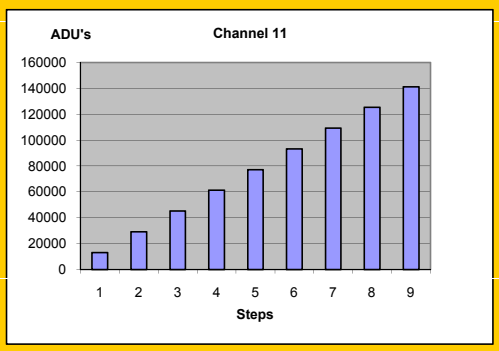
BrdTst6_006 / Channel 10					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13047	13069	13058.2	3.09949	10%
0x333	29025	29048	29037.6	3.07806	20%
0x4cc	45002	45025	45013.9	3.03623	30%
0x666	61020	61042	61031.9	3.11903	40%
0x800	77036	77057	77046.2	2.92909	50%
0x999	93014	93036	93025	3.09601	60%
0xb33	109032	109055	109044	2.98391	70%
0xccc	125013	125034	125024	3.13039	80%
0xe66	141030	141053	141042	3.23702	90%



TEST #6L: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

BrdTst6_006 / Channel 11					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13222	13246	13233.4	3.31988	10%
0x333	29213	29234	29222.9	3.15035	20%
0x4cc	45200	45223	45211.3	3.20677	30%
0x666	61228	61252	61240.1	3.23505	40%
0x800	77256	77277	77267.3	3.22861	50%
0x999	93245	93270	93257.4	3.18723	60%
0xb33	109275	109297	109286	3.24047	70%
0xccc	125265	125290	125278	3.2337	80%
0xe66	141296	141318	141307	3.20616	90%



Stage 13. Other Bit Tests. Table 11

Electronic Serial Number	0xDB8F82		Board Serial Number	20
Firmware Version	0x193		Name Of Person Testing	S. Holm
Ident Register	0x502		Board passed Functional Tests	YES