DES 12 Channel Board - Functional Tests: CCD Acquisition Board Revision 1.0

Stage 1. Preparation of documentation and configuration settings - Table 1.

Board Part Number	32		Board Serial Number	0xDB8F75
Date Of Tests	May 2010		Name Of Person Testing	S. Holm
Suggested Filename To Save	CCDACQ_12Ch_REPORT_BOARD32.xl		Sequence number: Test	

Stage 3. Power plane short test - Table 2.

Supply Name	Short test to ground: Impedance to ground	Test Point	
+1.2VD	38.60	TP43	~50 ohms
+1.8VD	2M	TPB12	> 1K ohm
+2.5VD	17K	TPB11	> 1K ohm
+3.3VD	5k	D13	> 1K ohm
+5VD	19k	D14	> 1K ohm
+5VA	2M	C267	> 1K ohm
-5VA	2M	C270	> 1K ohm
+15VA	2M	C288	> 1K ohm
-15VA	38K	C282	> 1K ohm
-28VA	2M	C307	> 1K ohm

Stage 4. Firmware programming tests - Table 3.

JTAG Order	Designator	Device	Load File	Check Sum or User Code
1	U122	XCF08PFS48C PROM	CcdAcqFpgaV41.mcs	0014ef670
2	U114	Spartan3 XC3S2000 FPGA	ccdacqfpgav41.bit	5102801

Stage 5. Power Consumption - Table 4.

Supply Name	Power Supply Consumption: Measured Voltage at test point	Measured Current on power supply	Test Point	
+1.2VD	1.20	N/A	TP43	
+1.8VD	1.80	N/A	TPB12	
+2.5VD	2.51	N/A	TPB11	
+3.3VD	3.29	0.112	D13	
+5VD	5.20	0.155	D14	
+5VA	4.98	0.667	C267	
-5VA	-4.89	0.433	C270	
+15VA	15.13	0.556	C288	
-15VA	-15.08	0.408	C282	
-28VA	-27.95	0.219	C307	
Vref 0+	10.03	N/A	R534	Vsub+ Reference(+10v)
Vref 0-	-2.50	N/A	R525	Vsub - Reference(-2.5v)
Vref Offset	2.50	N/A	R573	ADC Offset Reference(+2.5v)
Vclamp	1.87	N/A	VIA	ADC Clamp Voltage(+1.8v)
ADC Ref.	2.50	N/A	VIA	ADC Reference Voltage(+2.5v)
Vref 1+	2.50	N/A	R537	Vru and Vrl + Reference(+2.5v)
Vref 1-	-10.03	N/A	R535	Vru and Vrl - Reference(-10v)
Vref 2+	4.99	N/A	R563	Vog + Reference(+5v)
Vref 2-	-2.50	N/A	R555	Vog - Reference(-2.5v)
Vref 3+	2.50	N/A	R543	Vdd + Reference(+2.5v)
Vref 3-	10.07	N/A	R571	Vdd - Reference(-10v)

Power Dissipation:
27.3 Watts

~27 watts +/- 5%

Stage 7. Basic Bus Transactions - **D**igital **Register** Tests - Table 5.

Register name	Put an X on any bit that has an error: 31-24	23-16	15-08	07-00	Function	Test name: Pattern	Walking 0's	Walking 1's
CDS Control			00000000	00000000	16 bit R/W			
Digital Output	00000000	00000000	00000000	00000000	32 bit R/W			
ADC Config.			0000	00000000	12 bit R/W			
Offset DAC			0000	00000000	12 bit R/W			
Bias DAC			0000	00000000	12 bit R/W			
Telemetry Config.				0000	4 bit R/W			
Auxilary Config.			00	00000000	10 bit R/W			
Redirect				0000	4 bit R/W			
Pixel Transfer				00000000	8 bit R/W			
Micro SEQ			00000000	00000000	16 bit R/W			
RAM Buffer			00000000	00000000	16 bit R/W			
LED Control				0000	4 bit R/W			
Control			00000000	00000000	16 bit R/W			
All Register Test	00000000	00000000	00000000	00000000	16 bit R/W	**Passed**	**Passed**	**Passed**

Stage 8. Bias Voltage settings and output enables testing - Table 8

DAC Value	410	Bias Voltage Test Data 2048	3686	50% rms Noise	10-90% Rise Time			
Signal	volts	volts	volts	uV	millisec.	Fanout Brd	Slope	Offset
Vru 0	-13.17	-5.65	1.87	<10	2	BIAS 3	217.82	3278.68
Vru 1	-13.17	-5.65	1.87	<10	2	BIAS 4	217.82	3278.68
Vru 2	-13.17	-5.65	1.87	<10	2	BIAS 5	217.82	3278.68
Vru 3	-13.17	-5.65	1.87	<10	2	BIAS 6	217.82	3278.68
Vru 4	-13.17	-5.65	1.87	<10	2	BIAS 7	217.82	3278.68
Vru 5	-13.17	-5.65	1.87	<10	2	BIAS 8	217.82	3278.68
Vru 6	-13.17	-5.65	1.87	NA	NA	BIAS 9	217.82	3278.68
Vru 7	-13.17	-5.65	1.87	NA	NA	BIAS 10	217.82	3278.68
Vrl 0	-13.17	-5.65	1.87	<10	2	BIAS 11	217.82	3278.68
Vrl 1	-13.17	-5.65	1.87	<10	2	BIAS 12	217.82	3278.68
Vrl 2	-13.17	-5.65	1.87	<10	2	BIAS 13	217.82	3278.68
Vrl 3	-13.17	-5.65	1.87	<10	2	BIAS 14	217.82	3278.68
Vrl 4	-13.17	-5.65	1.87	<10	2	BIAS 15	217.82	3278.68
Vrl 5	-13.17	-5.65	1.87	<10	2	BIAS 16	217.82	3278.68
Vrl 6	-13.17	-5.65	1.87	NA	NA	BIAS 17	217.82	3278.68
Vrl 7	-13.17	-5.65	1.87	NA	NA	BIAS 18	217.82	3278.68
Vog 0	-1.75	1.24	4.24	<10	2	BIAS 19	546.91	1368.01
Vog 1	-1.75	1.24	4.24	<10	2	BIAS 20	546.91	1368.01
Vog 2	-1.75	1.24	4.24	<10	2	BIAS 21	546.91	1368.01
Vog 3	-1.75	1.24	4.24	<10	2	BIAS 22	546.91	1368.01
Vog 4	-1.75	1.24	4.24	<10	2	BIAS 23	546.91	1368.01
Vog 5	-1.75	1.24	4.24	<10	2	BIAS 24	546.91	1368.01
Vog 6	-1.75	1.24	4.24	NA	NA	BIAS 25	546.91	1368.01
Vog 7	-1.75	1.24	4.24	NA	NA	BIAS 26	546.91	1368.01
Vdd 0	-22.21	-9.55	3.11	<10	20	BIAS 27	129.38	3283.62
Vdd 1	-22.14	-9.52	3.10	<10	20	BIAS 28	129.79	3283.64
Vdd 2	-22.14	-9.52	3.09	<10	20	BIAS 29	129.85	3284.56
Vdd 3	-22.17	-9.55	3.08	<10	20	BIAS 30	129.74	3286.61
Vdd 4	-22.11	-9.51	3.09	<10	20	BIAS 21	130.00	3284.30
Vdd 5	-22.12	-9.52	3.09	<10	20	BIAS 32	129.95	3284.68
Vdd 6	-22.13	-9.52	3.09	NA	NA	BIAS 33	129.90	3284.62
Vdd 7	-22.18	-9.54	3.10	NA	NA	BIAS 34	129.59	3284.28

Vru	Slope		Offset
Mean	217.82	Mean	3278.68
Stdev	0	Stdev	0
Average	217.81915	Average	3278.678191
	Dac #	Average voltage	
	0	-15.0	
	4095	3.8	

Vrl	Slope		Offset
Mean	217.82	Mean	3278.68
Stdev	0	Stdev	0
Average	217.81915	Average	3278.678191
	Dac #	Average voltage	
	0	-15.1	
	4095	3.8	

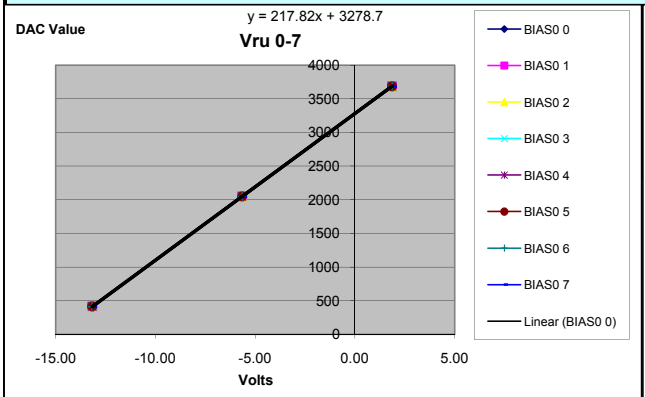
Vog	Slope		Offset
Mean	546.91	Mean	1368.01
Stdev	0	Stdev	2.27374E-13
Average	546.91101	Average	1368.00731
	Dac #	Average voltage	
	0	-2.5	
	4095	5.0	

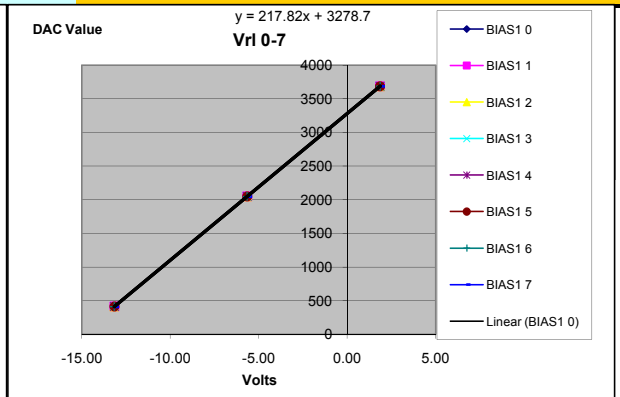
Vdd	Slope		Offset
Mean	129.77	Mean	3284.54
Stdev	0.1902779	Stdev	0.873181086
Average	129.77497	Average	3284.536841
	Dac #	Average voltage	
	0	-25.3	
	4095	6.3	

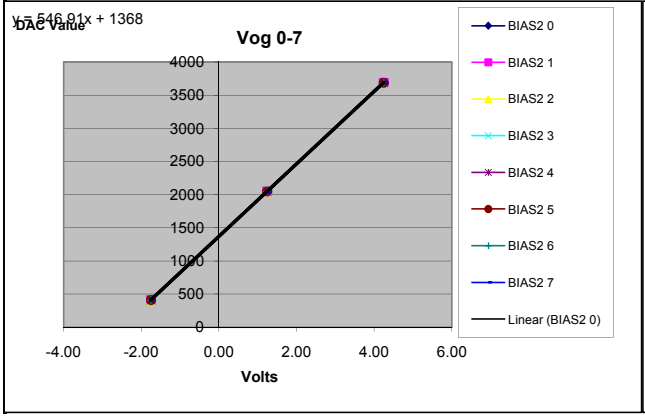
Notes and Observations

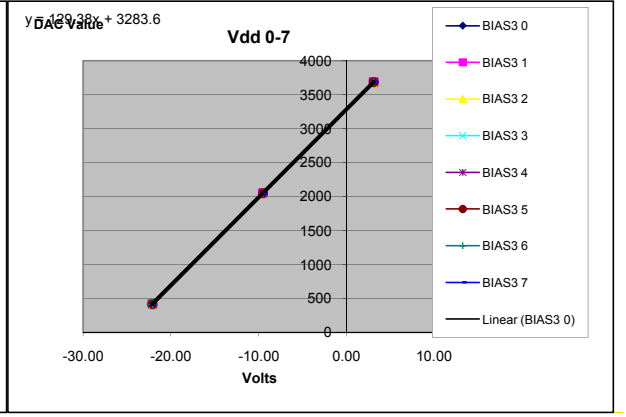
Checked for oscillations using a Agilent Oscilloscpe on AC.**OK**

average min & max voltages
(dac# -offset)/slope=voltage









Stage 8B. Telemetry System Tests - Table 7 (Bias Telemetry Tests)

DAC Value: 410 / 3686

Signal	Telemetry Return Values 10%	90%	Bias Signals Set Volts 10%	90%	Resolved Values for Telemetry Channel Slope	Offset
Vru 0	-1759	422	-13.17	1.87	145.0133	150.83
Vru 1	-1759	421	-13.17	1.87	144.9468	149.95
Vru 2	-1757	422	-13.17	1.87	144.8803	151.07
Vru 3	-1757	421	-13.17	1.87	144.8138	150.20
Vru 4	-1759	421	-13.17	1.87	144.9468	149.95
Vru 5	-1754	421	-13.17	1.87	144.6144	150.57
Vru 6	-1760	421	-13.17	1.87	145.0133	149.83
Vru 7	-1759	421	-13.17	1.87	144.9468	149.95
Vrl 0	-1755	422	-13.17	1.87	144.7473	151.32
Vrl 1	-1755	423	-13.17	1.87	144.8138	152.20
Vrl 2	-1755	423	-13.17	1.87	144.8138	152.20
Vrl 3	-1754	423	-13.17	1.87	144.7473	152.32
Vrl 4	-1752	423	-13.17	1.87	144.6144	152.57
Vrl 5	-1753	423	-13.17	1.87	144.6809	152.45
Vrl 6	-1754	423	-13.17	1.87	144.7473	152.32
Vrl 7	-1756	423	-13.17	1.87	144.8803	152.07
Vog 0	-361	865	-1.75	4.24	204.6745	-2.82
Vog 1	-362	864	-1.75	4.24	204.6745	-3.82
Vog 2	-362	865	-1.75	4.24	204.8414	-3.53
Vog 3	-362	864	-1.75	4.24	204.6745	-3.82
Vog 4	-362	865	-1.75	4.24	204.8414	-3.53
Vog 5	-362	865	-1.75	4.24	204.8414	-3.53
Vog 6	-362	865	-1.75	4.24	204.8414	-3.53
Vog 7	-362	865	-1.75	4.24	204.8414	-3.53
Vdd 0	-1760	574	-22.21	3.11	92.1801	287.32
Vdd 1	-1757	573	-22.14	3.10	92.3138	286.83
Vdd 2	-1756	573	-22.14	3.09	92.3107	287.76
Vdd 3	-1760	573	-22.17	3.08	92.3960	288.42
Vdd 4	-1754	572	-22.11	3.09	92.3016	286.79
Vdd 5	-1761	572	-22.12	3.09	92.5426	286.04
Vdd 6	-1757	573	-22.13	3.09	92.3870	287.52
Vdd 7	-1757	573	-22.18	3.10	92.1677	287.28

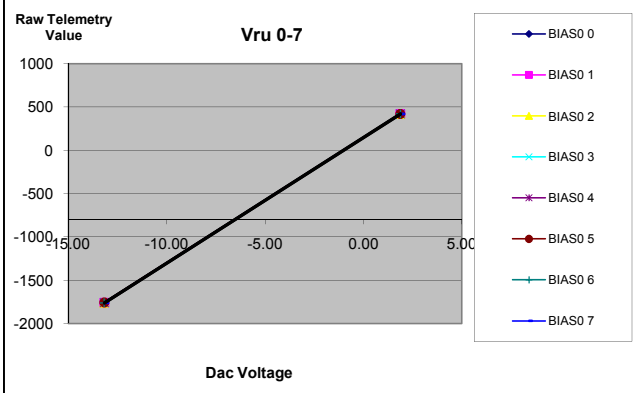
AVERAGE

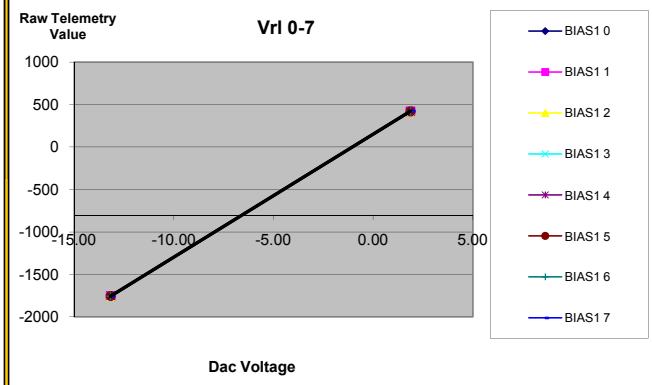
Vru	Slope		Offset
Mean	144.90	Mean	150.29
Stdev	0.1232746	Stdev	0.4404718

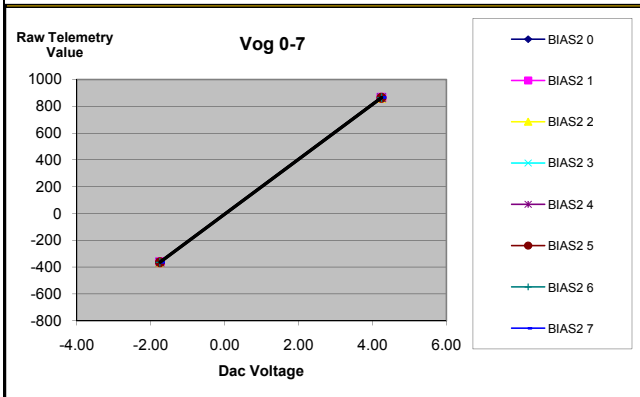
Vrl	Slope		Offset
Mean	144.76	Mean	152.18
Stdev	0.0775214	Stdev	0.3556746

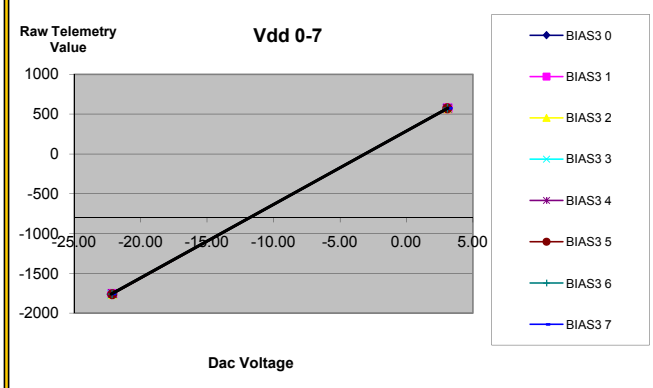
Vog	Slope		Offset
Mean	204.78	Mean	-3.51
Stdev	0.0808219	Stdev	0.2893627

Vdd	Slope		Offset
Mean	92.32	Mean	287.25
Stdev	0.1133959	Stdev	0.6669341









Stage 8C. Bias Voltage output enables testing - Table 8

Place a line through Bias Voltage name if enable/disable switch works

Vru 0	Vru 1	Vru 2	Vru 3	Vru 4	Vru 5
Vrl 0	Vrl 1	Vrl 2	Vrl 3	Vrl 4	Vrl 5
Vog 0	Vog 1	Vog 2	Vog 3	Vog 4	Vog 5
Vdd 0	Vdd 1	Vdd 2	Vdd 3	Vdd 4	Vdd 5

Stage 9. Vsub and Heater Control testing - Table 9

DAC Value	Vsub Measured Voltage Test Data 10%	50%	90%
Signal	volts	volts	volts
Vsub - rate	-1.25	3.76	8.77
Vsub - Limit	-1.25	3.76	8.77
Vsub0	0.00	0.00	0.00
	Vsub Enable Bit - pass		

DAC Value	Telemetery Readback Test Data 10%	50%	90%
Signal	dec	dec	dec
Vbias 0	150	216	466
Vbias 1	-30	696	1422
RTD1	220	NA	NA
RTD2	249	NA	NA
RTD3	275	NA	NA
RTD4	302	NA	NA
RTD5	325	NA	NA
RTD6	353	NA	NA
Reference 4096	836	NA	NA
eference buffere	836	NA	NA

Stage 10. Video Offset DAC Tests - Table 10.

	DAC Value 410				DAC Value 2048				DAC Value 3686			
ADC	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU
0	0.250	NA	NA	17046	1.250		NA	81068	2.250	NA	500ms	145091
1	0.250	NA	NA	17105	1.250		NA	81111	2.250	NA	500ms	145118
2	0.250	NA	NA	16825	1.250		NA	80916	2.250	NA	500ms	145012
3	0.250	NA	NA	17158	1.250		NA	81174	2.250	NA	500ms	145186
4	0.250	NA	NA	16823	1.250		NA	80955	2.250	NA	500ms	145092
5	0.250	NA	NA	17053	1.250		NA	81108	2.250	NA	500ms	145166
6	0.250	NA	NA	17033	1.250		NA	81130	2.250	NA	500ms	145235
7	0.250	NA	NA	17030	1.250		NA	81078	2.250	NA	500ms	145117
8	0.250	NA	NA	17271	1.250		NA	81335	2.250	NA	500ms	145384
9	0.250	NA	NA	16969	1.250		NA	80974	2.250	NA	500ms	144975
10	0.250	NA	NA	17234	1.250		NA	81259	2.250	NA	500ms	145290
11	0.250	NA	NA	17032	1.250		NA	81134	2.250	NA	500ms	145234

ADC	DC Volts		Data Set		
Channel	Slope	Offset	410	2048	3686
0	1638.000	0.500	0.250	1.250	2.250
1	1638.000	0.500	0.250	1.250	2.250
2	1638.000	0.500	0.250	1.250	2.250
3	1638.000	0.500	0.250	1.250	2.250
4	1638.000	0.500	0.250	1.250	2.250
5	1638.000	0.500	0.250	1.250	2.250
6	1638.000	0.500	0.250	1.250	2.250
7	1638.000	0.500	0.250	1.250	2.250
8	1638.000	0.500	0.250	1.250	2.250
9	1638.000	0.500	0.250	1.250	2.250
10	1638.000	0.500	0.250	1.250	2.250
11	1638.000	0.500	0.250	1.250	2.250

(dac# -offset)/slope=Voltage

ADC	ADU's		Data Set		
Channel	Slope	Offset	410	2048	3686
0	0.026	-26.11	17046	81068	145091
1	0.026	-27.73	17105	81111	145118
2	0.026	-19.97	16825	80916	145012
3	0.026	-29.06	17158	81174	145186
4	0.026	-19.64	16823	80955	145092
5	0.026	-26.05	17053	81108	145166
6	0.026	-25.22	17033	81130	145235
7	0.026	-25.60	17030	81078	145117
8	0.026	-31.70	17271	81335	145384
9	0.026	-24.30	16969	80974	144975
10	0.026	-30.86	17234	81259	145290
11	0.026	-25.23	17032	81134	145234

(dac# -offset)/slope=ADU

Notes and Observations

Checked for oscillations using a Agilent Oscilloscope on AC. OK

Stage 11. CDS Control Functions and Video Channel Performanc

TEST #1: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit is held static. The purpose of this test is to verify the correct operation of the ADC devices and measure the noise of the Offset voltage generators, ADC buffer amplifiers and ADC devices

Noise Test 1

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	81061	81076	81069.1	2.3093
CH 1	81103	81118	81110.2	2.34892
CH 2	80908	80926	80918	2.28906
CH 3	81163	81179	81171.5	2.26909
CH 4	80948	80962	80955.3	2.20773
CH 5	81102	81119	81110.4	2.22734
CH 6	81126	81143	81134.8	2.36092
CH 7	81071	81088	81078.6	2.27795
CH 8	81322	81338	81330.7	2.29249
CH 9	80965	80983	80973.9	2.32706
CH 10	81251	81270	81260.9	2.34021
CH 11	81125	81142	81133.1	2.42937

TEST #2: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the invert/non-invert and the DC Restore switches are held static.

Noise Test 2

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76319	76337	76327.5	2.69558
CH 1	76817	76838	76828.5	2.85413
CH 2	76016	76038	76025.6	2.85958
CH 3	76852	76875	76863.3	2.86018
CH 4	76121	76139	76129.7	2.58876
CH 5	76926	76947	76936.7	2.87493
CH 6	76791	76813	76800.8	2.76347
CH 7	76711	76731	76720.5	2.73674
CH 8	76960	76981	76971.5	2.78192
CH 9	76791	76811	76801.6	2.9874
CH 10	76614	76633	76624.1	2.7863
CH 11	76771	76791	76780.6	2.80749

TEST #3: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the DC Restore switch is held static.

Noise Test 3

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76314	76335	76323.2	2.88964
CH 1	76812	76834	76822.4	3.09932
CH 2	76006	76031	76017.9	3.08098
CH 3	76832	76854	76843.3	3.04808
CH 4	76115	76136	76125.7	2.90623
CH 5	76930	76953	76941.4	3.10965
CH 6	76786	76806	76795.8	3.00622
CH 7	76689	76712	76700.6	3.07621
CH 8	76956	76977	76966	3.04724
CH 9	76789	76815	76801.7	3.18757
CH 10	76610	76632	76620.1	3.03478
CH 11	76773	76793	76783.6	3.04176

TEST #4: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition.

Noise Test 4

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76305	76326	76315.5	3.13601
CH 1	76810	76837	76826.2	3.16773
CH 2	76008	76034	76021.4	3.09763
CH 3	76834	76855	76844.1	3.1878
CH 4	76152	76175	76163.3	3.08956
CH 5	76919	76942	76930.3	3.05648
CH 6	76791	76815	76801.7	3.18465
CH 7	76659	76682	76670.3	3.11948
CH 8	76996	77019	77007.7	3.09654
CH 9	76709	76733	76721.1	3.21033
CH 10	76627	76650	76639.3	3.16815
CH 11	76735	76757	76744.9	3.19025

TEST #5: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the circuitry set to high GAIN.

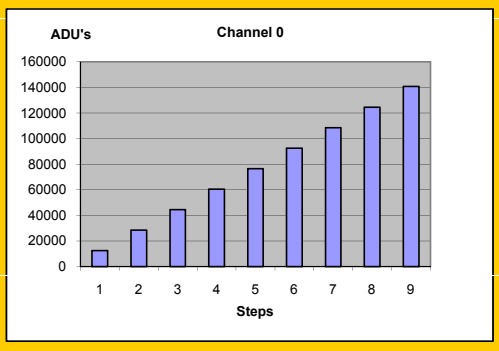
Noise Test 5

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76312	76341	76325.9	3.57381
CH 1	76825	76850	76838.2	3.51739
CH 2	76025	76052	76038.1	3.59617
CH 3	76836	76865	76849.8	3.58383
CH 4	76154	76180	76167.2	3.62438
CH 5	76916	76942	76929.1	3.56356
CH 6	76789	76815	76803.2	3.69814
CH 7	76658	76684	76670.7	3.69511
CH 8	77046	77073	77058.9	3.75235
CH 9	76706	76735	76720.9	3.81523
CH 10	76689	76715	76702	3.76019
CH 11	76731	76757	76744.1	3.65532

TEST #6A: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

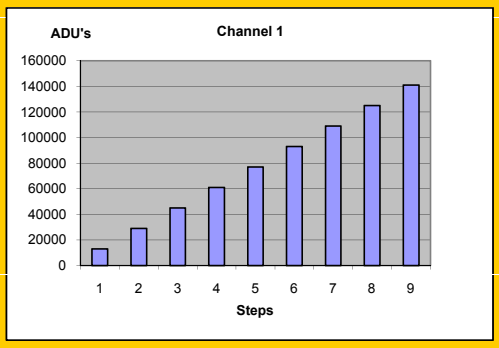
BrdTst6_006 / Channel 0					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12588	12611	12599.1	3.10793	10%
0x333	28572	28594	28583.2	3.1315	20%
0x4cc	44559	44580	44569.4	3.07396	30%
0x666	60580	60604	60592.9	3.10206	40%
0x800	76606	76628	76616.7	3.06559	50%
0x999	92592	92613	92602.5	3.10045	60%
0xb33	108615	108639	108627	3.22588	70%
0xccc	124604	124626	124615	3.16369	80%
0xe66	140630	140650	140641	3.03982	90%



TEST #6B: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

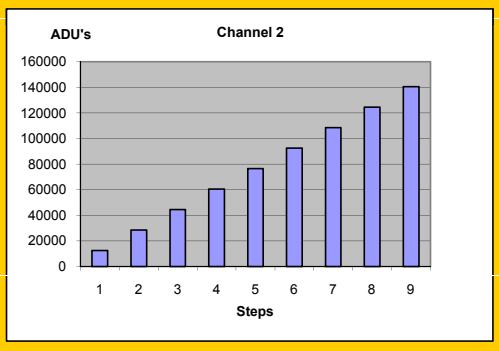
BrdTst6_006 / Channel 1					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13051	13075	13062.1	3.30804	10%
0x333	29032	29056	29042.4	3.08021	20%
0x4cc	45014	45038	45025.4	3.07015	30%
0x666	61033	61059	61045.7	3.24579	40%
0x800	77055	77079	77065.9	3.22272	50%
0x999	93039	93061	93050	3.22161	60%
0xb33	109059	109080	109070	3.13103	70%
0xccc	125044	125067	125055	3.18762	80%
0xe66	141064	141086	141076	3.02658	90%



TEST #6C: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

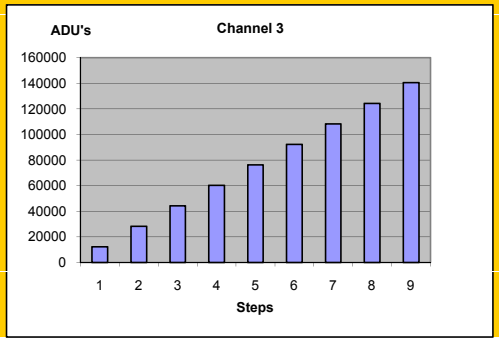
BrdTst6_006 / Channel 2					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12483	12504	12493.4	3.16046	10%
0x333	28466	28488	28477.2	3.14231	20%
0x4cc	44450	44472	44461.3	3.1509	30%
0x666	60472	60495	60484.1	3.21353	40%
0x800	76495	76516	76506	3.1417	50%
0x999	92481	92504	92492.8	3.1397	60%
0xb33	108506	108526	108516	3.16548	70%
0xccc	124494	124516	124504	3.12263	80%
0xe66	140515	140539	140528	3.07128	90%



TEST #6D: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

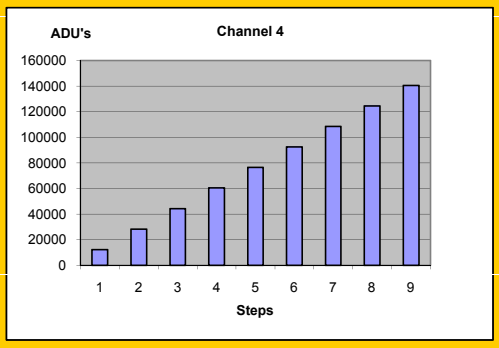
BrdTst6_006 / Channel 3					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12218	12240	12229.3	3.30434	10%
0x333	28220	28243	28230.5	3.09749	20%
0x4cc	44227	44251	44238.2	3.15287	30%
0x666	60267	60289	60278.3	3.20986	40%
0x800	76304	76327	76315.6	3.18008	50%
0x999	92308	92331	92319	3.13504	60%
0xb33	108348	108371	108360	3.19457	70%
0xccc	124358	124381	124369	3.15161	80%
0xe66	140396	140423	140411	3.2565	90%



TEST #6E: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

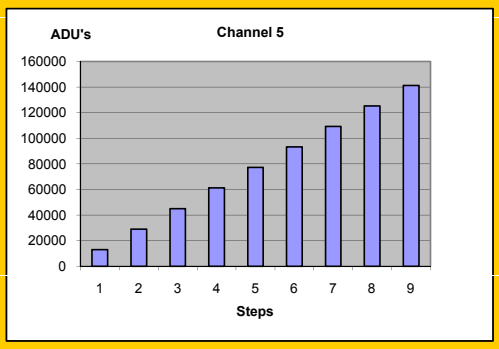
BrdTst6_006 / Channel 4					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12320	12342	12331.7	3.1246	10%
0x333	28335	28358	28346.3	3.14263	20%
0x4cc	44345	44372	44357.3	3.16302	30%
0x666	60401	60426	60411.9	3.03881	40%
0x800	76456	76477	76465.9	2.98519	50%
0x999	92468	92489	92478.4	3.14249	60%
0xb33	108521	108543	108532	2.90992	70%
0xccc	124536	124558	124546	3.09415	80%
0xe66	140588	140610	140599	3.13518	90%



TEST #6F: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

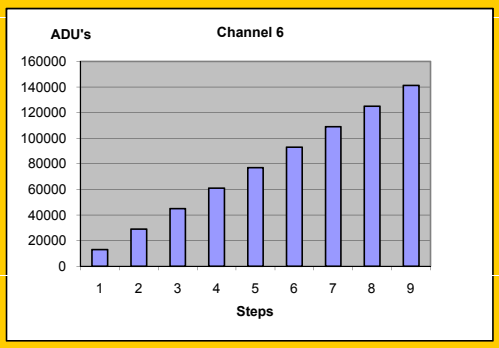
BrdTst6_006 / Channel 5					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13117	13140	13128.4	3.12288	10%
0x333	29110	29136	29122.1	3.14238	20%
0x4cc	45104	45124	45114.9	3.1791	30%
0x666	61138	61162	61148.8	3.1275	40%
0x800	77168	77192	77180.2	3.19379	50%
0x999	93166	93189	93177.3	3.16182	60%
0xb33	109198	109220	109210	3.0755	70%
0xccc	125190	125216	125205	3.13668	80%
0xe66	141226	141250	141238	3.07355	90%



TEST #6G: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

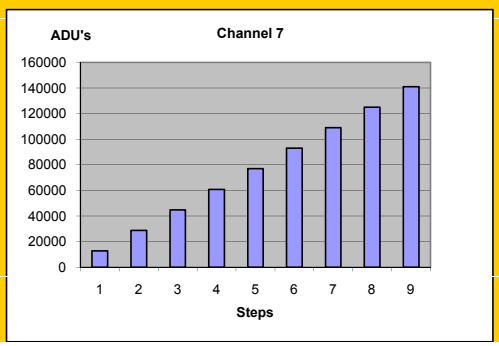
BrdTst6_006 / Channel 6					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12939	12963	12950.4	3.16474	10%
0x333	28941	28966	28954.5	3.17158	20%
0x4cc	44948	44971	44959.6	3.06215	30%
0x666	60992	61012	61002.2	3.12153	40%
0x800	77033	77057	77044.3	2.96407	50%
0x999	93039	93061	93049.9	3.08603	60%
0xb33	109082	109104	109093	3.15214	70%
0xccc	125088	125109	125099	3.11592	80%
0xe66	141131	141153	141143	3.08709	90%



TEST #6H: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

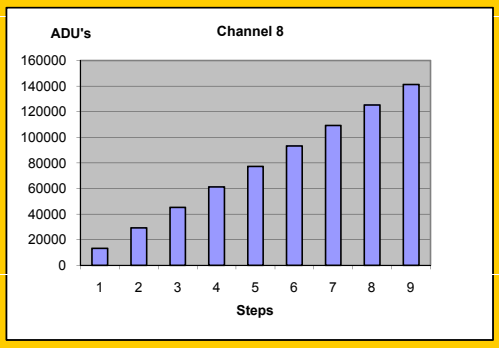
BrdTst6_006 / Channel 7					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12849	12871	12859.9	3.20678	10%
0x333	28840	28863	28850.7	3.09065	20%
0x4cc	44830	44852	44841.6	3.16837	30%
0x666	60860	60884	60872.3	3.19298	40%
0x800	76883	76914	76898.5	3.25532	50%
0x999	92876	92901	92888.7	3.17032	60%
0xb33	108908	108930	108919	3.13609	70%
0xccc	124899	124922	124911	3.16815	80%
0xe66	140930	140953	140942	3.16684	90%



TEST #6I: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

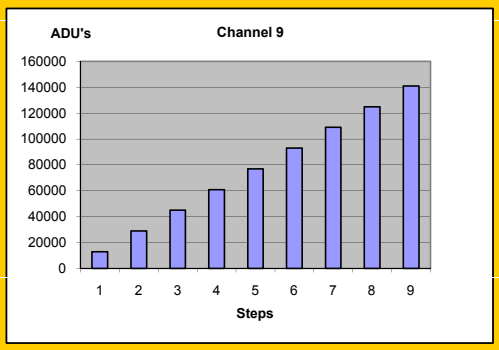
BrdTst6_006 / Channel 8					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13201	13228	13215.8	3.12969	10%
0x333	29203	29223	29211.9	3.13888	20%
0x4cc	45192	45214	45202.6	3.00708	30%
0x666	61226	61248	61237	3.10412	40%
0x800	77260	77282	77270.1	3.08793	50%
0x999	93257	93280	93267.5	3.14605	60%
0xb33	109292	109316	109303	3.1383	70%
0xccc	125282	125306	125295	3.16032	80%
0xe66	141321	141344	141332	3.03088	90%



TEST #6J: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

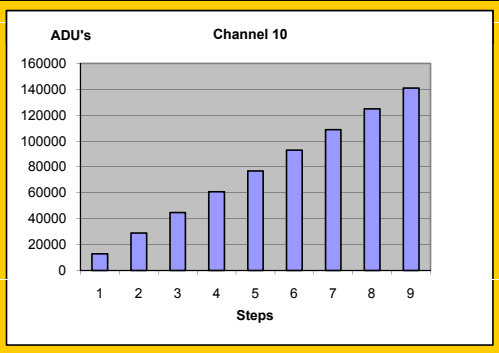
BrdTst6_006 / Channel 9					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12967	12994	12980.8	3.32158	10%
0x333	28948	28971	28960.3	3.03037	20%
0x4cc	44928	44952	44939.7	3.20783	30%
0x666	60949	60974	60960.5	3.11385	40%
0x800	76969	76992	76980.8	3.12817	50%
0x999	92955	92977	92965.2	3.09679	60%
0xb33	108975	108996	108985	3.17063	70%
0xccc	124953	124976	124965	2.92988	80%
0xe66	140973	140996	140985	3.27628	90%



TEST #6K: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

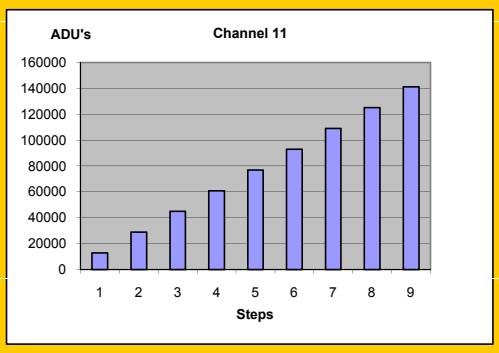
BrdTst6_006 / Channel 10					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12877	12898	12887.9	3.30208	10%
0x333	28867	28890	28878	3.16699	20%
0x4cc	44850	44874	44861.7	3.18522	30%
0x666	60878	60901	60889.8	3.22314	40%
0x800	76904	76925	76914.7	3.08492	50%
0x999	92893	92914	92903.9	3.16596	60%
0xb33	108922	108944	108933	3.10487	70%
0xccc	124910	124931	124920	3.14533	80%
0xe66	140938	140961	140950	3.24689	90%



TEST #6L: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

BrdTst6_006 / Channel 11					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12897	12920	12908	3.23364	10%
0x333	28902	28926	28913.9	3.20193	20%
0x4cc	44908	44931	44919.2	3.22489	30%
0x666	60953	60978	60965.4	3.02425	40%
0x800	76995	77017	77005.9	3.1738	50%
0x999	93000	93023	93011.8	3.26749	60%
0xb33	109046	109068	109056	3.30399	70%
0xccc	125053	125075	125064	3.14426	80%
0xe66	141099	141122	141110	3.15733	90%



Stage 13. Other Bit Tests. Table 11

Electronic Serial Number	0xDB8F75		Board Serial Number	32
Firmware Version	0x193		Name Of Person Testing	S. Holm
Ident Register	0x502		Board passed Functional Tests	YES