DES 12 Channel Board - Functional Tests: CCD Acquisition Board Revision 1.0

Stage 1. Preparation of documentation and configuration settings - Table 1.

Board Part Number	28		Board Serial Number	0xDB6F97BD
Date Of Tests	July 2010		Name Of Person Testing	S. Holm
Suggested Filename To Save	CCDACQ_12Ch_REPORT_BOARD6.xls		Sequence number: Test	

Stage 3. Power plane short test - Table 2.

Supply Name	Short test to ground: Impedance to ground	Test Point	
+1.2VD	49.60	TP43	~50 ohms
+1.8VD	2.5M	TPB12	> 1K ohm
+2.5VD	19k	TPB11	> 1K ohm
+3.3VD	6k	D13	> 1K ohm
+5VD	19k	D14	> 1K ohm
+5VA	4M	C267	> 1K ohm
-5VA	280k	C270	> 1K ohm
+15VA	400k	C288	> 1K ohm
-15VA	400k	C282	> 1K ohm
-28VA	2.6M	C307	> 1K ohm

Stage 4. Firmware programming tests - Table 3.

JTAG Order	Designator	Device	Load File	Check Sum or User Code
1	U122	XCF08PFS48C PROM	CcdAcqFpgaV41.mcs	0014ef670
2	U114	Spartan3 XC3S2000 FPGA	ccdacqfpgav41.bit	5102801

Stage 5. Power Consumption - Table 4.

Supply Name	Power Supply Consumption: Measured Voltage at test point	Measured Current on power supply	Test Point	
+1.2VD	1.19	N/A	TP43	
+1.8VD	1.80	N/A	TPB12	
+2.5VD	2.50	N/A	TPB11	
+3.3VD	3.28	0.228	D13	
+5VD	5.20	0.166	D14	
+5VA	5.05	0.628	C267	
-5VA	-4.97	0.434	C270	
+15VA	15.06	0.556	C288	
-15VA	-15.08	0.407	C282	
-28VA	-27.42	0.207	C307	
Vref 0+	10.05	N/A	R534	Vsub+ Reference(+10v)
Vref 0-	-2.52	N/A	R525	Vsub - Reference(-2.5v)
Vref Offset	2.50	N/A	R573	ADC Offset Reference(+2.5v)
Vclamp	1.87	N/A	VIA	ADC Clamp Voltage(+1.8v)
ADC Ref.	2.50	N/A	VIA	ADC Reference Voltage(+2.5v)
Vref 1+	2.50	N/A	R537	Vru and Vrl + Reference(+2.5v)
Vref 1-	-10.02	N/A	R535	Vru and Vrl - Reference(-10v)
Vref 2+	5.01	N/A	R563	Vog + Reference(+5v)
Vref 2-	-2.52	N/A	R555	Vog - Reference(-2.5v)
Vref 3+	2.50	N/A	R543	Vdd + Reference(+2.5v)
Vref 3-	-10.14	N/A	R571	Vdd - Reference(-10v)

Power Dissipation:
27.1 Watts

~27 watts +/- 5%

Stage 7. Basic Bus Transactions - **D**igital **Register** Tests - Table 5.

Register name	Put an X on any bit that has an error: 31-24 23-16 15-08 07-00	Function	Test name: Pattern	Walking 0's	Walking 1's
CDS Control	00000000 00000000	16 bit R/W			
Digital Output	00000000 00000000 00000000 00000000	32 bit R/W			
ADC Config.	0000 00000000	12 bit R/W			
Offset DAC	0000 00000000	12 bit R/W			
Bias DAC	0000 00000000	12 bit R/W			
Telemetry Config.	0000	4 bit R/W			
Auxilary Config.	00 00000000	10 bit R/W			
Redirect	0000	4 bit R/W			
Pixel Transfer	00000000	8 bit R/W			
Micro SEQ	00000000 00000000	16 bit R/W			
RAM Buffer	00000000 00000000	16 bit R/W			
LED Control	0000	4 bit R/W			
Control	00000000 00000000	16 bit R/W			
All Register Test	00000000 00000000 00000000 00000000	16 bit R/W	**Passed**	**Passed**	**Passed**

Stage 8. Bias Voltage settings and output enables testing - Table 8

DAC Value	Bias Voltage Test Data 410	2048	3686	50% rms Noise	10-90% Rise Time			
Signal	volts	volts	volts	uV	millisec.	Fanout Brd	Slope	Offset
Vru 0	-13.30	-5.72	1.86	<10	1	BIAS 3	216.09	3284.06
Vru 1	-13.30	-5.72	1.86	<10	1	BIAS 4	216.09	3284.06
Vru 2	-13.29	-5.72	1.86	<10	1	BIAS 5	216.24	3284.16
Vru 3	-13.30	-5.72	1.86	<10	1	BIAS 6	216.09	3284.06
Vru 4	-13.28	-5.72	1.86	<10	1	BIAS 7	216.38	3284.25
Vru 5	-13.30	-5.72	1.86	<10	1	BIAS 8	216.09	3284.06
Vru 6	-13.30	-5.72	1.86	NA	NA	BIAS 9	216.09	3284.06
Vru 7	-13.27	-5.72	1.86	NA	NA	BIAS 10	216.52	3284.35
Vrl 0	-13.29	-5.72	1.86	<10	1	BIAS 11	216.24	3284.16
Vrl 1	-13.29	-5.72	1.86	<10	1	BIAS 12	216.24	3284.16
Vrl 2	-13.29	-5.72	1.86	<10	1	BIAS 13	216.24	3284.16
Vrl 3	-13.28	-5.72	1.86	<10	1	BIAS 14	216.38	3284.25
Vrl 4	-13.30	-5.72	1.86	<10	1	BIAS 15	216.09	3284.06
Vrl 5	-13.30	-5.72	1.86	<10	1	BIAS 16	216.09	3284.06
Vrl 6	-13.29	-5.72	1.86	NA	NA	BIAS 17	216.24	3284.16
Vrl 7	-13.27	-5.72	1.86	NA	NA	BIAS 18	216.52	3284.35
Vog 0	-1.76	1.24	4.26	<10	1	BIAS 19	544.18	1369.58
Vog 1	-1.76	1.24	4.26	<10	1	BIAS 20	544.18	1369.58
Vog 2	-1.76	1.24	4.26	<10	1	BIAS 21	544.18	1369.58
Vog 3	-1.76	1.24	4.26	<10	1	BIAS 22	544.18	1369.58
Vog 4	-1.76	1.24	4.26	<10	1	BIAS 23	544.18	1369.58
Vog 5	-1.76	1.24	4.26	<10	1	BIAS 24	544.18	1369.58
Vog 6	-1.76	1.24	4.26	NA	NA	BIAS 25	544.18	1369.58
Vog 7	-1.76	1.24	4.26	NA	NA	BIAS 26	544.18	1369.58
Vdd 0	-22.16	-9.54	3.08	<10	20	BIAS 27	129.79	3286.23
Vdd 1	-22.24	-9.58	3.09	<10	20	BIAS 28	129.33	3286.58
Vdd 2	-22.19	-9.55	3.08	<10	20	BIAS 29	129.64	3286.49
Vdd 3	-22.23	-9.57	3.09	<10	20	BIAS 30	129.38	3286.20
Vdd 4	-22.18	-9.55	3.08	<10	20	BIAS 21	129.69	3286.55
Vdd 5	-22.27	-9.59	3.10	<10	20	BIAS 32	129.13	3285.92
Vdd 6	-22.25	-9.58	3.09	NA	NA	BIAS 33	129.28	3286.52
Vdd 7	-22.16	-9.54	3.08	NA	NA	BIAS 34	129.79	3286.23

Vru	Slope		Offset
Mean	216.20	Mean	3284.13
Stdev	0.1555158	Stdev	0.103212291
Average	216.202	Average	3284.134391
	Dac #	Average voltage	
	0	-15.0	
	4095	3.8	

Vrl	Slope		Offset
Mean	216.26	Mean	3284.17
Stdev	0.1323088	Stdev	0.087779849
Average	216.25548	Average	3284.169983
	Dac #	Average voltage	
	0	-15.2	
	4095	3.8	

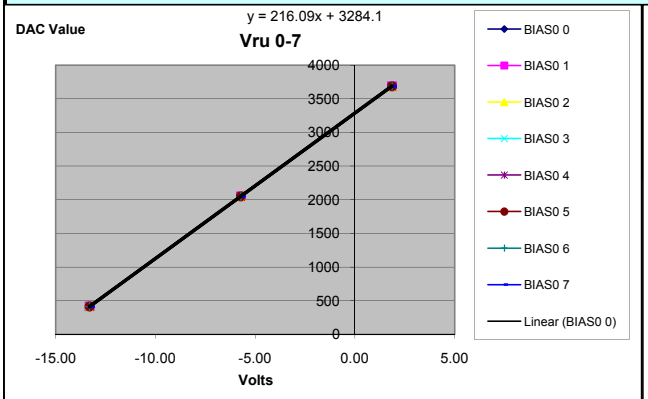
Vog	Slope		Offset
Mean	544.18	Mean	1369.58
Stdev	1.137E-13	Stdev	0
Average	544.18404	Average	1369.583891
	Dac #	Average voltage	
	0	-2.5	
	4095	5.0	

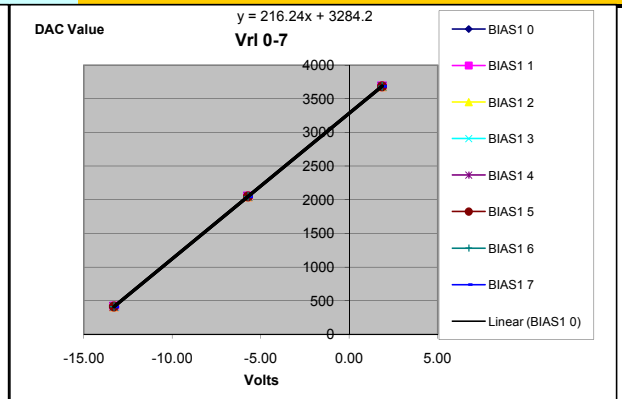
Vdd	Slope		Offset
Mean	129.51	Mean	3286.34
Stdev	0.2386145	Stdev	0.217157712
Average	129.5058	Average	3286.341126
	Dac #	Average voltage	
	0	-25.4	
	4095	6.3	

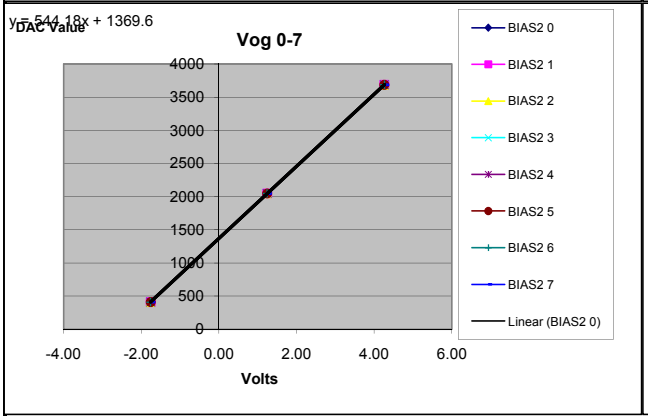
Notes and Observations

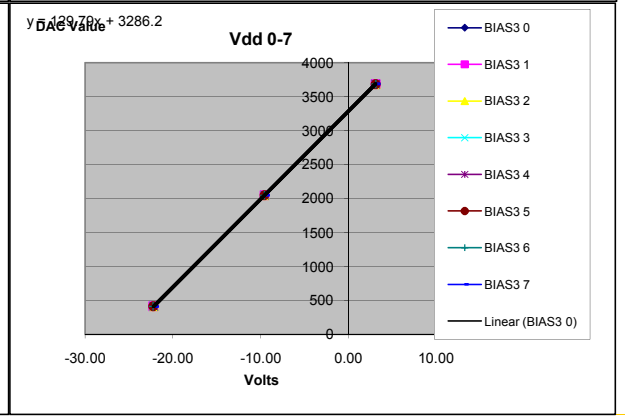
Checked for oscillations using a Agilent Oscilloscpe on AC.**OK**

average min & max voltages
(dac# -offset)/slope=voltage









Stage 8B. Telemetry System Tests - Table 7 (Bias Telemetry Tests)

DAC Value	410	3686	Bias Signals		Resolved Values for	
	Telemetry Return Values		Set Volts		Telemetry Channel	
Signal	10%	90%	10%	90%	Slope	Offset
Vru 0	-1756	421	-13.30	1.86	143.6016	153.90
Vru 1	-1758	421	-13.30	1.86	143.7335	153.66
Vru 2	-1760	421	-13.29	1.86	143.9604	153.23
Vru 3	-1756	421	-13.30	1.86	143.6016	153.90
Vru 4	-1756	421	-13.28	1.86	143.7913	153.55
Vru 5	-1755	421	-13.30	1.86	143.5356	154.02
Vru 6	-1761	420	-13.30	1.86	143.8654	152.41
Vru 7	-1758	420	-13.27	1.86	143.9524	152.25
Vrl 0	-1752	421	-13.29	1.86	143.4323	154.22
Vrl 1	-1753	422	-13.29	1.86	143.5644	154.97
Vrl 2	-1747	421	-13.29	1.86	143.1023	154.83
Vrl 3	-1750	421	-13.28	1.86	143.3950	154.29
Vrl 4	-1750	421	-13.30	1.86	143.2058	154.64
Vrl 5	-1752	421	-13.30	1.86	143.3377	154.39
Vrl 6	-1755	421	-13.29	1.86	143.6304	153.85
Vrl 7	-1748	421	-13.27	1.86	143.3576	154.35
Vog 0	-366	869	-1.76	4.26	205.1495	-4.94
Vog 1	-365	869	-1.76	4.26	204.9834	-4.23
Vog 2	-366	870	-1.76	4.26	205.3156	-4.64
Vog 3	-365	869	-1.76	4.26	204.9834	-4.23
Vog 4	-365	870	-1.76	4.26	205.1495	-3.94
Vog 5	-365	870	-1.76	4.26	205.1495	-3.94
Vog 6	-365	870	-1.76	4.26	205.1495	-3.94
Vog 7	-366	869	-1.76	4.26	205.1495	-4.94
Vdd 0	-1759	571	-22.16	3.08	92.3138	286.67
Vdd 1	-1754	571	-22.24	3.09	91.7884	287.37
Vdd 2	-1741	571	-22.19	3.08	91.4919	289.20
Vdd 3	-1745	571	-22.23	3.09	91.4692	288.36
Vdd 4	-1730	571	-22.18	3.08	91.0926	290.43
Vdd 5	-1741	572	-22.27	3.10	91.1707	289.37
Vdd 6	-1733	571	-22.25	3.09	90.9234	290.05
Vdd 7	-1725	570	-22.16	3.08	90.9271	289.94

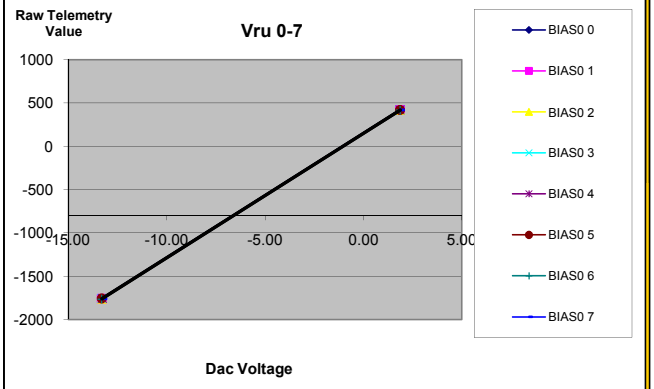
AVERAGE

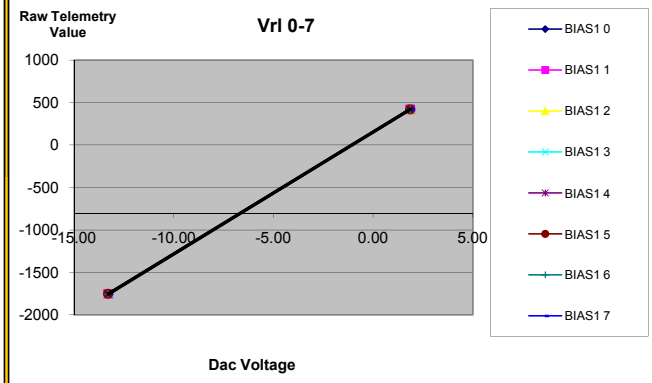
Vru	Slope		Offset
Mean	143.76	Mean	153.37
Stdev	0.1542457	Stdev	0.6424543

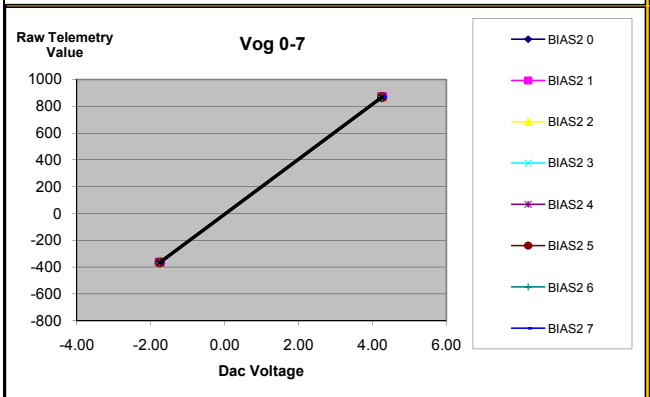
Vrl	Slope		Offset
Mean	143.38	Mean	154.44
Stdev	0.1617684	Stdev	0.3366575

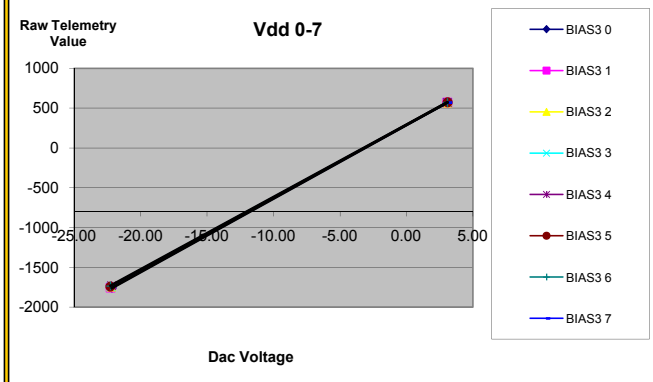
Vog	Slope		Offset
Mean	205.13	Mean	-4.35
Stdev	0.0995812	Stdev	0.4057016

Vdd	Slope		Offset
Mean	91.40	Mean	288.93
Stdev	0.4467701	Stdev	1.2573701









Stage 8C. Bias Voltage output enables testing - Table 8

Place a line through Bias Voltage name if enable/disable switch works

Vru 0	Vru 1	Vru 2	Vru 3	Vru 4	Vru 5
Vrl 0	Vrl 1	Vrl 2	Vrl 3	Vrl 4	Vrl 5
Vog 0	Vog 1	Vog 2	Vog 3	Vog 4	Vog 5
Vdd 0	Vdd 1	Vdd 2	Vdd 3	Vdd 4	Vdd 5

Stage 9. Vsub and Heater Control testing - Table 9

DAC Value	Vsub Measured Voltage Test Data 10%	50%	90%
Signal	volts	volts	volts
Vsub - rate	-1.26	3.76	8.78
Vsub - Limit	-1.26	3.76	8.78
Vsub0	0.00	0.00	0.00
	Vsub Enable Bit - pass		

DAC Value	Telemetery Readback Test Data 10%	50%	90%
Signal	dec	dec	dec
Vbias 0	155	268	454
Vbias 1	-31	696	1424
RTD1	219	NA	NA
RTD2	249	NA	NA
RTD3	273	NA	NA
RTD4	302	NA	NA
RTD5	325	NA	NA
RTD6	351	NA	NA
Reference 4096	836	NA	NA
eference buffere	836	NA	NA

Stage 10. Video Offset DAC Tests - Table 10.

	DAC Value 410				DAC Value 2048				DAC Value 3686			
ADC	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU
0	0.250	NA	NA	17216	1.250		NA	81249	2.250	NA	500ms	145272
1	0.250	NA	NA	17130	1.250		NA	81126	2.250	NA	500ms	145119
2	0.250	NA	NA	17215	1.250		NA	81240	2.250	NA	500ms	145258
3	0.250	NA	NA	16992	1.250		NA	81068	2.250	NA	500ms	145139
4	0.250	NA	NA	16997	1.250		NA	81044	2.250	NA	500ms	145080
5	0.250	NA	NA	16961	1.250		NA	81024	2.250	NA	500ms	145085
6	0.250	NA	NA	17179	1.250		NA	81197	2.250	NA	500ms	145209
7	0.250	NA	NA	16856	1.250		NA	80950	2.250	NA	500ms	145045
8	0.250	NA	NA	17132	1.250		NA	81213	2.250	NA	500ms	145281
9	0.250	NA	NA	17116	1.250		NA	81136	2.250	NA	500ms	145153
10	0.250	NA	NA	17160	1.250		NA	81208	2.250	NA	500ms	145240
11	0.250	NA	NA	17053	1.250		NA	81138	2.250	NA	500ms	145202

ADC	DC Volts		Data Set		
Channel	Slope	Offset	410	2048	3686
0	1638.000	0.500	0.250	1.250	2.250
1	1638.000	0.500	0.250	1.250	2.250
2	1638.000	0.500	0.250	1.250	2.250
3	1638.000	0.500	0.250	1.250	2.250
4	1638.000	0.500	0.250	1.250	2.250
5	1638.000	0.500	0.250	1.250	2.250
6	1638.000	0.500	0.250	1.250	2.250
7	1638.000	0.500	0.250	1.250	2.250
8	1638.000	0.500	0.250	1.250	2.250
9	1638.000	0.500	0.250	1.250	2.250
10	1638.000	0.500	0.250	1.250	2.250
11	1638.000	0.500	0.250	1.250	2.250

(dac# -offset)/slope=Voltage

ADC	ADU's		Data Set		
Channel	Slope	Offset	410	2048	3686
0	0.026	-30.47	17216	81249	145272
1	0.026	-28.47	17130	81126	145119
2	0.026	-30.48	17215	81240	145258
3	0.026	-24.41	16992	81068	145139
4	0.026	-24.78	16997	81044	145080
5	0.026	-23.68	16961	81024	145085
6	0.026	-29.60	17179	81197	145209
7	0.026	-20.77	16856	80950	145045
8	0.026	-28.02	17132	81213	145281
9	0.026	-27.95	17116	81136	145153
10	0.026	-28.98	17160	81208	145240
11	0.026	-26.03	17053	81138	145202

(dac# -offset)/slope=ADU

Notes and Observations

Checked for oscillations using a Agilent Oscilloscope on AC. OK

Stage 11. CDS Control Functions and Video Channel Performanc

TEST #1: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit is held static. The purpose of this test is to verify the correct operation of the ADC devices and measure the noise of the Offset voltage generators, ADC buffer amplifiers and ADC devices

Noise Test 1

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	81237	8.13E+04	81244.6	2.25715
CH 1	81119	8.11E+04	81126.1	2.38824
CH 2	81230	8.12E+04	81237	2.21938
CH 3	81059	8.11E+04	81067.9	2.3737
CH 4	81033	8.10E+04	81040.4	2.3064
CH 5	81012	8.10E+04	81021.1	2.26113
CH 6	81187	8.12E+04	81194.8	2.28857
CH 7	80941	8.10E+04	80950.2	2.39663
CH 8	81201	8.12E+04	81209	2.27227
CH 9	81123	8.11E+04	81131.3	2.40797
CH 10	81195	8.12E+04	81203.4	2.21504
CH 11	81127	8.11E+04	81135.1	2.39258

TEST #2: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the invert/non-invert and the DC Restore switches are held static.

Noise Test 2

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76465	7.65E+04	76473.9	2.85209
CH 1	76687	7.67E+04	76697	2.85148
CH 2	76654	7.67E+04	76664.1	2.9102
CH 3	76779	7.68E+04	76789	2.92191
CH 4	76409	7.64E+04	76419.3	2.85755
CH 5	76710	7.67E+04	76721.3	2.91678
CH 6	77115	7.71E+04	77125.4	2.72908
CH 7	76653	7.67E+04	76663.1	2.9317
CH 8	76697	7.67E+04	76707.5	2.73225
CH 9	76901	7.69E+04	76910.5	2.87548
CH 10	76666	7.67E+04	76676.9	2.91012
CH 11	76795	7.68E+04	76805.4	2.84016

TEST #3: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the DC Restore switch is held static.

Noise Test 3

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76462	7.65E+04	76472.8	3.03185
CH 1	76689	7.67E+04	76700	3.05582
CH 2	76649	7.67E+04	76660	3.11482
CH 3	76775	7.68E+04	76786.4	3.13684
CH 4	76411	7.64E+04	76421.6	3.03288
CH 5	76712	7.67E+04	76722.8	3.10294
CH 6	77111	7.71E+04	77120.7	2.94118
CH 7	76649	7.67E+04	76660.8	3.08084
CH 8	76700	7.67E+04	76710.6	2.98083
CH 9	76900	7.69E+04	76911.1	3.13471
CH 10	76667	7.67E+04	76677.1	3.15808
CH 11	76797	7.68E+04	76809.2	3.07493

TEST #4: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition.

Noise Test 4

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76455	7.65E+04	76466.3	3.12189
CH 1	76692	7.67E+04	76704.8	3.13201
CH 2	76654	7.67E+04	76667.3	3.25615
CH 3	76775	7.68E+04	76788.5	3.17465
CH 4	76453	7.65E+04	76463.6	3.21772
CH 5	76702	7.67E+04	76712.4	3.1984
CH 6	77118	7.71E+04	77129.5	3.13412
CH 7	76618	7.66E+04	76629.9	3.17845
CH 8	76748	7.68E+04	76758.8	3.1891
CH 9	76816	7.68E+04	76826.8	3.17894
CH 10	76686	7.67E+04	76699.2	3.2425
CH 11	76757	7.68E+04	76768.3	3.11707

TEST #5: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the circuitry set to high GAIN.

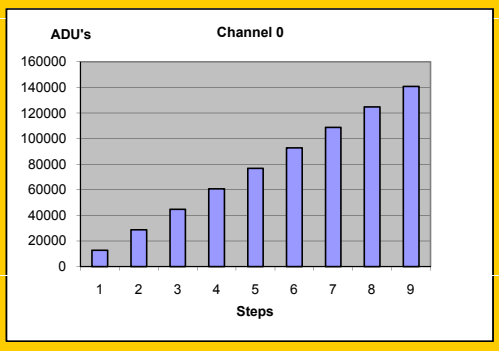
Noise Test 5

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76467	7.65E+04	76479.9	3.56467
CH 1	76709	7.67E+04	76721.7	3.56887
CH 2	76671	7.67E+04	76685.8	3.74699
CH 3	76782	7.68E+04	76794.3	3.7322
CH 4	76460	7.65E+04	76473.1	3.67345
CH 5	76702	7.67E+04	76715.7	3.70497
CH 6	77120	7.71E+04	77133.2	3.75733
CH 7	76620	7.66E+04	76633.3	3.76915
CH 8	76808	7.68E+04	76819.3	3.48306
CH 9	76814	7.68E+04	76829.8	3.62905
CH 10	76754	7.68E+04	76768.5	3.78301
CH 11	76759	7.68E+04	76770.7	3.59306

TEST #6A: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

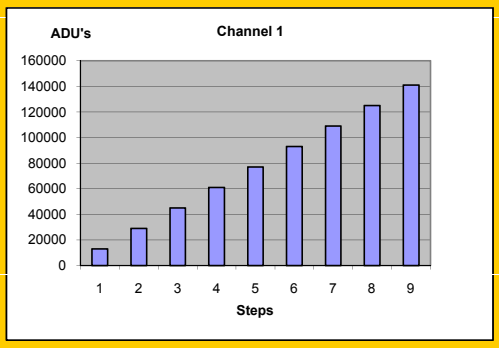
BrdTst6_006 / Channel 0					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12746	12771	12759.2	3.06654	10%
0x333	28732	28757	28745.1	3.11513	20%
0x4cc	44721	44744	44732.5	3.09845	30%
0x666	60746	60771	60758.5	3.21812	40%
0x800	76774	76796	76786.7	3.15124	50%
0x999	92766	92790	92777.5	3.15813	60%
0xb33	108788	108811	108800	3.1183	70%
0xccc	124794	124816	124806	3.24824	80%
0xe66	140823	140846	140834	3.23374	90%



TEST #6B: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

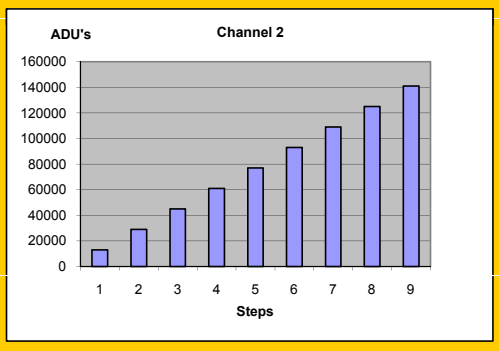
BrdTst6_006 / Channel 1					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12950	12974	12961.9	3.1434	10%
0x333	28928	28950	28938.4	3.16905	20%
0x4cc	44905	44929	44917.4	3.13819	30%
0x666	60923	60945	60933.8	3.15948	40%
0x800	76939	76960	76950.5	3.21255	50%
0x999	92919	92941	92930.3	3.00815	60%
0xb33	108934	108957	108945	3.14135	70%
0xccc	124922	124945	124935	3.1506	80%
0xe66	140940	140965	140952	3.20833	90%



TEST #6C: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

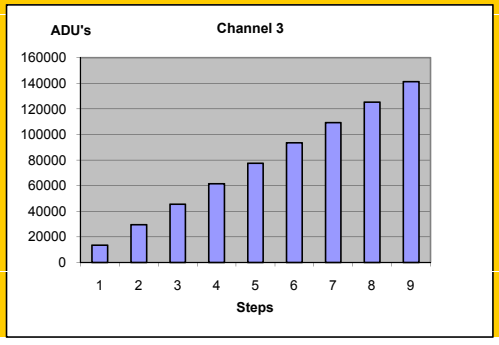
BrdTst6_006 / Channel 2					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12950	12973	12962.7	3.14153	10%
0x333	28934	28957	28946.2	3.05638	20%
0x4cc	44923	44945	44934.2	3.04847	30%
0x666	60946	60969	60957.4	3.0857	40%
0x800	76970	76993	76982	3.1546	50%
0x999	92960	92982	92970.8	3.09666	60%
0xb33	108978	109004	108992	3.21707	70%
0xccc	124980	125004	124992	2.98618	80%
0xe66	141007	141030	141018	3.15677	90%



TEST #6D: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

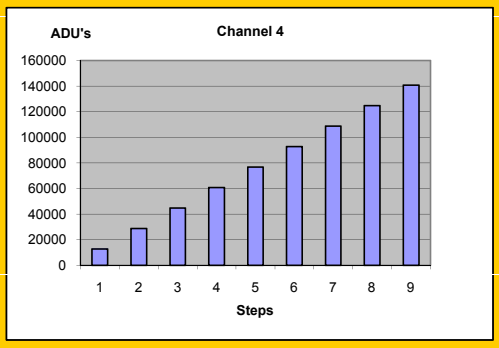
BrdTst6_006 / Channel 3					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13522	13544	13533.4	3.20405	10%
0x333	29477	29501	29488.7	3.23158	20%
0x4cc	45431	45457	45444.7	3.16707	30%
0x666	61428	61449	61438	3.09839	40%
0x800	77422	77444	77433	3.21221	50%
0x999	93376	93398	93387.3	3.16426	60%
0xb33	109370	109392	109382	3.07594	70%
0xccc	125328	125351	125340	3.18744	80%
0xe66	141324	141347	141335	3.16625	90%



TEST #6E: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

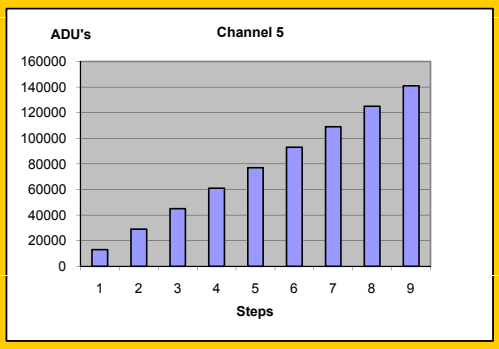
BrdTst6_006 / Channel 4					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12722	12744	12732.8	3.13341	10%
0x333	28713	28735	28723.6	3.11767	20%
0x4cc	44703	44727	44714.4	3.10721	30%
0x666	60734	60755	60744.2	3.08154	40%
0x800	76767	76790	76778	3.15573	50%
0x999	92760	92781	92770.7	3.01017	60%
0xb33	108788	108808	108798	3.10576	70%
0xccc	124792	124817	124805	3.1498	80%
0xe66	140826	140848	140837	3.14624	90%



TEST #6F: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

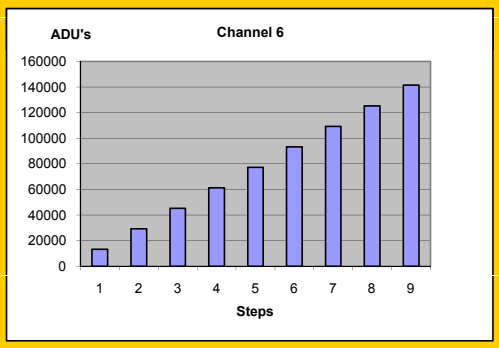
BrdTst6_006 / Channel 5					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12908	12932	12920.3	3.18563	10%
0x333	28907	28929	28917.5	3.21004	20%
0x4cc	44900	44920	44909.7	3.07172	30%
0x666	60936	60959	60946.6	3.24129	40%
0x800	76971	76993	76981.7	3.17889	50%
0x999	92966	92989	92978.7	3.20213	60%
0xb33	109002	109026	109014	3.13135	70%
0xccc	125009	125033	125020	3.20995	80%
0xe66	141047	141069	141058	3.15294	90%



TEST #6G: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

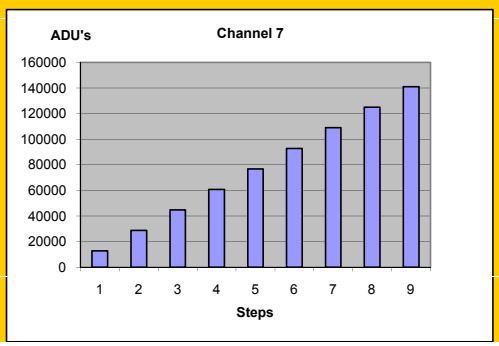
BrdTst6_006 / Channel 6					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13352	13373	13362.3	3.04368	10%
0x333	29334	29358	29346.6	3.07493	20%
0x4cc	45317	45341	45329.8	3.12281	30%
0x666	61342	61364	61353.4	3.14049	40%
0x800	77366	77390	77377.6	2.94285	50%
0x999	93350	93373	93361.6	3.11833	60%
0xb33	109374	109395	109384	3.07461	70%
0xccc	125363	125386	125374	3.11644	80%
0xe66	141386	141409	141398	3.16989	90%



TEST #6H: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

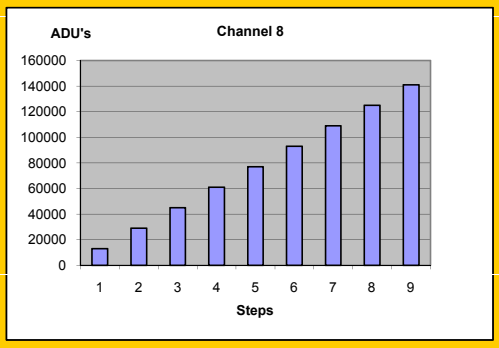
BrdTst6_006 / Channel 7					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12773	12798	12784.9	3.23962	10%
0x333	28774	28800	28787	3.29226	20%
0x4cc	44781	44803	44790.7	3.13736	30%
0x666	60822	60845	60834	3.13744	40%
0x800	76865	76889	76877.7	3.19511	50%
0x999	92872	92898	92883.4	3.21527	60%
0xb33	108914	108936	108924	3.22239	70%
0xccc	124925	124948	124937	3.18419	80%
0xe66	140969	140993	140981	3.21465	90%



TEST #6I: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

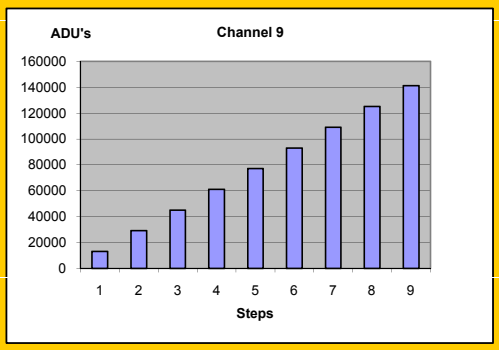
BrdTst6_006 / Channel 8					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12959	12985	12972.7	3.13468	10%
0x333	28960	28984	28973.1	3.10651	20%
0x4cc	44957	44981	44969	3.16716	30%
0x666	60997	61018	61007.8	3.08705	40%
0x800	77032	77054	77042.9	3.31481	50%
0x999	93028	93054	93042.3	3.18451	60%
0xb33	109067	109091	109080	3.16256	70%
0xccc	125078	125100	125090	3.0871	80%
0xe66	141118	141141	141130	3.16684	90%



TEST #6J: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

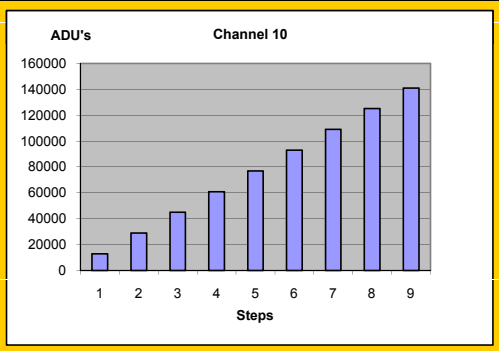
BrdTst6_006 / Channel 9					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13075	13099	13088.2	3.18399	10%
0x333	29060	29084	29072.1	3.16736	20%
0x4cc	45042	45068	45055.3	3.27435	30%
0x666	61069	61091	61080.4	3.15236	40%
0x800	77091	77116	77104.7	3.21378	50%
0x999	93081	93107	93093.9	3.26936	60%
0xb33	109104	109124	109114	3.07207	70%
0xccc	125098	125122	125109	3.09634	80%
0xe66	141120	141145	141132	3.27727	90%



TEST #6K: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

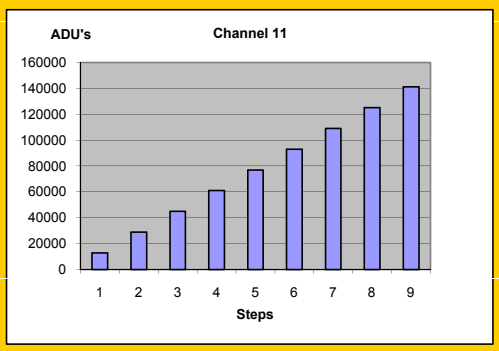
BrdTst6_006 / Channel 10					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12946	12968	12956.4	3.20776	10%
0x333	28937	28957	28947	3.00556	20%
0x4cc	44924	44946	44934.7	3.14447	30%
0x666	60955	60978	60965.7	3.14449	40%
0x800	76985	77008	76996	3.05606	50%
0x999	92977	93000	92989.4	3.19478	60%
0xb33	109007	109033	109018	3.16363	70%
0xccc	125009	125032	125021	3.17688	80%
0xe66	141042	141064	141053	3.14959	90%



TEST #6L: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

BrdTst6_006 / Channel 11					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12959	12981	12971.2	3.23838	10%
0x333	28957	28981	28969.4	3.19071	20%
0x4cc	44958	44982	44968.3	3.23359	30%
0x666	60994	61017	61006.2	3.17316	40%
0x800	77032	77055	77042.7	3.18806	50%
0x999	93034	93057	93044.7	3.20445	60%
0xb33	109068	109092	109080	3.13759	70%
0xccc	125078	125100	125089	3.19962	80%
0xe66	141116	141140	141127	3.15354	90%



Stage 13. Other Bit Tests. Table 11

Electronic Serial Number	0xDB6F97		Board Serial Number	28
Firmware Version	0x193		Name Of Person Testing	S. Holm
Ident Register	0x502		Board passed Functional Tests	YES