# DES 12 Channel Board - Functional Tests: CCD Acquisition Board Revision 1.0

Stage 1. Preparation of documentation and configuration settings - Table 1.

| | | | | |
|---|---|---|---|---|
| Board Part Number | 23 | | Board Serial Number | 0xDB8F85 |
| Date Of Tests | August 2010 | | Name Of Person Testing | S. Holm |
| Suggested Filename To Save | CCDACQ_12Ch_REPORT_BOARD12.xl | | Sequence number: Test | |

Stage 3. Power plane short test - Table 2.

| Supply Name | Short test to ground: Impedance to ground | Test Point | |
|---|---|---|---|
| +1.2VD | 45.00 | TP43 | ~50 ohms |
| +1.8VD | 1.5M | TPB12 | > 1K ohm |
| +2.5VD | 18K | TPB11 | > 1K ohm |
| +3.3VD | 6K | D13 | > 1K ohm |
| +5VD | 19K | D14 | > 1K ohm |
| +5VA | 4M | C267 | > 1K ohm |
| -5VA | 300K | C270 | > 1K ohm |
| +15VA | 500K | C288 | > 1K ohm |
| -15VA | 500K | C282 | > 1K ohm |
| -28VA | 2.6M | C307 | > 1K ohm |

Stage 4. Firmware programming tests - Table 3.

| JTAG Order | Designator | Device | Load File | Check Sum or User Code |
|---|---|---|---|---|
| 1 | U122 | XCF08PFS48C PROM | CcdAcqFpgaV41.mcs | 0014ef670 |
| 2 | U114 | Spartan3 XC3S2000 FPGA | ccdacqfpgav41.bit | 5102801 |

Stage 5. Power Consumption - Table 4.

| Supply Name | Power Supply Consumption: Measured Voltage at test point | Measured Current on power supply | Test Point | |
|---|---|---|---|---|
| +1.2VD | 1.20 | N/A | TP43 | |
| +1.8VD | 1.81 | N/A | TPB12 | |
| +2.5VD | 2.50 | N/A | TPB11 | |
| +3.3VD | 3.28 | 0.302 | D13 | |
| +5VD | 5.20 | 0.148 | D14 | |
| +5VA | 4.84 | 0.552 | C267 | |
| -5VA | -5.00 | 0.437 | C270 | |
| +15VA | 14.96 | 0.558 | C288 | |
| -15VA | -15.06 | 0.406 | C282 | |
| -28VA | -27.72 | 0.196 | C307 | |
| Vref 0+ | 10.04 | N/A | R534 | Vsub+ Reference(+10v) |
| Vref 0- | -2.51 | N/A | R525 | Vsub - Reference(-2.5v) |
| Vref Offset | 2.50 | N/A | R573 | ADC Offset Reference(+2.5v) |
| Vclamp | 1.88 | N/A | VIA | ADC Clamp Voltage(+1.8v) |
| ADC Ref. | 2.50 | N/A | VIA | ADC Reference Voltage(+2.5v) |
| Vref 1+ | 2.50 | N/A | R537 | Vru and Vrl + Reference(+2.5v) |
| Vref 1- | -10.05 | N/A | R535 | Vru and Vrl - Reference(-10v) |
| Vref 2+ | 5.02 | N/A | R563 | Vog + Reference(+5v) |
| Vref 2- | -2.51 | N/A | R555 | Vog - Reference(-2.5v) |
| Vref 3+ | 2.50 | N/A | R543 | Vdd + Reference(+2.5v) |
| Vref 3- | -10.07 | N/A | R571 | Vdd - Reference(-10v) |

| Power Dissipation: |
|---|
| 26.5 Watts |

~27 watts +/- 5%

Stage 7. Basic Bus Transactions - **D**igital **Register** Tests - Table 5.

| Register name | Put an X on any bit that has an error: 31-24 | 23-16 | 15-08 | 07-00 | Function | Test name: Pattern | Walking 0's | Walking 1's |
|---|---|---|---|---|---|---|---|---|
| CDS Control | | | 00000000 | 00000000 | 16 bit R/W | | | |
| Digital Output | 00000000 | 00000000 | 00000000 | 00000000 | 32 bit R/W | | | |
| ADC Config. | | | 0000 | 00000000 | 12 bit R/W | | | |
| Offset DAC | | | 0000 | 00000000 | 12 bit R/W | | | |
| Bias DAC | | | 0000 | 00000000 | 12 bit R/W | | | |
| Telemetry Config. | | | | 0000 | 4 bit R/W | | | |
| Auxilary Config. | | | | 00 00000000 | 10 bit R/W | | | |
| Redirect | | | | 0000 | 4 bit R/W | | | |
| Pixel Transfer | | | | 00000000 | 8 bit R/W | | | |
| Micro SEQ | | | 00000000 | 00000000 | 16 bit R/W | | | |
| RAM Buffer | | | 00000000 | 00000000 | 16 bit R/W | | | |
| LED Control | | | | 0000 | 4 bit R/W | | | |
| Control | | | 00000000 | 00000000 | 16 bit R/W | | | |
| **All Register Test** | 00000000 | 00000000 | 00000000 | 00000000 | 16 bit R/W | **Passed** | **Passed** | **Passed** |

Stage 8. Bias Voltage settings and output enables testing - Table 8

| DAC Value | Bias Voltage Test Data 410 | 2048 | 3686 | 50% rms Noise | 10-90% Rise Time | | | |
|---|---|---|---|---|---|---|---|---|
| Signal | volts | volts | volts | uV | millisec. | Fanout Brd | Slope | Offset |
| Vru 0 | -13.20 | -5.66 | 1.86 | <10 | 1 | BIAS 3 | 217.53 | 3280.67 |
| Vru 1 | -13.20 | -5.66 | 1.86 | <10 | 1 | BIAS 4 | 217.53 | 3280.67 |
| Vru 2 | -13.20 | -5.66 | 1.86 | <10 | 1 | BIAS 5 | 217.53 | 3280.67 |
| Vru 3 | -13.20 | -5.66 | 1.86 | <10 | 1 | BIAS 6 | 217.53 | 3280.67 |
| Vru 4 | -13.20 | -5.66 | 1.86 | <10 | 1 | BIAS 7 | 217.53 | 3280.67 |
| Vru 5 | -13.20 | -5.66 | 1.86 | <10 | 1 | BIAS 8 | 217.53 | 3280.67 |
| Vru 6 | -13.20 | -5.66 | 1.86 | NA | NA | BIAS 9 | 217.53 | 3280.67 |
| Vru 7 | -13.20 | -5.66 | 1.86 | NA | NA | BIAS 10 | 217.53 | 3280.67 |
| Vrl 0 | -13.20 | -5.66 | 1.86 | <10 | 1 | BIAS 11 | 217.53 | 3280.67 |
| Vrl 1 | -13.20 | -5.66 | 1.86 | <10 | 1 | BIAS 12 | 217.53 | 3280.67 |
| Vrl 2 | -13.20 | -5.66 | 1.86 | <10 | 1 | BIAS 13 | 217.53 | 3280.67 |
| Vrl 3 | -13.20 | -5.66 | 1.86 | <10 | 1 | BIAS 14 | 217.53 | 3280.67 |
| Vrl 4 | -13.20 | -5.66 | 1.86 | <10 | 1 | BIAS 15 | 217.53 | 3280.67 |
| Vrl 5 | -13.20 | -5.66 | 1.86 | <10 | 1 | BIAS 16 | 217.53 | 3280.67 |
| Vrl 6 | -13.20 | -5.66 | 1.86 | NA | NA | BIAS 17 | 217.53 | 3280.67 |
| Vrl 7 | -13.20 | -5.66 | 1.86 | NA | NA | BIAS 18 | 217.53 | 3280.67 |
| Vog 0 | -1.75 | 1.25 | 4.26 | <10 | 1 | BIAS 19 | 545.09 | 1364.82 |
| Vog 1 | -1.75 | 1.25 | 4.26 | <10 | 1 | BIAS 20 | 545.09 | 1364.82 |
| Vog 2 | -1.75 | 1.25 | 4.26 | <10 | 1 | BIAS 21 | 545.09 | 1364.82 |
| Vog 3 | -1.75 | 1.25 | 4.26 | <10 | 1 | BIAS 22 | 545.09 | 1364.82 |
| Vog 4 | -1.75 | 1.25 | 4.26 | <10 | 1 | BIAS 23 | 545.09 | 1364.82 |
| Vog 5 | -1.75 | 1.25 | 4.26 | <10 | 1 | BIAS 24 | 545.09 | 1364.82 |
| Vog 6 | -1.75 | 1.25 | 4.26 | NA | NA | BIAS 25 | 545.09 | 1364.82 |
| Vog 7 | -1.75 | 1.25 | 4.26 | NA | NA | BIAS 26 | 545.09 | 1364.82 |
| Vdd 0 | -22.01 | -9.47 | 3.10 | <10 | 20 | BIAS 27 | 130.47 | 3282.21 |
| Vdd 1 | -22.06 | -9.47 | 3.10 | <10 | 20 | BIAS 28 | 130.21 | 3281.93 |
| Vdd 2 | -22.17 | -9.47 | 3.10 | <10 | 20 | BIAS 29 | 129.64 | 3281.30 |
| Vdd 3 | -22.05 | -9.47 | 3.10 | <10 | 20 | BIAS 30 | 130.26 | 3281.98 |
| Vdd 4 | -22.05 | -9.47 | 3.10 | <10 | 20 | BIAS 21 | 130.26 | 3281.98 |
| Vdd 5 | -22.05 | -9.47 | 3.10 | <10 | 20 | BIAS 32 | 130.26 | 3281.98 |
| Vdd 6 | -22.03 | -9.47 | 3.10 | NA | NA | BIAS 33 | 130.36 | 3282.09 |
| Vdd 7 | -22.03 | -9.47 | 3.10 | NA | NA | BIAS 34 | 130.36 | 3282.09 |

| Vru | Slope | | Offset |
|---|---|---|---|
| Mean | 217.53 | Mean | 3280.67 |
| Stdev | 0 | Stdev | 9.09495E-13 |
| Average | 217.52975 | Average | 3280.668598 |
| | Dac # | Average voltage | |
| | 0 | -15.0 | |
| | 4095 | 3.7 | |

| Vrl | Slope | | Offset |
|---|---|---|---|
| Mean | 217.53 | Mean | 3280.67 |
| Stdev | 0 | Stdev | 9.09495E-13 |
| Average | 217.52975 | Average | 3280.668598 |
| | Dac # | Average voltage | |
| | 0 | -15.1 | |
| | 4095 | 3.7 | |

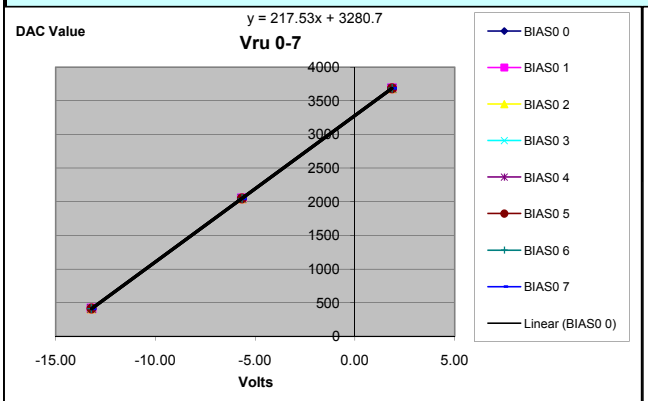
| Vog | Slope | | Offset |
|---|---|---|---|
| Mean | 545.09 | Mean | 1364.82 |
| Stdev | 1.137E-13 | Stdev | 0 |
| Average | 545.09101 | Average | 1364.819266 |
| | Dac # | Average voltage | |
| | 0 | -2.5 | |
| | 4095 | 5.0 | |

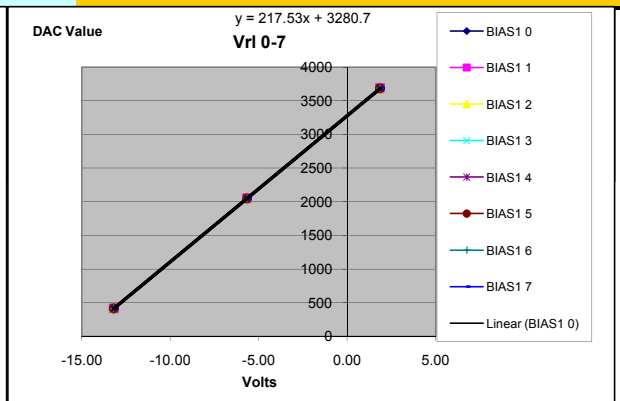
| Vdd | Slope | | Offset |
|---|---|---|---|
| Mean | 130.23 | Mean | 3281.95 |
| Stdev | 0.2353181 | Stdev | 0.259431075 |
| Average | 130.22635 | Average | 3281.945392 |
| | Dac # | Average voltage | |
| | 0 | -25.2 | |
| | 4095 | 6.3 | |

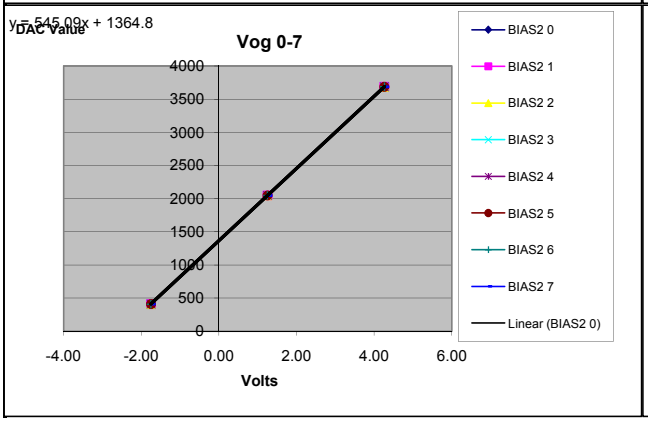
Notes and Observations

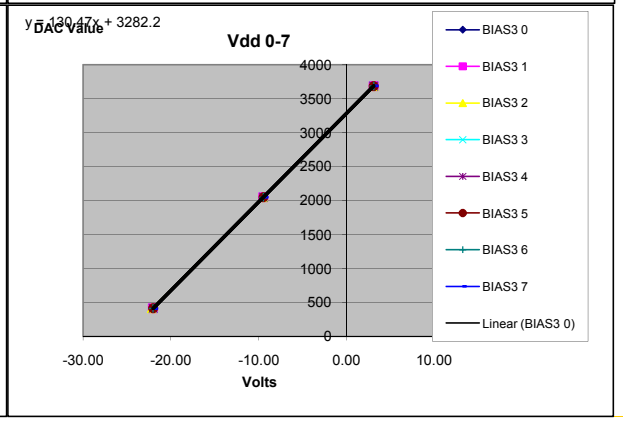
Checked for oscillations using a Agilent Oscilloscpe on AC.**OK**

average min & max voltages
(dac# -offset)/slope=voltage



## Stage 8B. Telemetry System Tests - Table 7 (Bias Telemetry Tests)

DAC Value: 410 / 3686

| Signal | Telemetry Return Values 10% | 90% | Bias Signals Set Volts 10% | 90% | Resolved Values for Telemetry Channel Slope | Offset |
|---|---|---|---|---|---|---|
| Vru 0 | -1752 | 422 | -13.20 | 1.86 | 144.3559 | 153.50 |
| Vru 1 | -1750 | 422 | -13.20 | 1.86 | 144.2231 | 153.75 |
| Vru 2 | -1756 | 422 | -13.20 | 1.86 | 144.6215 | 153.00 |
| Vru 3 | -1754 | 422 | -13.20 | 1.86 | 144.4887 | 153.25 |
| Vru 4 | -1756 | 422 | -13.20 | 1.86 | 144.6215 | 153.00 |
| Vru 5 | -1756 | 422 | -13.20 | 1.86 | 144.6215 | 153.00 |
| Vru 6 | -1756 | 422 | -13.20 | 1.86 | 144.6215 | 153.00 |
| Vru 7 | -1752 | 422 | -13.20 | 1.86 | 144.3559 | 153.50 |
| Vrl 0 | -1762 | 422 | -13.20 | 1.86 | 145.0199 | 152.26 |
| Vrl 1 | -1760 | 422 | -13.20 | 1.86 | 144.8871 | 152.51 |
| Vrl 2 | -1757 | 422 | -13.20 | 1.86 | 144.6879 | 152.88 |
| Vrl 3 | -1761 | 422 | -13.20 | 1.86 | 144.9535 | 152.39 |
| Vrl 4 | -1760 | 422 | -13.20 | 1.86 | 144.8871 | 152.51 |
| Vrl 5 | -1760 | 422 | -13.20 | 1.86 | 144.8871 | 152.51 |
| Vrl 6 | -1759 | 422 | -13.20 | 1.86 | 144.8207 | 152.63 |
| Vrl 7 | -1761 | 423 | -13.20 | 1.86 | 145.0199 | 153.26 |
| Vog 0 | -364 | 874 | -1.75 | 4.26 | 205.9900 | -3.52 |
| Vog 1 | -364 | 874 | -1.75 | 4.26 | 205.9900 | -3.52 |
| Vog 2 | -364 | 874 | -1.75 | 4.26 | 205.9900 | -3.52 |
| Vog 3 | -364 | 873 | -1.75 | 4.26 | 205.8236 | -3.81 |
| Vog 4 | -365 | 874 | -1.75 | 4.26 | 206.1564 | -4.23 |
| Vog 5 | -364 | 874 | -1.75 | 4.26 | 205.9900 | -3.52 |
| Vog 6 | -364 | 874 | -1.75 | 4.26 | 205.9900 | -3.52 |
| Vog 7 | -364 | 874 | -1.75 | 4.26 | 205.9900 | -3.52 |
| Vdd 0 | -1735 | 572 | -22.01 | 3.10 | 91.8757 | 287.19 |
| Vdd 1 | -1743 | 573 | -22.06 | 3.10 | 92.0509 | 287.64 |
| Vdd 2 | -1752 | 574 | -22.17 | 3.10 | 92.0459 | 288.66 |
| Vdd 3 | -1743 | 573 | -22.05 | 3.10 | 92.0875 | 287.53 |
| Vdd 4 | -1746 | 573 | -22.05 | 3.10 | 92.2068 | 287.16 |
| Vdd 5 | -1747 | 573 | -22.05 | 3.10 | 92.2465 | 287.04 |
| Vdd 6 | -1744 | 573 | -22.03 | 3.10 | 92.2006 | 287.18 |
| Vdd 7 | -1741 | 572 | -22.03 | 3.10 | 92.0414 | 286.67 |

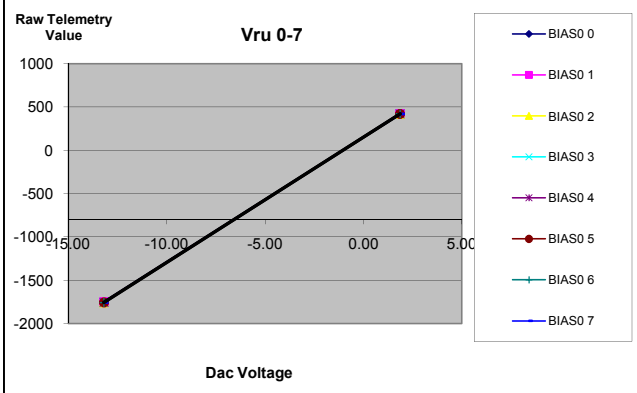
AVERAGE

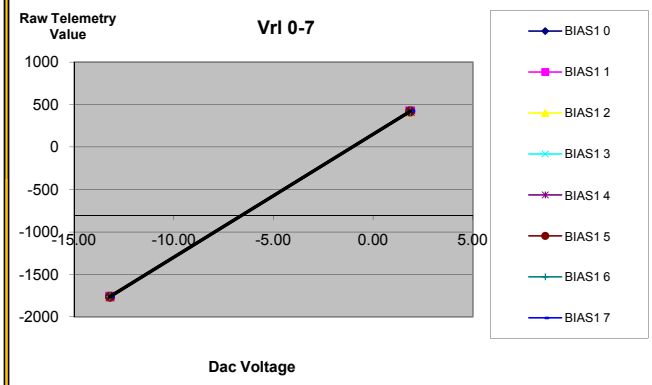
| Vru | Slope | | Offset |
|---|---|---|---|
| Mean | 144.49 | Mean | 153.25 |
| Stdev | 0.1484773 | Stdev | 0.2761678 |

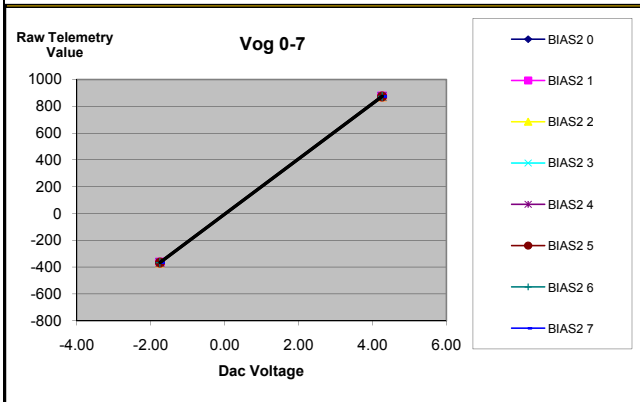
| Vrl | Slope | | Offset |
|---|---|---|---|
| Mean | 144.90 | Mean | 152.62 |
| Stdev | 0.1019937 | Stdev | 0.2957547 |

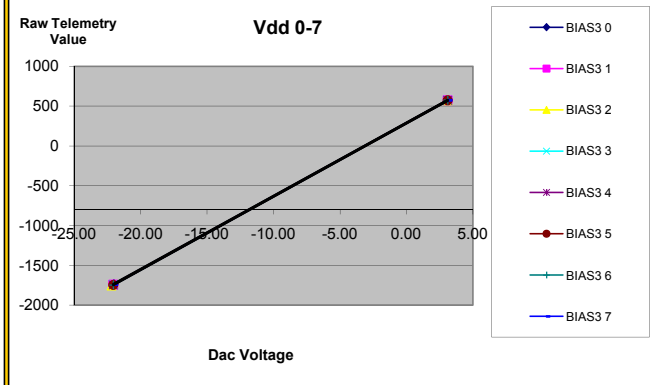
| Vog | Slope | | Offset |
|---|---|---|---|
| Mean | 205.99 | Mean | -3.64 |
| Stdev | 0.0831947 | Stdev | 0.240367 |

| Vdd | Slope | | Offset |
|---|---|---|---|
| Mean | 92.09 | Mean | 287.38 |
| Stdev | 0.1128876 | Stdev | 0.5557698 |




## Stage 8C. Bias Voltage output enables testing - Table 8

Place a line through Bias Voltage name if enable/disable switch works

| | | | | | |
|---|---|---|---|---|---|
| Vru 0 | Vru 1 | Vru 2 | Vru 3 | Vru 4 | Vru 5 |
| Vrl 0 | Vrl 1 | Vrl 2 | Vrl 3 | Vrl 4 | Vrl 5 |
| Vog 0 | Vog 1 | Vog 2 | Vog 3 | Vog 4 | Vog 5 |
| Vdd 0 | Vdd 1 | Vdd 2 | Vdd 3 | Vdd 4 | Vdd 5 |

Stage 9. Vsub and Heater Control testing - Table 9

| DAC Value | Vsub Measured Voltage Test Data 10% | 50% | 90% |
|---|---|---|---|
| Signal | volts | volts | volts |
| Vsub - rate | -1.25 | 3.77 | 8.78 |
| Vsub - Limit | -1.25 | 3.77 | 8.78 |
| Vsub0 | 0.00 | 0.00 | 0.00 |
| | Vsub Enable Bit - pass | | |

| DAC Value | Telemetery Readback Test Data 10% | 50% | 90% |
|---|---|---|---|
| Signal | dec | dec | dec |
| Vbias 0 | 152 | 269 | 452 |
| Vbias 1 | -29 | 696 | 1422 |
| RTD1 | 220 | NA | NA |
| RTD2 | 248 | NA | NA |
| RTD3 | 275 | NA | NA |
| RTD4 | 300 | NA | NA |
| RTD5 | 324 | NA | NA |
| RTD6 | 351 | NA | NA |
| Reference 4096 | 836 | NA | NA |
| eference buffere | 836 | NA | NA |

## Stage 10. Video Offset DAC Tests - Table 10.

| | DAC Value 410 | | | | DAC Value 2048 | | | | DAC Value 3686 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADC | DC Volts | RMS Noise | Rise Time | ADU | DC Volts | RMS Noise | Rise Time | ADU | DC Volts | RMS Noise | Rise Time | ADU |
| 0 | 0.250 | NA | NA | 17080 | 1.250 | | NA | 81154 | 2.250 | NA | 500ms | 145228 |
| 1 | 0.250 | NA | NA | 17293 | 1.250 | | NA | 81203 | 2.250 | NA | 500ms | 145116 |
| 2 | 0.250 | NA | NA | 17118 | 1.250 | | NA | 81134 | 2.250 | NA | 500ms | 145155 |
| 3 | 0.250 | NA | NA | 17155 | 1.250 | | NA | 81128 | 2.250 | NA | 500ms | 145102 |
| 4 | 0.250 | NA | NA | 17181 | 1.250 | | NA | 81180 | 2.250 | NA | 500ms | 145177 |
| 5 | 0.250 | NA | NA | 17009 | 1.250 | | NA | 81089 | 2.250 | NA | 500ms | 145173 |
| 6 | 0.250 | NA | NA | 17065 | 1.250 | | NA | 81117 | 2.250 | NA | 500ms | 145172 |
| 7 | 0.250 | NA | NA | 17090 | 1.250 | | NA | 81090 | 2.250 | NA | 500ms | 145092 |
| 8 | 0.250 | NA | NA | 17120 | 1.250 | | NA | 81092 | 2.250 | NA | 500ms | 145062 |
| 9 | 0.250 | NA | NA | 17121 | 1.250 | | NA | 81122 | 2.250 | NA | 500ms | 145131 |
| 10 | 0.250 | NA | NA | 16850 | 1.250 | | NA | 81009 | 2.250 | NA | 500ms | 145169 |
| 11 | 0.250 | NA | NA | 17050 | 1.250 | | NA | 81073 | 2.250 | NA | 500ms | 145101 |

| ADC | DC Volts | | Data Set | | |
|---|---|---|---|---|---|
| Channel | Slope | Offset | 410 | 2048 | 3686 |
| 0 | 1638.000 | 0.500 | 0.250 | 1.250 | 2.250 |
| 1 | 1638.000 | 0.500 | 0.250 | 1.250 | 2.250 |
| 2 | 1638.000 | 0.500 | 0.250 | 1.250 | 2.250 |
| 3 | 1638.000 | 0.500 | 0.250 | 1.250 | 2.250 |
| 4 | 1638.000 | 0.500 | 0.250 | 1.250 | 2.250 |
| 5 | 1638.000 | 0.500 | 0.250 | 1.250 | 2.250 |
| 6 | 1638.000 | 0.500 | 0.250 | 1.250 | 2.250 |
| 7 | 1638.000 | 0.500 | 0.250 | 1.250 | 2.250 |
| 8 | 1638.000 | 0.500 | 0.250 | 1.250 | 2.250 |
| 9 | 1638.000 | 0.500 | 0.250 | 1.250 | 2.250 |
| 10 | 1638.000 | 0.500 | 0.250 | 1.250 | 2.250 |
| 11 | 1638.000 | 0.500 | 0.250 | 1.250 | 2.250 |

(dac# -offset)/slope=Voltage

| ADC | ADU's | | Data Set | | |
|---|---|---|---|---|---|
| Channel | Slope | Offset | 410 | 2048 | 3686 |
| 0 | 0.026 | -26.64 | 17080 | 81154 | 145228 |
| 1 | 0.026 | -33.19 | 17293 | 81203 | 145116 |
| 2 | 0.026 | -27.97 | 17118 | 81134 | 145155 |
| 3 | 0.026 | -29.24 | 17155 | 81128 | 145102 |
| 4 | 0.026 | -29.75 | 17181 | 81180 | 145177 |
| 5 | 0.026 | -24.75 | 17009 | 81089 | 145173 |
| 6 | 0.026 | -25.17 | 17065 | 81117 | 145330 |
| 7 | 0.026 | -27.30 | 17090 | 81090 | 145103 |
| 8 | 0.026 | -27.94 | 17120 | 81092 | 145118 |
| 9 | 0.026 | -27.35 | 17121 | 81122 | 145232 |
| 10 | 0.026 | -20.24 | 16850 | 81009 | 145161 |
| 11 | 0.026 | -25.83 | 17050 | 81073 | 145146 |

(dac# -offset)/slope=ADU

Notes and Observations

Checked for oscillations using a Agilent Oscilloscope on AC. OK

## Stage 11. CDS Control Functions and Video Channel Performanc

TEST #1: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit is held static. The purpose of this test is to verify the correct operation of the ADC devices and measure the noise of the Offset voltage generators, ADC buffer amplifiers and ADC devices

**Noise Test 1**

| | Min Pix Value | Max Pix | Mean Pix | Std. Dev. |
|---|---|---|---|---|
| CH 0 | 81145 | 8.12E+04 | 81154.2 | 2.08813 |
| CH 1 | 81197 | 8.12E+04 | 81204.7 | 2.14208 |
| CH 2 | 81130 | 8.11E+04 | 81138.2 | 2.2467 |
| CH 3 | 81119 | 8.11E+04 | 81126.7 | 2.30251 |
| CH 4 | 81172 | 8.12E+04 | 81181.6 | 2.2759 |
| CH 5 | 81083 | 8.11E+04 | 81091.6 | 2.48506 |
| CH 6 | 81113 | 8.11E+04 | 81121.3 | 2.33365 |
| CH 7 | 81080 | 8.11E+04 | 81090.3 | 2.38788 |
| CH 8 | 81082 | 8.11E+04 | 81090.3 | 2.20309 |
| CH 9 | 81120 | 8.11E+04 | 81127.8 | 2.33296 |
| CH 10 | 81001 | 8.10E+04 | 81010.6 | 2.21432 |
| CH 11 | 81067 | 8.11E+04 | 81074.4 | 2.44425 |

TEST #2: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the invert/non-invert and the DC Restore switches are held static.

**Noise Test 2**

| | Min Pix Value | Max Pix | Mean Pix | Std. Dev. |
|---|---|---|---|---|
| CH 0 | 76614 | 7.66E+04 | 76623.9 | 2.75451 |
| CH 1 | 77018 | 7.70E+04 | 77028.3 | 2.71086 |
| CH 2 | 76714 | 7.67E+04 | 76724.4 | 2.84614 |
| CH 3 | 76849 | 7.69E+04 | 76859.1 | 2.85848 |
| CH 4 | 76501 | 7.65E+04 | 76511.3 | 2.72612 |
| CH 5 | 77005 | 7.70E+04 | 77014 | 2.83103 |
| CH 6 | 76948 | 7.70E+04 | 76957.9 | 2.83743 |
| CH 7 | 76973 | 7.70E+04 | 76983.2 | 2.78139 |
| CH 8 | 76647 | 7.67E+04 | 76659.1 | 2.69109 |
| CH 9 | 77186 | 7.72E+04 | 77196.8 | 2.85796 |
| CH 10 | 75522 | 7.55E+04 | 75533.4 | 2.77271 |
| CH 11 | 76769 | 7.68E+04 | 76779.6 | 2.9192 |

TEST #3: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the DC Restore switch is held static.

**Noise Test 3**

| | Min Pix Value | Max Pix | Mean Pix | Std. Dev. |
|---|---|---|---|---|
| CH 0 | 76622 | 7.66E+04 | 76635.4 | 3.0576 |
| CH 1 | 77012 | 7.70E+04 | 77021.9 | 2.97357 |
| CH 2 | 76714 | 7.67E+04 | 76725 | 3.02968 |
| CH 3 | 76825 | 7.68E+04 | 76836 | 2.95167 |
| CH 4 | 76497 | 7.65E+04 | 76508.4 | 3.01388 |
| CH 5 | 76996 | 7.70E+04 | 77007.7 | 2.9909 |
| CH 6 | 76936 | 7.70E+04 | 76947.3 | 3.09328 |
| CH 7 | 76981 | 7.70E+04 | 76991.1 | 3.05021 |
| CH 8 | 76641 | 7.67E+04 | 76650.4 | 3.01175 |
| CH 9 | 77185 | 7.72E+04 | 77197.1 | 3.09002 |
| CH 10 | 75524 | 7.55E+04 | 75534.2 | 3.00842 |
| CH 11 | 76766 | 7.68E+04 | 76777 | 3.06366 |

TEST #4: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition.

**Noise Test 4**

| | Min Pix Value | Max Pix | Mean Pix | Std. Dev. |
|---|---|---|---|---|
| CH 0 | 76617 | 7.66E+04 | 76628.5 | 3.16032 |
| CH 1 | 77015 | 7.70E+04 | 77025.9 | 2.96432 |
| CH 2 | 76718 | 7.67E+04 | 76729.2 | 3.20106 |
| CH 3 | 76824 | 7.68E+04 | 76835.1 | 3.04599 |
| CH 4 | 76530 | 7.66E+04 | 76541.6 | 3.14286 |
| CH 5 | 76985 | 7.70E+04 | 76997.4 | 3.10344 |
| CH 6 | 76944 | 7.70E+04 | 76954.3 | 3.15488 |
| CH 7 | 76948 | 7.70E+04 | 76958.7 | 3.17573 |
| CH 8 | 76680 | 7.67E+04 | 76691.3 | 2.99463 |
| CH 9 | 77107 | 7.71E+04 | 77117.9 | 3.11566 |
| CH 10 | 75533 | 7.56E+04 | 75544.3 | 3.15297 |
| CH 11 | 76727 | 7.68E+04 | 76737.9 | 3.04729 |

TEST #5: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the circuitry set to high GAIN.

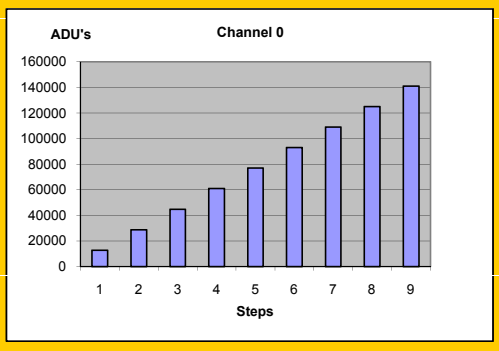
**Noise Test 5**

| | Min Pix Value | Max Pix | Mean Pix | Std. Dev. |
|---|---|---|---|---|
| CH 0 | 76626 | 7.67E+04 | 76639.1 | 3.73011 |
| CH 1 | 77024 | 7.71E+04 | 77038.2 | 3.66975 |
| CH 2 | 76733 | 7.68E+04 | 76746.6 | 3.72456 |
| CH 3 | 76827 | 7.69E+04 | 76840.5 | 3.65472 |
| CH 4 | 76534 | 7.66E+04 | 76545.8 | 3.52486 |
| CH 5 | 76979 | 7.70E+04 | 76995.4 | 3.56162 |
| CH 6 | 76943 | 7.70E+04 | 76956.7 | 3.67246 |
| CH 7 | 76946 | 7.70E+04 | 76960.1 | 3.63386 |
| CH 8 | 76731 | 7.68E+04 | 76744.8 | 3.64082 |
| CH 9 | 77104 | 7.71E+04 | 77118 | 3.6251 |
| CH 10 | 75595 | 7.56E+04 | 75607.6 | 3.65224 |
| CH 11 | 76722 | 7.68E+04 | 76737.9 | 3.56241 |

TEST #6A: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

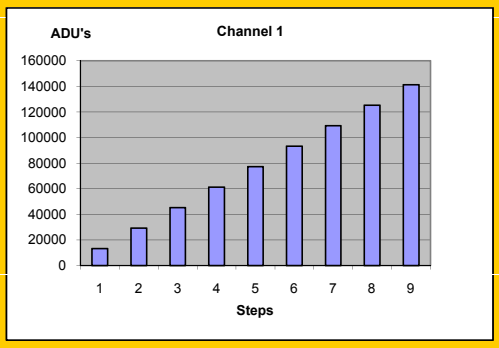
| BrdTst6_006 / Channel 0 | | | | | |
|---|---|---|---|---|---|
| OFFSET DAC VALUE | Min Pix Value | Max Pix Value | Mean Pix Value | Std. Dev. | Remarks |
| 0x19a | 12859 | 12882 | 12870 | 3.20841 | 10% |
| 0x333 | 28858 | 28883 | 28868.5 | 3.07955 | 20% |
| 0x4cc | 44853 | 44875 | 44864.8 | 3.17196 | 30% |
| 0x666 | 60890 | 60915 | 60902.1 | 3.22532 | 40% |
| 0x800 | 76929 | 76950 | 76939.9 | 3.16258 | 50% |
| 0x999 | 92929 | 92955 | 92941.3 | 3.25865 | 60% |
| 0xb33 | 108969 | 108992 | 108980 | 3.15813 | 70% |
| 0xccc | 124967 | 124990 | 124979 | 3.12205 | 80% |
| 0xe66 | 141007 | 141029 | 141018 | 3.17994 | 90% |




TEST #6B: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

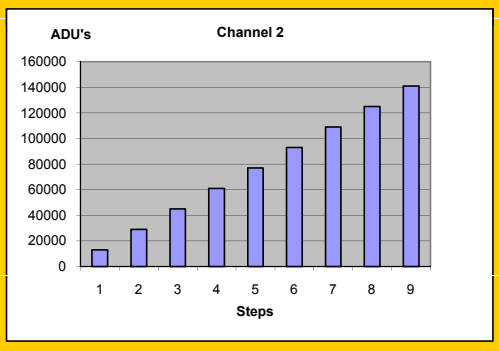
| BrdTst6_006 / Channel 1 | | | | | |
|---|---|---|---|---|---|
| OFFSET DAC VALUE | Min Pix Value | Max Pix Value | Mean Pix Value | Std. Dev. | Remarks |
| 0x19a | 13347 | 13371 | 13358.7 | 3.07353 | 10% |
| 0x333 | 29300 | 29326 | 29314.4 | 3.22372 | 20% |
| 0x4cc | 45263 | 45285 | 45273.2 | 3.08263 | 30% |
| 0x666 | 61257 | 61280 | 61268.5 | 3.16297 | 40% |
| 0x800 | 77254 | 77274 | 77264.7 | 3.05399 | 50% |
| 0x999 | 93213 | 93234 | 93222.9 | 3.04882 | 60% |
| 0xb33 | 109209 | 109230 | 109219 | 3.10595 | 70% |
| 0xccc | 125170 | 125192 | 125181 | 3.14398 | 80% |
| 0xe66 | 141165 | 141187 | 141176 | 3.16723 | 90% |




TEST #6C: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

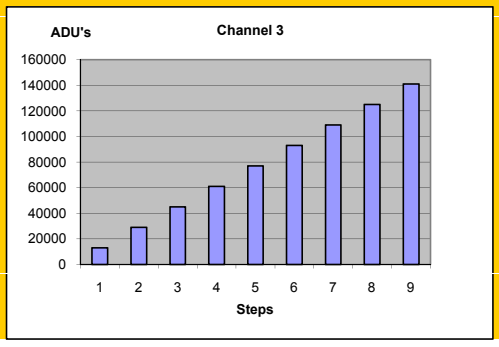
| BrdTst6_006 / Channel 2 | | | | | |
|---|---|---|---|---|---|
| OFFSET DAC VALUE | Min Pix Value | Max Pix Value | Mean Pix Value | Std. Dev. | Remarks |
| 0x19a | 12989 | 13011 | 12999.3 | 3.03618 | 10% |
| 0x333 | 28973 | 28994 | 28983.5 | 3.0504 | 20% |
| 0x4cc | 44957 | 44980 | 44968 | 3.09428 | 30% |
| 0x666 | 60979 | 61004 | 60992 | 3.0334 | 40% |
| 0x800 | 77009 | 77032 | 77019.1 | 3.167 | 50% |
| 0x999 | 92995 | 93017 | 93006.1 | 3.20126 | 60% |
| 0xb33 | 109019 | 109042 | 109031 | 3.24137 | 70% |
| 0xccc | 125006 | 125030 | 125018 | 3.1586 | 80% |
| 0xe66 | 141030 | 141052 | 141041 | 3.03319 | 90% |




TEST #6D: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

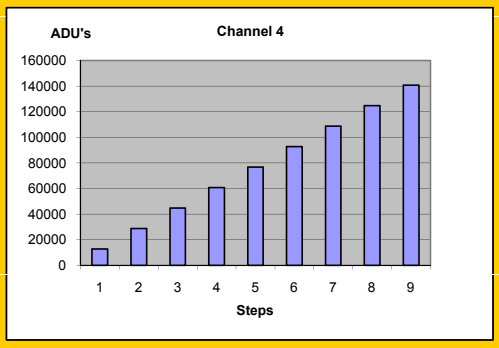
| BrdTst6_006 / Channel 3 | | | | | |
|---|---|---|---|---|---|
| OFFSET DAC VALUE | Min Pix Value | Max Pix Value | Mean Pix Value | Std. Dev. | Remarks |
| 0x19a | 13073 | 13096 | 13085.5 | 3.14548 | 10% |
| 0x333 | 29048 | 29070 | 29058.7 | 3.14328 | 20% |
| 0x4cc | 45024 | 45050 | 45035.8 | 3.1757 | 30% |
| 0x666 | 61036 | 61060 | 61048.4 | 3.1169 | 40% |
| 0x800 | 77050 | 77074 | 77061.1 | 3.09428 | 50% |
| 0x999 | 93027 | 93050 | 93037.6 | 3.23671 | 60% |
| 0xb33 | 109038 | 109062 | 109051 | 3.23179 | 70% |
| 0xccc | 125018 | 125040 | 125029 | 3.19333 | 80% |
| 0xe66 | 141032 | 141056 | 141043 | 3.0283 | 90% |



TEST #6E: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

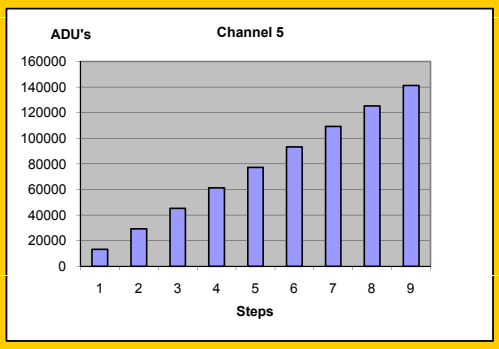
| BrdTst6_006 / Channel 4 | | | | | |
|---|---|---|---|---|---|
| OFFSET DAC VALUE | Min Pix Value | Max Pix Value | Mean Pix Value | Std. Dev. | Remarks |
| 0x19a | 12825 | 12849 | 12837.5 | 3.18401 | 10% |
| 0x333 | 28806 | 28829 | 28817.1 | 3.15789 | 20% |
| 0x4cc | 44788 | 44811 | 44799.3 | 3.14558 | 30% |
| 0x666 | 60805 | 60830 | 60818.6 | 2.9983 | 40% |
| 0x800 | 76824 | 76844 | 76833.8 | 2.92121 | 50% |
| 0x999 | 92801 | 92823 | 92812.2 | 3.17581 | 60% |
| 0xb33 | 108821 | 108844 | 108832 | 3.16964 | 70% |
| 0xccc | 124804 | 124828 | 124816 | 3.2192 | 80% |
| 0xe66 | 140824 | 140846 | 140835 | 3.0223 | 90% |




TEST #6F: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

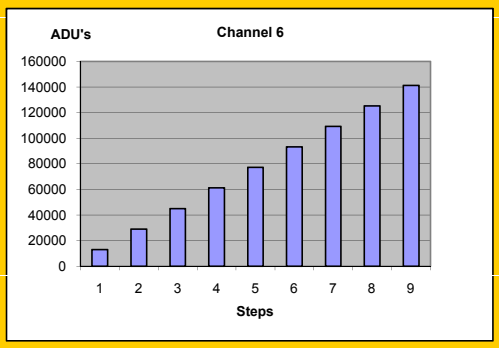
| BrdTst6_006 / Channel 5 | | | | | |
|---|---|---|---|---|---|
| OFFSET DAC VALUE | Min Pix Value | Max Pix Value | Mean Pix Value | Std. Dev. | Remarks |
| 0x19a | 13149 | 13173 | 13161 | 3.16616 | 10% |
| 0x333 | 29152 | 29177 | 29163 | 3.20335 | 20% |
| 0x4cc | 45151 | 45176 | 45161.8 | 3.09516 | 30% |
| 0x666 | 61193 | 61216 | 61203.3 | 3.15949 | 40% |
| 0x800 | 77229 | 77251 | 77240.6 | 3.15886 | 50% |
| 0x999 | 93231 | 93253 | 93242.2 | 3.18007 | 60% |
| 0xb33 | 109271 | 109296 | 109283 | 3.14105 | 70% |
| 0xccc | 125275 | 125296 | 125285 | 3.02128 | 80% |
| 0xe66 | 141315 | 141338 | 141327 | 3.21081 | 90% |




TEST #6G: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

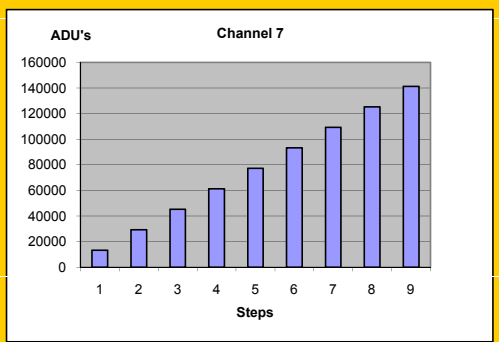
| BrdTst6_006 / Channel 6 | | | | | |
|---|---|---|---|---|---|
| OFFSET DAC VALUE | Min Pix Value | Max Pix Value | Mean Pix Value | Std. Dev. | Remarks |
| 0x19a | 13124 | 13146 | 13134.7 | 3.20981 | 10% |
| 0x333 | 29117 | 29139 | 29126.9 | 3.05292 | 20% |
| 0x4cc | 45110 | 45132 | 45121.9 | 3.11489 | 30% |
| 0x666 | 61142 | 61165 | 61154.3 | 3.11914 | 40% |
| 0x800 | 77172 | 77196 | 77183.8 | 3.07787 | 50% |
| 0x999 | 93168 | 93188 | 93178.8 | 3.15589 | 60% |
| 0xb33 | 109201 | 109222 | 109211 | 3.18104 | 70% |
| 0xccc | 125199 | 125222 | 125211 | 3.16411 | 80% |
| 0xe66 | 141231 | 141254 | 141242 | 3.16636 | 90% |




TEST #6H: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

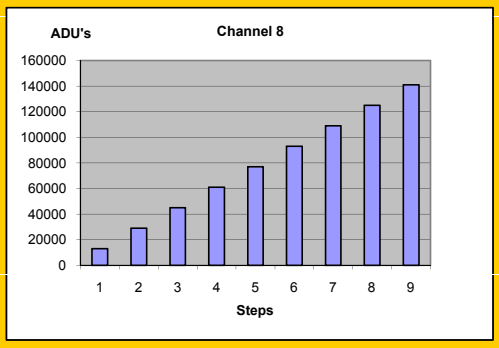
| BrdTst6_006 / Channel 7 | | | | | |
|---|---|---|---|---|---|
| OFFSET DAC VALUE | Min Pix Value | Max Pix Value | Mean Pix Value | Std. Dev. | Remarks |
| 0x19a | 13184 | 13207 | 13195 | 3.17169 | 10% |
| 0x333 | 29162 | 29185 | 29173.5 | 3.00194 | 20% |
| 0x4cc | 45141 | 45164 | 45153.1 | 3.13904 | 30% |
| 0x666 | 61161 | 61182 | 61172 | 3.1755 | 40% |
| 0x800 | 77181 | 77206 | 77192.9 | 3.15243 | 50% |
| 0x999 | 93163 | 93190 | 93176.2 | 3.23002 | 60% |
| 0xb33 | 109182 | 109208 | 109194 | 3.17382 | 70% |
| 0xccc | 125164 | 125190 | 125178 | 3.21831 | 80% |
| 0xe66 | 141184 | 141206 | 141196 | 3.16483 | 90% |



TEST #6I: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

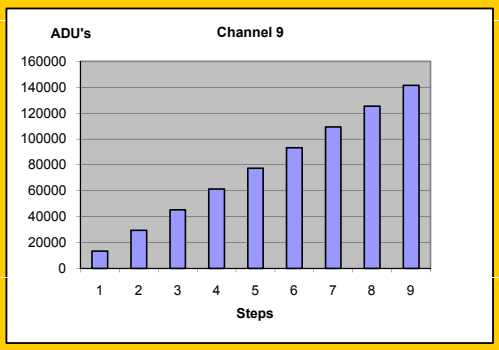
| BrdTst6_006 / Channel 8 | | | | | |
|---|---|---|---|---|---|
| OFFSET DAC VALUE | Min Pix Value | Max Pix Value | Mean Pix Value | Std. Dev. | Remarks |
| 0x19a | 12980 | 13002 | 12991 | 3.1104 | 10% |
| 0x333 | 28952 | 28974 | 28963.4 | 3.0219 | 20% |
| 0x4cc | 44926 | 44951 | 44938.2 | 3.14398 | 30% |
| 0x666 | 60937 | 60962 | 60949.9 | 3.19694 | 40% |
| 0x800 | 76953 | 76973 | 76962.3 | 3.09516 | 50% |
| 0x999 | 92924 | 92947 | 92936.2 | 3.17854 | 60% |
| 0xb33 | 108938 | 108960 | 108949 | 3.1741 | 70% |
| 0xccc | 124915 | 124938 | 124926 | 3.13454 | 80% |
| 0xe66 | 140928 | 140950 | 140939 | 3.20022 | 90% |




TEST #6J: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

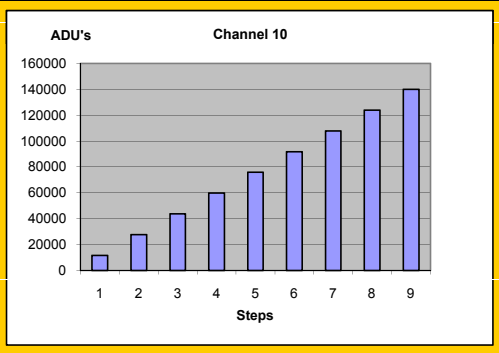
| BrdTst6_006 / Channel 9 | | | | | |
|---|---|---|---|---|---|
| OFFSET DAC VALUE | Min Pix Value | Max Pix Value | Mean Pix Value | Std. Dev. | Remarks |
| 0x19a | 13364 | 13389 | 13377.1 | 3.1979 | 10% |
| 0x333 | 29347 | 29368 | 29357.7 | 3.18382 | 20% |
| 0x4cc | 45328 | 45352 | 45340 | 3.21363 | 30% |
| 0x666 | 61351 | 61372 | 61361.2 | 3.1198 | 40% |
| 0x800 | 77364 | 77391 | 77377.8 | 3.16037 | 50% |
| 0x999 | 93351 | 93375 | 93363.3 | 3.2037 | 60% |
| 0xb33 | 109372 | 109398 | 109384 | 3.20048 | 70% |
| 0xccc | 125358 | 125381 | 125369 | 3.20601 | 80% |
| 0xe66 | 141377 | 141399 | 141388 | 3.19712 | 90% |




TEST #6K: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

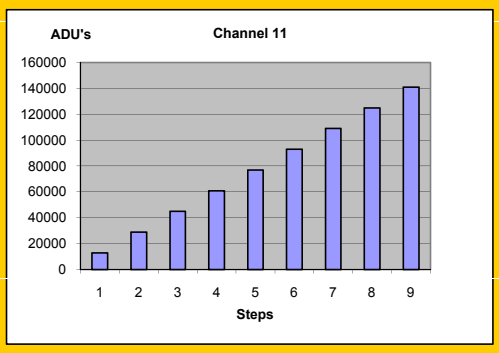
| BrdTst6_006 / Channel 10 | | | | | |
|---|---|---|---|---|---|
| OFFSET DAC VALUE | Min Pix Value | Max Pix Value | Mean Pix Value | Std. Dev. | Remarks |
| 0x19a | 11652 | 11676 | 11662.4 | 3.20202 | 10% |
| 0x333 | 27671 | 27695 | 27682.4 | 3.11876 | 20% |
| 0x4cc | 43691 | 43714 | 43702.4 | 3.10383 | 30% |
| 0x666 | 59747 | 59771 | 59760.5 | 3.08575 | 40% |
| 0x800 | 75807 | 75829 | 75818.7 | 3.11978 | 50% |
| 0x999 | 91830 | 91853 | 91841.7 | 3.08027 | 60% |
| 0xb33 | 107887 | 107911 | 107900 | 3.13964 | 70% |
| 0xccc | 123912 | 123937 | 123924 | 3.05661 | 80% |
| 0xe66 | 139972 | 139995 | 139984 | 3.20143 | 90% |




TEST #6L: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

| BrdTst6_006 / Channel 11 | | | | | |
|---|---|---|---|---|---|
| OFFSET DAC VALUE | Min Pix Value | Max Pix Value | Mean Pix Value | Std. Dev. | Remarks |
| 0x19a | 12961 | 12983 | 12972.5 | 3.19679 | 10% |
| 0x333 | 28945 | 28966 | 28955.9 | 3.16649 | 20% |
| 0x4cc | 44931 | 44954 | 44942.9 | 3.20748 | 30% |
| 0x666 | 60953 | 60977 | 60966.2 | 3.15126 | 40% |
| 0x800 | 76984 | 77009 | 76995 | 3.20844 | 50% |
| 0x999 | 92971 | 92996 | 92983.2 | 3.1665 | 60% |
| 0xb33 | 108992 | 109018 | 109006 | 3.25692 | 70% |
| 0xccc | 124985 | 125009 | 124996 | 3.22931 | 80% |
| 0xe66 | 141007 | 141030 | 141019 | 3.27251 | 90% |




Stage 13. Other Bit Tests. Table 11

| | | | | |
|---|---|---|---|---|
| Electronic Serial Number | 0xDB8F85 | | Board Serial Number | 23 |
| Firmware Version | 0x193 | | Name Of Person Testing | S. Holm |
| Ident Register | 0x502 | | Board passed Functional Tests | YES |