DES 12 Channel Board - Functional Tests: CCD Acquisition Board Revision 1.0

Stage 1. Preparation of documentation and configuration settings - Table 1.

Board Part Number	8		Board Serial Number	0xDB8F7A
Date Of Tests	August 2010		Name Of Person Testing	S. Holm
Suggested Filename To Save	CCDACQ_12Ch_REPORT_BOARD12.xl		Sequence number: Test	

Stage 3. Power plane short test - Table 2.

Supply Name	Short test to ground: Impedance to ground	Test Point	
+1.2VD	62.50	TP43	~50 ohms
+1.8VD	1.3M	TPB12	> 1K ohm
+2.5VD	16K	TPB11	> 1K ohm
+3.3VD	171.00	D13	> 1K ohm
+5VD	3k	D14	> 1K ohm
+5VA	4M	C267	> 1K ohm
-5VA	300K	C270	> 1K ohm
+15VA	500K	C288	> 1K ohm
-15VA	500K	C282	> 1K ohm
-28VA	2.5M	C307	> 1K ohm

Stage 4. Firmware programming tests - Table 3.

JTAG Order	Designator	Device	Load File	Check Sum or User Code
1	U122	XCF08PFS48C PROM	CcdAcqFpgaV41.mcs	0014ef670
2	U114	Spartan3 XC3S2000 FPGA	ccdacqfpgav41.bit	5102801

Stage 5. Power Consumption - Table 4.

Supply Name	Power Supply Consumption: Measured Voltage at test point	Measured Current on power supply	Test Point	
+1.2VD	1.20	N/A	TP43	
+1.8VD	1.80	N/A	TPB12	
+2.5VD	2.50	N/A	TPB11	
+3.3VD	3.29	0.24	D13	
+5VD	5.20	0.15	D14	
+5VA	4.92	0.55	C267	
-5VA	-5.01	0.43	C270	
+15VA	14.92	0.55	C288	
-15VA	-14.93	0.4	C282	
-28VA	-27.89	0.229	C307	
Vref 0+	10.04	N/A	R534	Vsub+ Reference(+10v)
Vref 0-	-2.52	N/A	R525	Vsub - Reference(-2.5v)
Vref Offset	2.50	N/A	R573	ADC Offset Reference(+2.5v)
Vclamp	1.88	N/A	VIA	ADC Clamp Voltage(+1.8v)
ADC Ref.	2.50	N/A	VIA	ADC Reference Voltage(+2.5v)
Vref 1+	2.50	N/A	R537	Vru and Vrl + Reference(+2.5v)
Vref 1-	-10.11	N/A	R535	Vru and Vrl - Reference(-10v)
Vref 2+	5.00	N/A	R563	Vog + Reference(+5v)
Vref 2-	-2.52	N/A	R555	Vog - Reference(-2.5v)
Vref 3+	2.50	N/A	R543	Vdd + Reference(+2.5v)
Vref 3-	-10.03	N/A	R571	Vdd - Reference(-10v)

Power Dissipation:
27.0 Watts

~27 watts +/- 5%

Stage 7. Basic Bus Transactions - **D**igital **Register** Tests - Table 5.

Register name	Put an X on any bit that has an error: 31-24 23-16 15-08 07-00	Function	Test name: Pattern	Walking 0's	Walking 1's
CDS Control	00000000 00000000	16 bit R/W			
Digital Output	00000000 00000000 00000000 00000000	32 bit R/W			
ADC Config.	0000 00000000	12 bit R/W			
Offset DAC	0000 00000000	12 bit R/W			
Bias DAC	0000 00000000	12 bit R/W			
Telemetry Config.	0000	4 bit R/W			
Auxilary Config.	00 00000000	10 bit R/W			
Redirect	0000	4 bit R/W			
Pixel Transfer	00000000	8 bit R/W			
Micro SEQ	00000000 00000000	16 bit R/W			
RAM Buffer	00000000 00000000	16 bit R/W			
LED Control	0000	4 bit R/W			
Control	00000000 00000000	16 bit R/W			
All Register Test	00000000 00000000 00000000 00000000	16 bit R/W	**Passed**	**Passed**	**Passed**

Stage 8. Bias Voltage settings and output enables testing - Table 8

DAC Value	Bias Voltage Test Data 410	2048	3686	50% rms Noise	10-90% Rise Time			
Signal	volts	volts	volts	uV	millisec.	Fanout Brd	Slope	Offset
Vru 0	-13.28	-5.71	1.85	<10	1	BIAS 3	216.52	3285.07
Vru 1	-13.28	-5.71	1.85	<10	1	BIAS 4	216.52	3285.07
Vru 2	-13.28	-5.71	1.85	<10	1	BIAS 5	216.52	3285.07
Vru 3	-13.28	-5.71	1.85	<10	1	BIAS 6	216.52	3285.07
Vru 4	-13.28	-5.71	1.85	<10	1	BIAS 7	216.52	3285.07
Vru 5	-13.28	-5.71	1.85	<10	1	BIAS 8	216.52	3285.07
Vru 6	-13.28	-5.71	1.85	NA	NA	BIAS 9	216.52	3285.07
Vru 7	-13.28	-5.71	1.85	NA	NA	BIAS 10	216.52	3285.07
Vrl 0	-13.28	-5.71	1.85	<10	1	BIAS 11	216.52	3285.07
Vrl 1	-13.28	-5.71	1.85	<10	1	BIAS 12	216.52	3285.07
Vrl 2	-13.28	-5.71	1.85	<10	1	BIAS 13	216.52	3285.07
Vrl 3	-13.28	-5.71	1.85	<10	1	BIAS 14	216.52	3285.07
Vrl 4	-13.28	-5.71	1.85	<10	1	BIAS 15	216.52	3285.07
Vrl 5	-13.28	-5.71	1.85	<10	1	BIAS 16	216.52	3285.07
Vrl 6	-13.28	-5.71	1.85	NA	NA	BIAS 17	216.52	3285.07
Vrl 7	-13.28	-5.71	1.85	NA	NA	BIAS 18	216.52	3285.07
Vog 0	-1.77	1.24	4.25	<10	1	BIAS 19	544.19	1373.21
Vog 1	-1.77	1.24	4.25	<10	1	BIAS 20	544.19	1373.21
Vog 2	-1.77	1.24	4.25	<10	1	BIAS 21	544.19	1373.21
Vog 3	-1.77	1.24	4.25	<10	1	BIAS 22	544.19	1373.21
Vog 4	-1.77	1.24	4.25	<10	1	BIAS 23	544.19	1373.21
Vog 5	-1.77	1.24	4.25	<10	1	BIAS 24	544.19	1373.21
Vog 6	-1.77	1.24	4.25	NA	NA	BIAS 25	544.19	1373.21
Vog 7	-1.77	1.24	4.25	NA	NA	BIAS 26	544.19	1373.21
Vdd 0	-22.22	-9.57	3.09	<10	20	BIAS 27	129.43	3286.26
Vdd 1	-22.20	-9.56	3.09	<10	20	BIAS 28	129.54	3285.95
Vdd 2	-22.15	-9.54	3.09	<10	20	BIAS 29	129.79	3285.37
Vdd 3	-22.19	-9.56	3.09	<10	20	BIAS 30	129.59	3286.00
Vdd 4	-22.22	-9.57	3.09	<10	20	BIAS 21	129.43	3286.26
Vdd 5	-22.25	-9.58	3.09	<10	20	BIAS 32	129.28	3286.52
Vdd 6	-22.20	-9.56	3.09	NA	NA	BIAS 33	129.54	3285.95
Vdd 7	-22.13	-9.53	3.09	NA	NA	BIAS 34	129.90	3285.05

Vru	Slope		Offset
Mean	216.52	Mean	3285.07
Stdev	2.842E-14	Stdev	4.54747E-13
Average	216.52343	Average	3285.07054
	Dac #	Average voltage	
	0	-15.0	
	4095	3.7	

Vrl	Slope		Offset
Mean	216.52	Mean	3285.07
Stdev	2.842E-14	Stdev	4.54747E-13
Average	216.52343	Average	3285.07054
	Dac #	Average voltage	
	0	-15.2	
	4095	3.7	

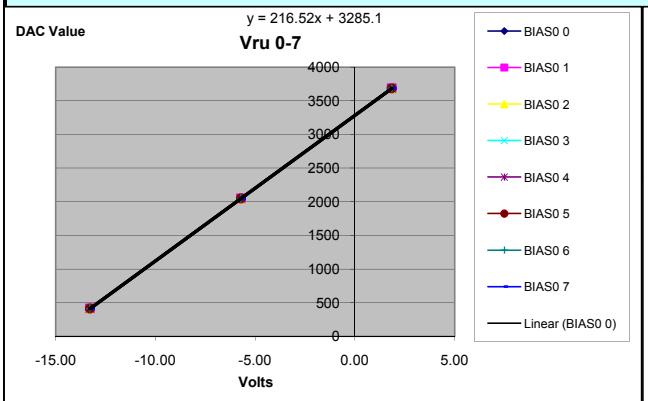
Vog	Slope		Offset
Mean	544.19	Mean	1373.21
Stdev	0	Stdev	2.27374E-13
Average	544.18605	Average	1373.209302
	Dac #	Average voltage	
	0	-2.5	
	4095	5.0	

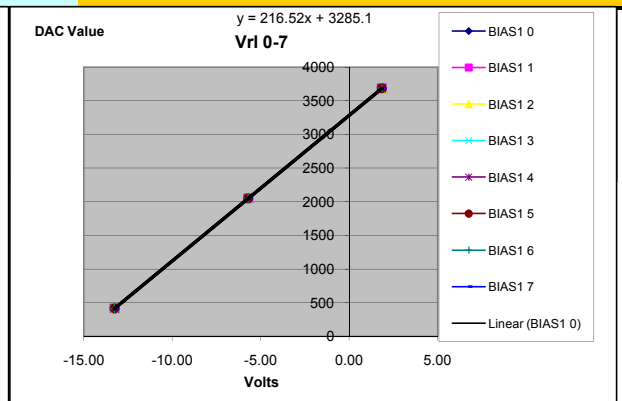
Vdd	Slope		Offset
Mean	129.56	Mean	3285.92
Stdev	0.1866289	Stdev	0.45536592
Average	129.56324	Average	3285.919531
	Dac #	Average voltage	
	0	-25.4	
	4095	6.3	

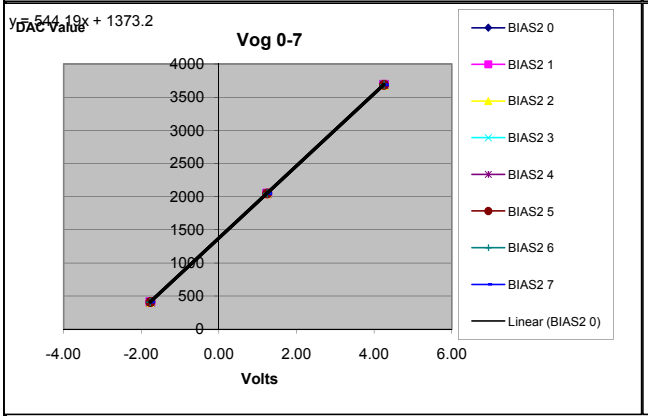
Notes and Observations

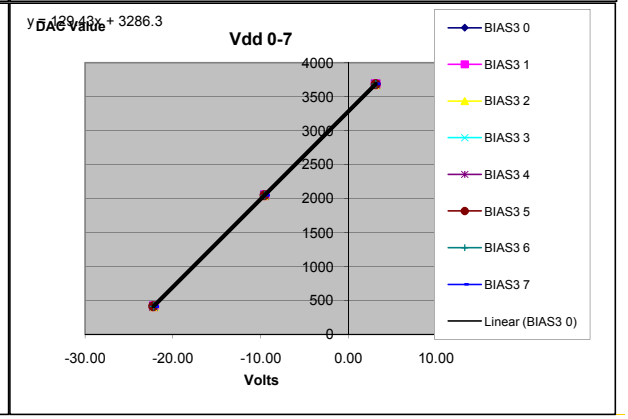
Checked for oscillations using a Agilent Oscilloscpe on AC.**OK**

average min & max voltages
(dac# -offset)/slope=voltage









Stage 8B. Telemetry System Tests - Table 7 (Bias Telemetry Tests)

DAC Value	410	3686	Bias Signals Set Volts		Resolved Values for Telemetry Channel	
	Telemetry Return Values					
Signal	10%	90%	10%	90%	Slope	Offset
Vru 0	-1771	421	-13.28	1.85	144.8777	152.98
Vru 1	-1774	420	-13.28	1.85	145.0099	151.73
Vru 2	-1775	420	-13.28	1.85	145.0760	151.61
Vru 3	-1775	420	-13.28	1.85	145.0760	151.61
Vru 4	-1774	421	-13.28	1.85	145.0760	152.61
Vru 5	-1771	421	-13.28	1.85	144.8777	152.98
Vru 6	-1774	420	-13.28	1.85	145.0099	151.73
Vru 7	-1774	420	-13.28	1.85	145.0099	151.73
Vrl 0	-1773	421	-13.28	1.85	145.0099	152.73
Vrl 1	-1769	421	-13.28	1.85	144.7455	153.22
Vrl 2	-1770	421	-13.28	1.85	144.8116	153.10
Vrl 3	-1772	421	-13.28	1.85	144.9438	152.85
Vrl 4	-1769	421	-13.28	1.85	144.7455	153.22
Vrl 5	-1770	421	-13.28	1.85	144.8116	153.10
Vrl 6	-1776	421	-13.28	1.85	145.2082	152.36
Vrl 7	-1775	421	-13.28	1.85	145.1421	152.49
Vog 0	-365	868	-1.77	4.25	204.8173	-2.47
Vog 1	-365	868	-1.77	4.25	204.8173	-2.47
Vog 2	-365	868	-1.77	4.25	204.8173	-2.47
Vog 3	-365	868	-1.77	4.25	204.8173	-2.47
Vog 4	-365	868	-1.77	4.25	204.8173	-2.47
Vog 5	-365	868	-1.77	4.25	204.8173	-2.47
Vog 6	-365	867	-1.77	4.25	204.6512	-2.77
Vog 7	-365	867	-1.77	4.25	204.6512	-2.77
Vdd 0	-1769	572	-22.22	3.09	92.4931	286.20
Vdd 1	-1763	571	-22.20	3.09	92.2894	285.83
Vdd 2	-1760	571	-22.15	3.09	92.3534	285.63
Vdd 3	-1763	571	-22.19	3.09	92.3259	285.71
Vdd 4	-1768	572	-22.22	3.09	92.4536	286.32
Vdd 5	-1771	572	-22.25	3.09	92.4625	286.29
Vdd 6	-1764	571	-22.20	3.09	92.3290	285.70
Vdd 7	-1753	571	-22.13	3.09	92.1491	286.26

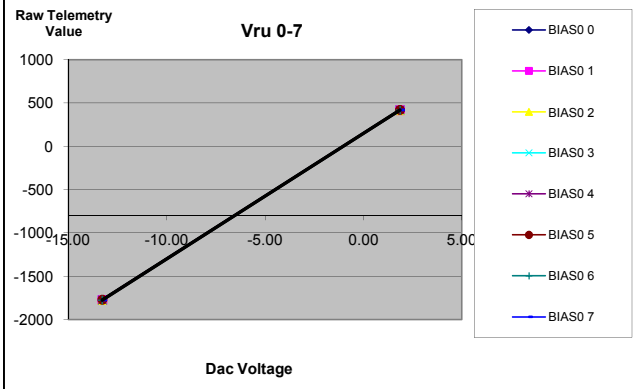
AVERAGE

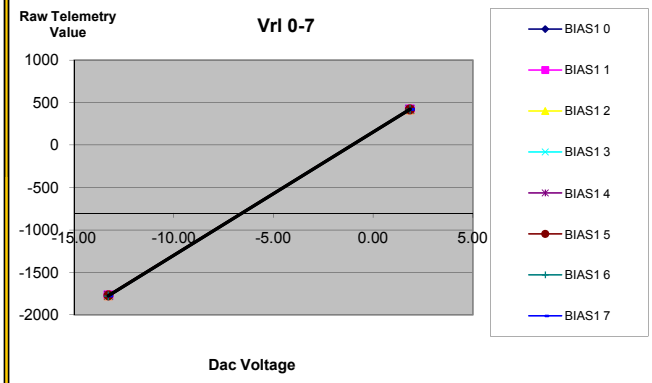
Vru	Slope		Offset
Mean	145.00	Mean	152.12
Stdev	0.0770603	Stdev	0.5787408

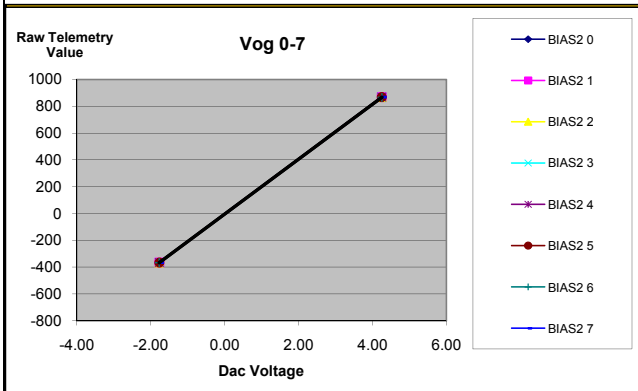
Vrl	Slope		Offset
Mean	144.93	Mean	152.88
Stdev	0.1676948	Stdev	0.3102354

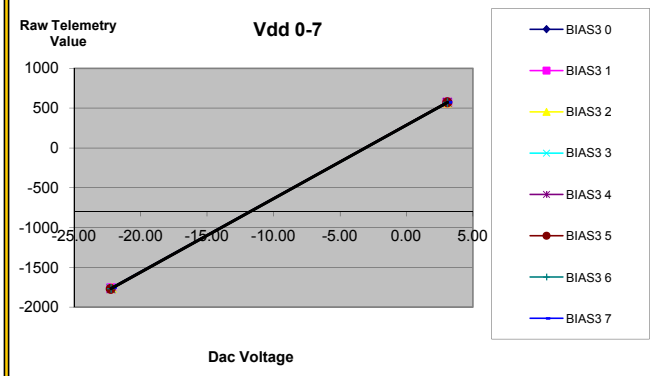
Vog	Slope		Offset
Mean	204.78	Mean	-2.55
Stdev	0.071929	Stdev	0.1273144

Vdd	Slope		Offset
Mean	92.36	Mean	285.99
Stdev	0.1051974	Stdev	0.280738









Stage 8C. Bias Voltage output enables testing - Table 8

Place a line through Bias Voltage name if enable/disable switch works

Vru 0	Vru 1	Vru 2	Vru 3	Vru 4	Vru 5
Vrl 0	Vrl 1	Vrl 2	Vrl 3	Vrl 4	Vrl 5
Vog 0	Vog 1	Vog 2	Vog 3	Vog 4	Vog 5
Vdd 0	Vdd 1	Vdd 2	Vdd 3	Vdd 4	Vdd 5

Stage 9. Vsub and Heater Control testing - Table 9

DAC Value	Vsub Measured Voltage Test Data 10%	50%	90%
Signal	volts	volts	volts
Vsub - rate	-1.26	3.75	8.78
Vsub - Limit	-1.26	3.75	8.78
Vsub0	0.00	0.00	0.00
	Vsub Enable Bit - pass		

DAC Value	Telemetery Readback Test Data 10%	50%	90%
Signal	dec	dec	dec
Vbias 0	154	264	439
Vbias 1	-30	695	1421
RTD1	220	NA	NA
RTD2	248	NA	NA
RTD3	275	NA	NA
RTD4	301	NA	NA
RTD5	328	NA	NA
RTD6	350	NA	NA
Reference 4096	836	NA	NA
eference buffere	836	NA	NA

Stage 10. Video Offset DAC Tests - Table 10.

	DAC Value 410				DAC Value 2048				DAC Value 3686			
ADC	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU
0	0.250	NA	NA	17213	1.250		NA	81188	2.250	NA	500ms	145160
1	0.250	NA	NA	16840	1.250		NA	80903	2.250	NA	500ms	144971
2	0.250	NA	NA	16930	1.250		NA	80932	2.250	NA	500ms	144917
3	0.250	NA	NA	17160	1.250		NA	81190	2.250	NA	500ms	145213
4	0.250	NA	NA	17108	1.250		NA	81105	2.250	NA	500ms	145086
5	0.250	NA	NA	17035	1.250		NA	81082	2.250	NA	500ms	145135
6	0.250	NA	NA	17135	1.250		NA	81234	2.250	NA	500ms	145145
7	0.250	NA	NA	17190	1.250		NA	81148	2.250	NA	500ms	145044
8	0.250	NA	NA	17095	1.250		NA	81109	2.250	NA	500ms	145082
9	0.250	NA	NA	16975	1.250		NA	81102	2.250	NA	500ms	145026
10	0.250	NA	NA	17132	1.250		NA	81146	2.250	NA	500ms	145148
11	0.250	NA	NA	17074	1.250		NA	81112	2.250	NA	500ms	145206

ADC	DC Volts		Data Set		
Channel	Slope	Offset	410	2048	3686
0	1638.000	0.500	0.250	1.250	2.250
1	1638.000	0.500	0.250	1.250	2.250
2	1638.000	0.500	0.250	1.250	2.250
3	1638.000	0.500	0.250	1.250	2.250
4	1638.000	0.500	0.250	1.250	2.250
5	1638.000	0.500	0.250	1.250	2.250
6	1638.000	0.500	0.250	1.250	2.250
7	1638.000	0.500	0.250	1.250	2.250
8	1638.000	0.500	0.250	1.250	2.250
9	1638.000	0.500	0.250	1.250	2.250
10	1638.000	0.500	0.250	1.250	2.250
11	1638.000	0.500	0.250	1.250	2.250

(dac# -offset)/slope=Voltage

ADC	ADU's		Data Set		
Channel	Slope	Offset	410	2048	3686
0	0.026	-30.74	17213	81188	145160
1	0.026	-20.54	16840	80903	144971
2	0.026	-23.42	16930	80932	144917
3	0.026	-29.04	17160	81190	145213
4	0.026	-28.00	17108	81105	145086
5	0.026	-25.62	17035	81082	145135
6	0.026	-27.89	17135	81234	145330
7	0.026	-30.27	17190	81148	145103
8	0.026	-27.47	17095	81109	145118
9	0.026	-23.57	16975	81102	145232
10	0.026	-28.37	17132	81146	145161
11	0.026	-26.76	17074	81112	145146

(dac# -offset)/slope=ADU

Notes and Observations

Checked for oscillations using a Agilent Oscilloscope on AC. OK

Stage 11. CDS Control Functions and Video Channel Performanc

TEST #1: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit is held static. The purpose of this test is to verify the correct operation of the ADC devices and measure the noise of the Offset voltage generators, ADC buffer amplifiers and ADC devices

Noise Test 1

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	81187	8.12E+04	81196.4	2.28565
CH 1	80904	8.09E+04	80912.6	2.24097
CH 2	80929	8.09E+04	80935.9	2.26826
CH 3	81187	8.12E+04	81194.4	2.37763
CH 4	81105	8.11E+04	81113.5	2.23387
CH 5	81082	8.11E+04	81091.1	2.40753
CH 6	81235	8.13E+04	81244.8	2.40589
CH 7	81148	8.12E+04	81156.7	2.39011
CH 8	81109	8.11E+04	81117.3	2.27567
CH 9	81101	81118	81109.1	2.53545
CH 10	81145	81163	81153.6	2.38714
CH 11	81112	81129	81120.3	2.36535

TEST #2: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the invert/non-invert and the DC Restore switches are held static.

Noise Test 2

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76564	7.66E+04	76575.8	2.82937
CH 1	76540	7.66E+04	76550.4	2.77858
CH 2	76338	7.64E+04	76347.7	2.87163
CH 3	76845	7.69E+04	76855.6	2.84793
CH 4	76343	7.64E+04	76353.1	2.90673
CH 5	76655	7.67E+04	76664.9	2.88902
CH 6	77210	7.72E+04	77219.7	2.81268
CH 7	76887	7.69E+04	76896.8	2.7529
CH 8	76701	7.67E+04	76711.2	2.84507
CH 9	76968	76989	76978.4	2.94901
CH 10	76925	76949	76937	3.11529
CH 11	76833	76852	76841.8	2.97403

TEST #3: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the DC Restore switch is held static.

Noise Test 3

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76586	7.66E+04	76596.9	3.0321
CH 1	76548	7.66E+04	76559.1	3.10641
CH 2	76343	7.64E+04	76355.8	2.89561
CH 3	76844	7.69E+04	76854.2	3.12259
CH 4	76353	7.64E+04	76362.6	3.00941
CH 5	76654	7.67E+04	76667.7	3.07971
CH 6	77211	7.72E+04	77223.5	3.06606
CH 7	76895	7.69E+04	76904.5	3.01466
CH 8	76712	7.67E+04	76722.5	2.87003
CH 9	76972	76993	76983.4	3.1409
CH 10	76952	76973	76962.2	2.92824
CH 11	76838	76860	76848.2	3.10102

TEST #4: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition.

Noise Test 4

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76612	7.66E+04	76622.6	3.14596
CH 1	76567	7.66E+04	76579.4	3.1567
CH 2	76368	7.64E+04	76379.9	3.26245
CH 3	76844	7.69E+04	76856	3.22535
CH 4	76414	7.64E+04	76425.6	3.12446
CH 5	76662	7.67E+04	76675.1	3.30686
CH 6	77226	7.72E+04	77236.7	3.08391
CH 7	76873	7.69E+04	76884.7	3.30517
CH 8	76764	7.68E+04	76775.4	3.02037
CH 9	76920	76942	76931.4	3.27704
CH 10	76991	77015	77003.1	3.23279
CH 11	76819	76841	76830.2	3.1867

TEST #5: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the circuitry set to high GAIN.

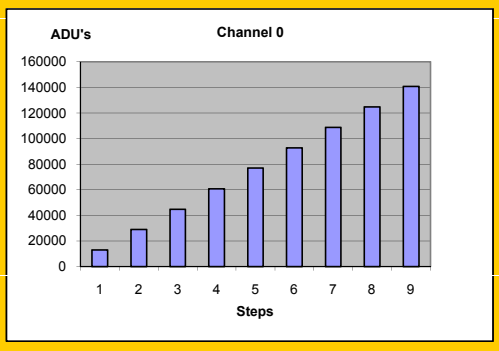
Noise Test 5

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76659	7.67E+04	76673	3.57855
CH 1	76599	7.66E+04	76611.1	3.67244
CH 2	76414	7.64E+04	76426.2	3.66529
CH 3	76868	7.69E+04	76883.3	3.68957
CH 4	76454	7.65E+04	76468.9	3.62909
CH 5	76681	7.67E+04	76695.7	3.71487
CH 6	77237	7.73E+04	77251.7	3.77349
CH 7	76895	7.69E+04	76909	3.6274
CH 8	76828	7.69E+04	76841.1	3.59315
CH 9	76940	76967	76951.8	3.61975
CH 10	77074	77102	77087.1	3.62791
CH 11	76835	76861	76847.9	3.76986

TEST #6A: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

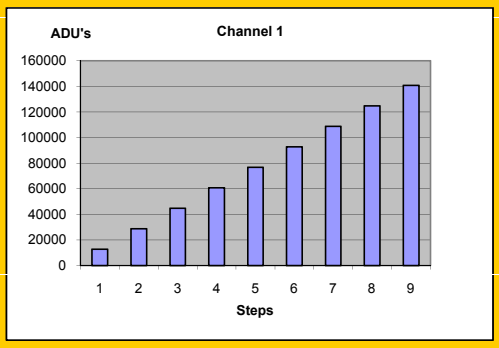
BrdTst6_006 / Channel 0					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12911	12933	12921.7	3.16925	10%
0x333	28884	28907	28897	3.16804	20%
0x4cc	44855	44878	44866.5	3.17418	30%
0x666	60868	60891	60879.9	3.16446	40%
0x800	76881	76902	76891.5	3.19418	50%
0x999	92854	92877	92864.8	3.18985	60%
0xb33	108873	108896	108883	3.09496	70%
0xccc	124847	124867	124857	3.20807	80%
0xe66	140861	140884	140872	3.25055	90%



TEST #6B: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

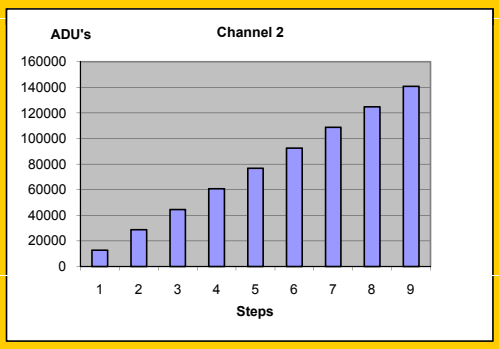
BrdTst6_006 / Channel 1					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12733	12755	12743.8	3.17838	10%
0x333	28730	28751	28741.1	3.19186	20%
0x4cc	44721	44743	44732.6	3.14467	30%
0x666	60757	60779	60767.9	3.15017	40%
0x800	76792	76814	76802.2	3.1545	50%
0x999	92785	92810	92799.1	3.16448	60%
0xb33	108828	108850	108838	3.11692	70%
0xccc	124820	124842	124831	3.11434	80%
0xe66	140857	140881	140868	3.09348	90%



TEST #6C: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

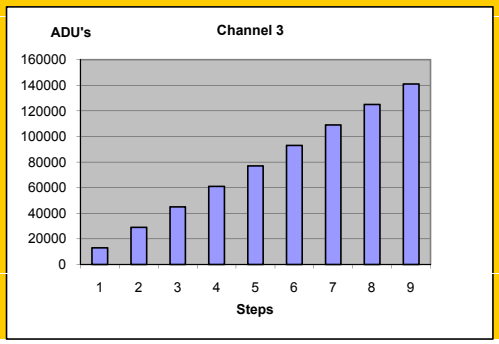
BrdTst6_006 / Channel 2					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12654	12678	12665	3.20966	10%
0x333	28634	28656	28644.1	3.0294	20%
0x4cc	44611	44633	44622.6	3.13777	30%
0x666	60627	60650	60639.4	3.10385	40%
0x800	76642	76666	76655.3	3.15982	50%
0x999	92623	92645	92634	3.13201	60%
0xb33	108643	108665	108655	3.15573	70%
0xccc	124626	124648	124637	3.14052	80%
0xe66	140644	140667	140656	3.26937	90%



TEST #6D: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

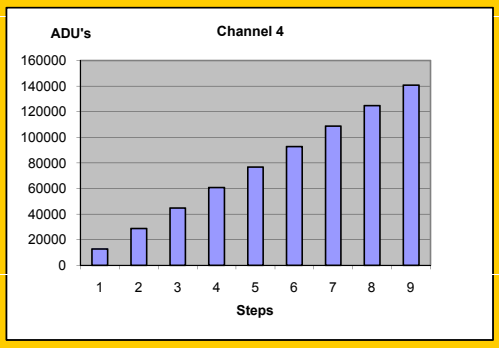
BrdTst6_006 / Channel 3					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13058	13082	13070.1	3.26697	10%
0x333	29046	29068	29057.5	3.20466	20%
0x4cc	45033	45054	45042.8	3.22144	30%
0x666	61057	61082	61068.4	3.17286	40%
0x800	77080	77102	77091	3.01575	50%
0x999	93066	93089	93077.7	3.21312	60%
0xb33	109095	109117	109106	3.22651	70%
0xccc	125080	125105	125093	3.02019	80%
0xe66	141109	141134	141121	3.21846	90%



TEST #6E: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

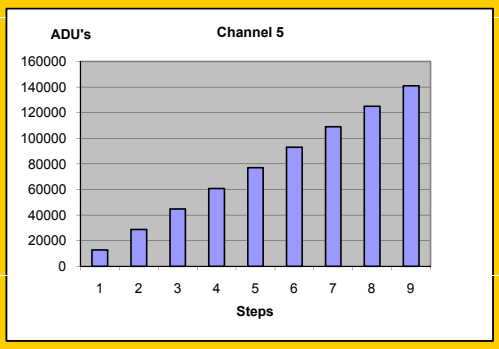
BrdTst6_006 / Channel 4					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12695	12720	12708.8	3.26852	10%
0x333	28676	28697	28686.5	3.13189	20%
0x4cc	44654	44677	44663.4	3.14411	30%
0x666	60668	60691	60678.9	3.08391	40%
0x800	76683	76705	76693.5	3.06094	50%
0x999	92662	92685	92672.6	3.13811	60%
0xb33	108684	108706	108694	3.05228	70%
0xccc	124662	124684	124674	3.0628	80%
0xe66	140678	140703	140691	3.05077	90%



TEST #6F: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

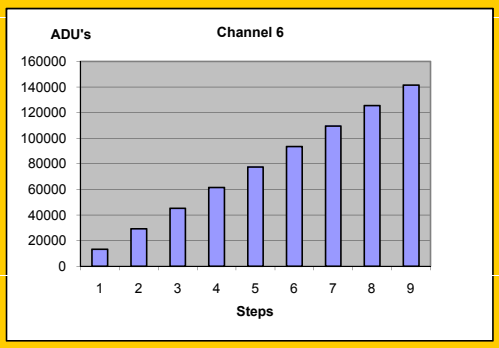
BrdTst6_006 / Channel 5					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12846	12870	12858.2	3.27404	10%
0x333	28838	28861	28849.6	3.30214	20%
0x4cc	44833	44856	44843.4	3.23538	30%
0x666	60860	60887	60872.5	3.274	40%
0x800	76891	76914	76902.9	3.28381	50%
0x999	92886	92910	92896.8	3.26924	60%
0xb33	108918	108941	108930	3.27937	70%
0xccc	124913	124936	124925	3.23018	80%
0xe66	140946	140968	140957	3.20372	90%



TEST #6G: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

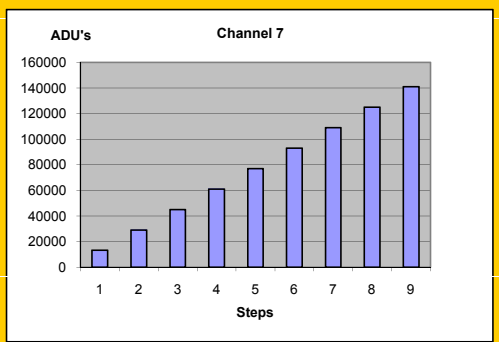
BrdTst6_006 / Channel 6					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13353	13380	13368.2	3.25059	10%
0x333	29362	29387	29374.4	3.1713	20%
0x4cc	45370	45391	45379.9	3.01836	30%
0x666	61411	61436	61423.1	3.20553	40%
0x800	77450	77474	77462.8	3.31899	50%
0x999	93460	93480	93470.1	3.14884	60%
0xb33	109505	109529	109516	3.26476	70%
0xccc	125510	125532	125522	3.20858	80%
0xe66	141553	141579	141567	3.1925	90%



TEST #6H: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

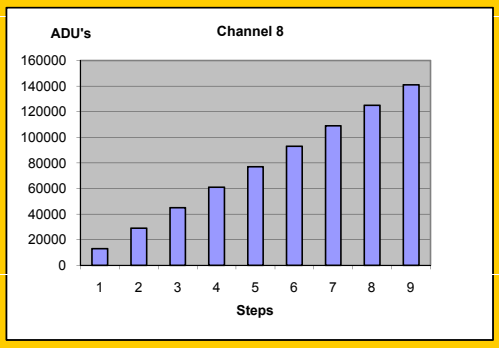
BrdTst6_006 / Channel 7					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13146	13170	13156.6	3.06733	10%
0x333	29112	29138	29127.6	3.28144	20%
0x4cc	45084	45105	45093.3	3.10721	30%
0x666	61091	61114	61101.9	3.21791	40%
0x800	77099	77121	77110.2	3.23739	50%
0x999	93069	93092	93079.7	3.16327	60%
0xb33	109080	109103	109091	2.93176	70%
0xccc	125047	125069	125058	3.15572	80%
0xe66	141058	141086	141069	3.2418	90%



TEST #6I: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

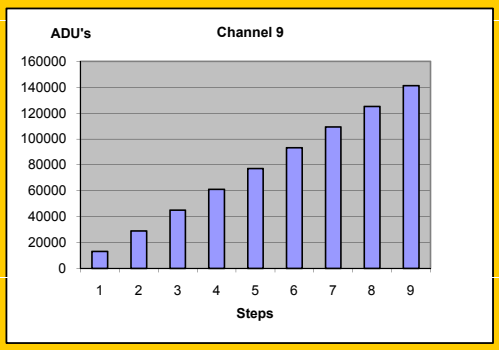
BrdTst6_006 / Channel 8					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13002	13025	13012.6	3.32553	10%
0x333	28986	29008	28996.6	3.06637	20%
0x4cc	44966	44986	44976.3	3.06493	30%
0x666	60989	61012	60999.8	3.06124	40%
0x800	77009	77033	77020.6	3.06814	50%
0x999	92990	93013	93001.7	3.1297	60%
0xb33	109017	109039	109027	3.21166	70%
0xccc	124999	125022	125010	3.1466	80%
0xe66	141023	141045	141034	3.12278	90%



TEST #6J: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

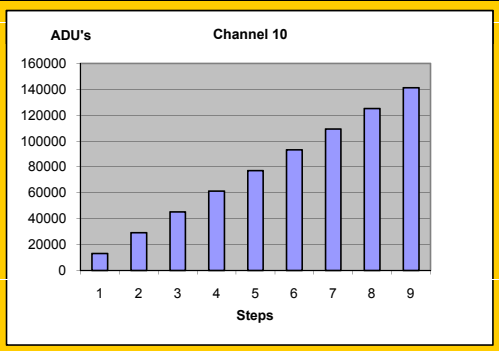
BrdTst6_006 / Channel 9					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13030	13054	13041.7	3.24885	10%
0x333	29042	29067	29056.7	3.12527	20%
0x4cc	45055	45077	45066.9	3.29633	30%
0x666	61108	61129	61118.5	3.32114	40%
0x800	77155	77180	77168.1	3.23162	50%
0x999	93170	93193	93182.1	3.29493	60%
0xb33	109227	109251	109238	3.11293	70%
0xccc	125237	125262	125250	3.28564	80%
0xe66	141293	141316	141305	3.29111	90%



TEST #6K: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

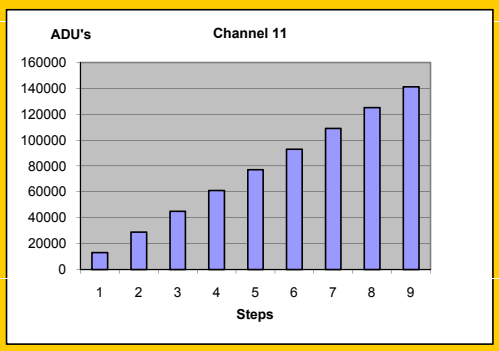
BrdTst6_006 / Channel 10					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13226	13248	13237.7	3.23441	10%
0x333	29209	29232	29219.7	2.98178	20%
0x4cc	45193	45218	45205.5	3.14101	30%
0x666	61215	61237	61226.1	3.17306	40%
0x800	77236	77260	77248.7	3.2166	50%
0x999	93220	93243	93232.7	3.04738	60%
0xb33	109247	109270	109259	3.2339	70%
0xccc	125234	125256	125245	3.29165	80%
0xe66	141259	141279	141269	3.06098	90%



TEST #6L: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

BrdTst6_006 / Channel 11					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13027	13051	13039.4	3.34403	10%
0x333	29015	29041	29029	3.28316	20%
0x4cc	45006	45030	45018.2	3.30828	30%
0x666	61034	61059	61045	3.15087	40%
0x800	77060	77087	77073.5	3.29173	50%
0x999	93054	93078	93065.2	3.24792	60%
0xb33	109083	109108	109096	3.28447	70%
0xccc	125074	125098	125087	3.32669	80%
0xe66	141103	141129	141116	3.3314	90%



Stage 13. Other Bit Tests. Table 11

Electronic Serial Number	0xDB8F7A		Board Serial Number	8
Firmware Version	0x193		Name Of Person Testing	S. Holm
Ident Register	0x502		Board passed Functional Tests	YES