DES 12 Channel Board - Functional Tests: CCD Acquisition Board Revision 1.0

Stage 1. Preparation of documentation and configuration settings - Table 1.

Board Part Number	12	Board Serial Number	0xDB6F9F
Date Of Tests	July 2010	Name Of Person Testing	S. Holm
Suggested Filename To Save	CCDACQ_12Ch_REPORT_BOARD12.xl	Sequence number: Test	

Stage 3. Power plane short test - Table 2.

Supply Name	Short test to ground: Impedance to ground	Test Point	
+1.2VD	41.30	TP43	~50 ohms
+1.8VD	1.2M	TPB12	> 1K ohm
+2.5VD	17K	TPB11	> 1K ohm
+3.3VD	5.8K	D13	> 1K ohm
+5VD	18K	D14	> 1K ohm
+5VA	4M	C267	> 1K ohm
-5VA	300K	C270	> 1K ohm
+15VA	500K	C288	> 1K ohm
-15VA	500K	C282	> 1K ohm
-28VA	2.5M	C307	> 1K ohm

Stage 4. Firmware programming tests - Table 3.

JTAG Order	Designator	Device	Load File	Check Sum or User Code
1	U122	XCF08PFS48C PROM	CcdAcqFpgaV41.mcs	0014ef670
2	U114	Spartan3 XC3S2000 FPGA	ccdacqfpgav41.bit	5102801

Stage 5. Power Consumption - Table 4.

Supply Name	Power Supply Consumption: Measured Voltage at test point	Measured Current on power supply	Test Point	
+1.2VD	1.20	N/A	TP43	
+1.8VD	1.80	N/A	TPB12	
+2.5VD	2.51	N/A	TPB11	
+3.3VD	3.30	0.214	D13	
+5VD	5.20	0.153	D14	
+5VA	5.01	0.657	C267	
-5VA	-5.01	0.437	C270	
+15VA	15.01	0.561	C288	
-15VA	-15.08	0.404	C282	
-28VA	-28.00	0.203	C307	
Vref 0+	10.02	N/A	R534	Vsub+ Reference(+10v)
Vref 0-	-2.50	N/A	R525	Vsub - Reference(-2.5v)
Vref Offset	2.50	N/A	R573	ADC Offset Reference(+2.5v)
Vclamp	1.88	N/A	VIA	ADC Clamp Voltage(+1.8v)
ADC Ref.	2.50	N/A	VIA	ADC Reference Voltage(+2.5v)
Vref 1+	2.50	N/A	R537	Vru and Vrl + Reference(+2.5v)
Vref 1-	-9.98	N/A	R535	Vru and Vrl - Reference(-10v)
Vref 2+	5.01	N/A	R563	Vog + Reference(+5v)
Vref 2-	-2.50	N/A	R555	Vog - Reference(-2.5v)
Vref 3+	2.50	N/A	R543	Vdd + Reference(+2.5v)
Vref 3-	-10.06	N/A	R571	Vdd - Reference(-10v)

Power Dissipation:
27.2 Watts

~27 watts +/- 5%

Stage 7. Basic Bus Transactions - **D**igital **Register** Tests - Table 5.

Register name	Put an X on any bit that has an error: 31-24	23-16	15-08	07-00	Function	Test name: Pattern	Walking 0's	Walking 1's
CDS Control			00000000	00000000	16 bit R/W			
Digital Output	00000000	00000000	00000000	00000000	32 bit R/W			
ADC Config.			0000	00000000	12 bit R/W			
Offset DAC			0000	00000000	12 bit R/W			
Bias DAC			0000	00000000	12 bit R/W			
Telemetry Config.				0000	4 bit R/W			
Auxilary Config.			00	00000000	10 bit R/W			
Redirect				0000	4 bit R/W			
Pixel Transfer				00000000	8 bit R/W			
Micro SEQ			00000000	00000000	16 bit R/W			
RAM Buffer			00000000	00000000	16 bit R/W			
LED Control				0000	4 bit R/W			
Control			00000000	00000000	16 bit R/W			
All Register Test	00000000	00000000	00000000	00000000	16 bit R/W	**Passed**	**Passed**	**Passed**

Stage 8. Bias Voltage settings and output enables testing - Table 8

DAC Value	410	Bias Voltage Test Data 2048	3686	50% rms Noise	10-90% Rise Time			
Signal	volts	volts	volts	uV	millisec.	Fanout Brd	Slope	Offset
Vru 0	-13.10	-5.61	1.88	<10	1	BIAS 3	218.69	3274.86
Vru 1	-13.10	-5.61	1.88	<10	1	BIAS 4	218.69	3274.86
Vru 2	-13.10	-5.61	1.88	<10	1	BIAS 5	218.69	3274.86
Vru 3	-13.12	-5.62	1.88	<10	1	BIAS 6	218.40	3275.41
Vru 4	-13.10	-5.61	1.88	<10	1	BIAS 7	218.69	3274.86
Vru 5	-13.12	-5.62	1.88	<10	1	BIAS 8	218.40	3275.41
Vru 6	-13.09	-5.62	1.88	NA	NA	BIAS 9	218.84	3275.68
Vru 7	-13.10	-5.61	1.88	NA	NA	BIAS 10	218.69	3274.86
Vrl 0	-13.11	-5.61	1.87	<10	1	BIAS 11	218.69	3276.32
Vrl 1	-13.09	-5.61	1.87	<10	1	BIAS 12	218.98	3276.50
Vrl 2	-13.09	-5.61	1.87	<10	1	BIAS 13	218.98	3276.50
Vrl 3	-13.10	-5.61	1.87	<10	1	BIAS 14	218.84	3276.41
Vrl 4	-13.09	-5.61	1.87	<10	1	BIAS 15	218.98	3276.50
Vrl 5	-13.10	-5.61	1.87	<10	1	BIAS 16	218.84	3276.41
Vrl 6	-13.12	-5.62	1.87	NA	NA	BIAS 17	218.55	3276.96
Vrl 7	-13.12	-5.62	1.87	NA	NA	BIAS 18	218.55	3276.96
Vog 0	-1.75	1.25	4.25	<10	1	BIAS 19	546.00	1365.50
Vog 1	-1.75	1.25	4.25	<10	1	BIAS 20	546.00	1365.50
Vog 2	-1.75	1.25	4.25	<10	1	BIAS 21	546.00	1365.50
Vog 3	-1.75	1.25	4.25	<10	1	BIAS 22	546.00	1365.50
Vog 4	-1.75	1.25	4.25	<10	1	BIAS 23	546.00	1365.50
Vog 5	-1.75	1.25	4.25	<10	1	BIAS 24	546.00	1365.50
Vog 6	-1.75	1.25	4.25	NA	NA	BIAS 25	546.00	1365.50
Vog 7	-1.75	1.25	4.25	NA	NA	BIAS 26	546.00	1365.50
Vdd 0	-22.04	-9.47	3.11	<10	20	BIAS 27	130.26	3281.11
Vdd 1	-21.96	-9.43	3.10	<10	20	BIAS 28	130.73	3280.75
Vdd 2	-22.04	-9.47	3.11	<10	20	BIAS 29	130.26	3281.11
Vdd 3	-22.06	-9.48	3.11	<10	20	BIAS 30	130.15	3281.43
Vdd 4	-22.04	-9.47	3.11	<10	20	BIAS 21	130.26	3281.11
Vdd 5	-22.01	-9.45	3.10	<10	20	BIAS 32	130.47	3281.34
Vdd 6	-21.98	-9.44	3.10	NA	NA	BIAS 33	130.62	3281.07
Vdd 7	-22.01	-9.45	3.11	NA	NA	BIAS 34	130.41	3280.41

Vru	Slope		Offset
Mean	218.64	Mean	3275.10
Stdev	0.1446508	Stdev	0.318575965
Average	218.63692	Average	3275.099098
	Dac #	Average voltage	
	0	-14.0	
	4095	3.8	

Vrl	Slope		Offset
Mean	218.80	Mean	3276.57
Stdev	0.1751772	Stdev	0.231132935
Average	218.80124	Average	3276.568067
	Dac #	Average voltage	
	0	-15.0	
	4095	3.7	

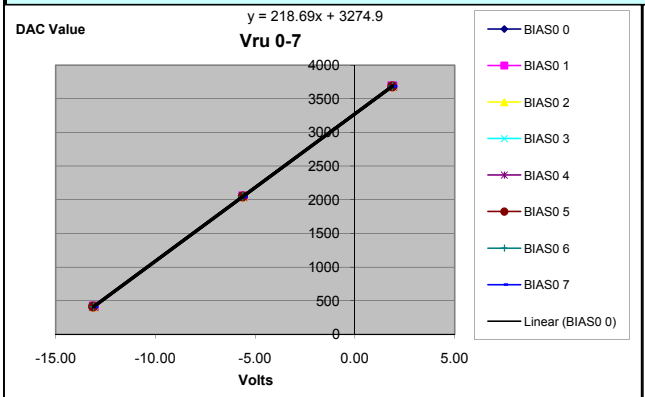
Vog	Slope		Offset
Mean	546.00	Mean	1365.50
Stdev	0	Stdev	0
Average	546	Average	1365.5
	Dac #	Average voltage	
	0	-2.5	
	4095	5.0	

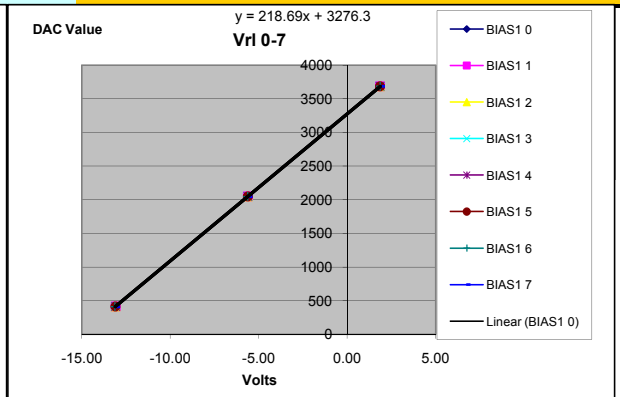
Vdd	Slope		Offset
Mean	130.39	Mean	3281.04
Stdev	0.1871602	Stdev	0.304268265
Average	130.39481	Average	3281.043198
	Dac #	Average voltage	
	0	-25.2	
	4095	6.2	

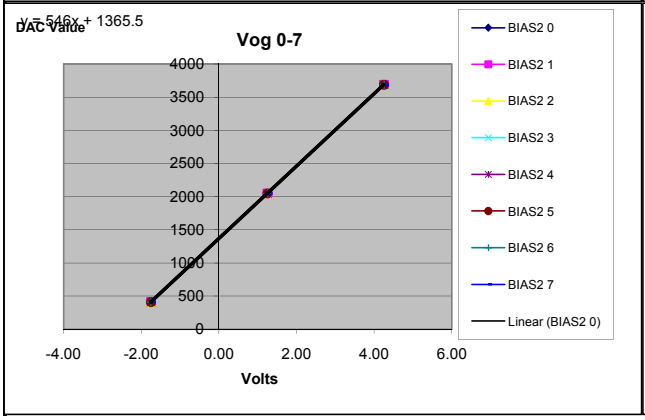
Notes and Observations

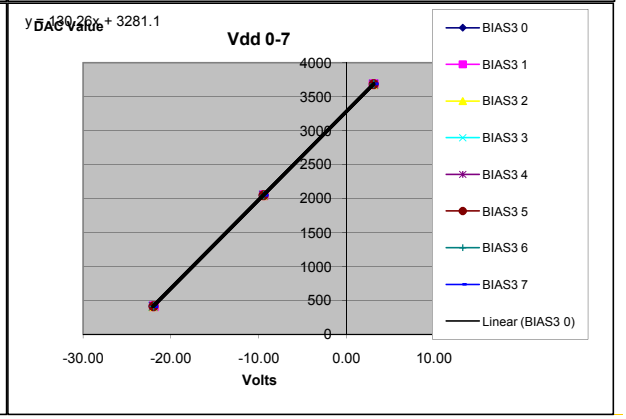
Checked for oscillations using a Agilent Oscilloscpe on AC.**OK**

average min & max voltages
(dac# -offset)/slope=voltage









Stage 8B. Telemetry System Tests - Table 7 (Bias Telemetry Tests)

DAC Value: 410 / 3686

Signal	Telemetry Return Values 10%	90%	Bias Signals Set Volts 10%	90%	Resolved Values for Telemetry Channel Slope	Offset
Vru 0	-1736	424	-13.10	1.88	144.1923	152.92
Vru 1	-1736	424	-13.10	1.88	144.1923	152.92
Vru 2	-1738	425	-13.10	1.88	144.3925	153.54
Vru 3	-1739	425	-13.12	1.88	144.2667	153.78
Vru 4	-1737	424	-13.10	1.88	144.2590	152.79
Vru 5	-1736	424	-13.12	1.88	144.0000	153.28
Vru 6	-1740	424	-13.09	1.88	144.5558	152.24
Vru 7	-1740	424	-13.10	1.88	144.4593	152.42
Vrl 0	-1738	424	-13.11	1.87	144.3258	154.11
Vrl 1	-1735	424	-13.09	1.87	144.3182	154.13
Vrl 2	-1737	424	-13.09	1.87	144.4519	153.88
Vrl 3	-1737	424	-13.10	1.87	144.3554	154.06
Vrl 4	-1738	424	-13.09	1.87	144.5187	153.75
Vrl 5	-1741	424	-13.10	1.87	144.6226	153.56
Vrl 6	-1743	424	-13.12	1.87	144.5630	153.67
Vrl 7	-1740	424	-13.12	1.87	144.3629	154.04
Vog 0	-362	869	-1.75	4.25	205.1667	-2.96
Vog 1	-362	870	-1.75	4.25	205.3333	-2.67
Vog 2	-362	869	-1.75	4.25	205.1667	-2.96
Vog 3	-362	869	-1.75	4.25	205.1667	-2.96
Vog 4	-362	869	-1.75	4.25	205.1667	-2.96
Vog 5	-362	869	-1.75	4.25	205.1667	-2.96
Vog 6	-362	869	-1.75	4.25	205.1667	-2.96
Vog 7	-362	869	-1.75	4.25	205.1667	-2.96
Vdd 0	-1741	574	-22.04	3.11	92.0477	287.73
Vdd 1	-1734	573	-21.96	3.10	92.0591	287.62
Vdd 2	-1743	574	-22.04	3.11	92.1272	287.48
Vdd 3	-1738	574	-22.06	3.11	91.8554	288.33
Vdd 4	-1741	574	-22.04	3.11	92.0477	287.73
Vdd 5	-1739	574	-22.01	3.10	92.1147	288.44
Vdd 6	-1736	573	-21.98	3.10	92.0654	287.60
Vdd 7	-1739	574	-22.01	3.11	92.0780	287.64

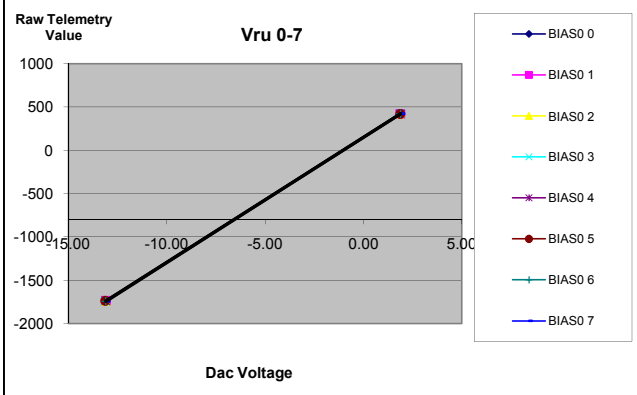
AVERAGE

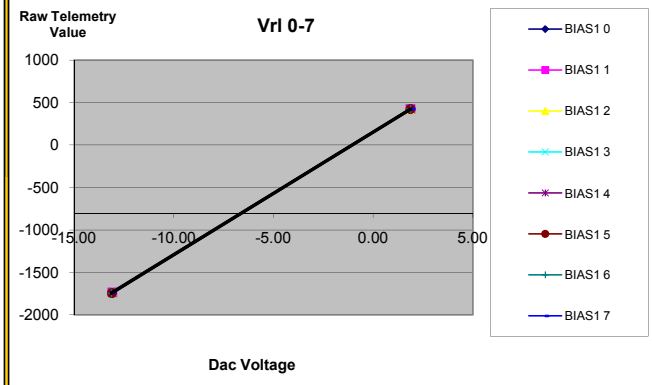
Vru	Slope		Offset
Mean	144.29	Mean	152.99
Stdev	0.1637514	Stdev	0.4947648

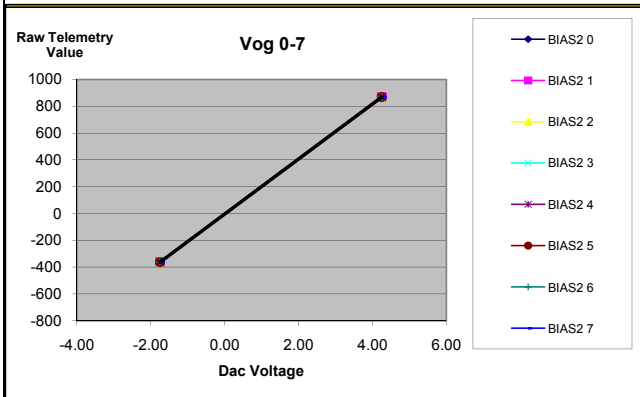
Vrl	Slope		Offset
Mean	144.44	Mean	153.90
Stdev	0.1094326	Stdev	0.2046389

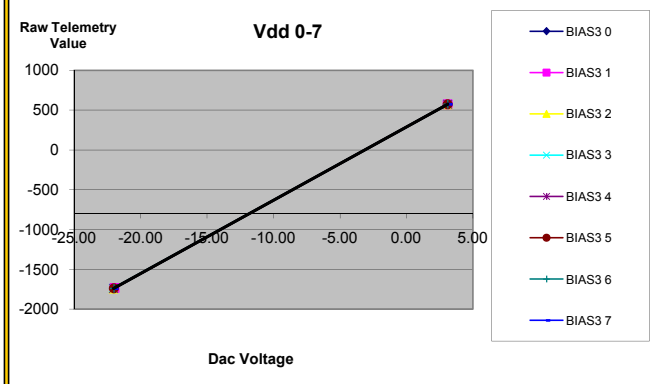
Vog	Slope		Offset
Mean	205.19	Mean	-2.92
Stdev	0.0551198	Stdev	0.0964597

Vdd	Slope		Offset
Mean	92.05	Mean	287.82
Stdev	0.0783729	Stdev	0.335837









Stage 8C. Bias Voltage output enables testing - Table 8

Place a line through Bias Voltage name if enable/disable switch works

Vru 0	Vru 1	Vru 2	Vru 3	Vru 4	Vru 5
Vrl 0	Vrl 1	Vrl 2	Vrl 3	Vrl 4	Vrl 5
Vog 0	Vog 1	Vog 2	Vog 3	Vog 4	Vog 5
Vdd 0	Vdd 1	Vdd 2	Vdd 3	Vdd 4	Vdd 5

Stage 9. Vsub and Heater Control testing - Table 9

DAC Value	Vsub Measured Voltage Test Data 10%	50%	90%
Signal	volts	volts	volts
Vsub - rate	-1.24	3.75	8.76
Vsub - Limit	-1.24	3.75	8.76
Vsub0	0.00	0.00	0.00
	Vsub Enable Bit - pass		

DAC Value	Telemetery Readback Test Data 10%	50%	90%
Signal	dec	dec	dec
Vbias 0	156	270	452
Vbias 1	-26	695	1415
RTD1	218	NA	NA
RTD2	250	NA	NA
RTD3	274	NA	NA
RTD4	301	NA	NA
RTD5	324	NA	NA
RTD6	350	NA	NA
Reference 4096	836	NA	NA
eference buffere	836	NA	NA

Stage 10. Video Offset DAC Tests - Table 10.

	DAC Value 410				DAC Value 2048				DAC Value 3686			
ADC	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU
0	0.250	NA	NA	17093	1.250		NA	81115	2.250	NA	500ms	145124
1	0.250	NA	NA	16934	1.250		NA	81060	2.250	NA	500ms	145185
2	0.250	NA	NA	17194	1.250		NA	81140	2.250	NA	500ms	145092
3	0.250	NA	NA	17102	1.250		NA	81132	2.250	NA	500ms	145166
4	0.250	NA	NA	17166	1.250		NA	81158	2.250	NA	500ms	145147
5	0.250	NA	NA	17018	1.250		NA	81112	2.250	NA	500ms	145217
6	0.250	NA	NA	17015	1.250		NA	81045	2.250	NA	500ms	145077
7	0.250	NA	NA	17021	1.250		NA	81096	2.250	NA	500ms	145171
8	0.250	NA	NA	16837	1.250		NA	80938	2.250	NA	500ms	145044
9	0.250	NA	NA	16974	1.250		NA	81053	2.250	NA	500ms	145132
10	0.250	NA	NA	17049	1.250		NA	81110	2.250	NA	500ms	145174
11	0.250	NA	NA	17019	1.250		NA	81086	2.250	NA	500ms	145143

ADC	DC Volts		Data Set		
Channel	Slope	Offset	410	2048	3686
0	1638.000	0.500	0.250	1.250	2.250
1	1638.000	0.500	0.250	1.250	2.250
2	1638.000	0.500	0.250	1.250	2.250
3	1638.000	0.500	0.250	1.250	2.250
4	1638.000	0.500	0.250	1.250	2.250
5	1638.000	0.500	0.250	1.250	2.250
6	1638.000	0.500	0.250	1.250	2.250
7	1638.000	0.500	0.250	1.250	2.250
8	1638.000	0.500	0.250	1.250	2.250
9	1638.000	0.500	0.250	1.250	2.250
10	1638.000	0.500	0.250	1.250	2.250
11	1638.000	0.500	0.250	1.250	2.250

(dac# -offset)/slope=Voltage

ADC	ADU's		Data Set		
Channel	Slope	Offset	410	2048	3686
0	0.026	-27.42	17093	81115	145124
1	0.026	-22.56	16934	81060	145185
2	0.026	-30.38	17194	81140	145092
3	0.026	-27.47	17102	81132	145166
4	0.026	-29.42	17166	81158	145147
5	0.026	-24.83	17018	81112	145217
6	0.026	-25.26	17015	81045	145077
7	0.026	-25.12	17021	81096	145171
8	0.026	-20.20	16837	80938	145044
9	0.026	-23.89	16974	81053	145132
10	0.026	-25.91	17049	81110	145174
11	0.026	-25.20	17019	81086	145143

(dac# -offset)/slope=ADU

Notes and Observations

Checked for oscillations using a Agilent Oscilloscope on AC. OK

Stage 11. CDS Control Functions and Video Channel Performanc

TEST #1: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit is held static. The purpose of this test is to verify the correct operation of the ADC devices and measure the noise of the Offset voltage generators, ADC buffer amplifiers and ADC devices

Noise Test 1

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	81102	81117	81109.9	2.26672
CH 1	81055	81073	81062.5	2.31938
CH 2	81134	81151	81142.1	2.24696
CH 3	81128	81145	81136.6	2.33005
CH 4	81149	81164	81156.8	2.21019
CH 5	81108	81124	81115.8	2.33803
CH 6	81034	81053	81045	2.30972
CH 7	81088	81104	81096.4	2.45444
CH 8	80934	80950	80942.6	2.26197
CH 9	81044	81061	81051.5	2.31416
CH 10	81102	81119	81110.5	2.18762
CH 11	81075	81091	81083.4	2.37042

TEST #2: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the invert/non-invert and the DC Restore switches are held static.

Noise Test 2

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76359	76381	76369.4	2.72394
CH 1	76573	76592	76581.9	2.73021
CH 2	76569	76588	76578.5	2.62697
CH 3	76695	76715	76705.3	2.88918
CH 4	76486	76506	76496.8	2.75973
CH 5	76841	76861	76849.8	2.71667
CH 6	76858	76879	76867.8	2.63047
CH 7	76861	76882	76871.7	2.89072
CH 8	76415	76436	76425.2	2.74312
CH 9	76921	76942	76931.1	2.7373
CH 10	76448	76468	76456.5	2.81105
CH 11	76965	76988	76975	2.84173

TEST #3: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the DC Restore switch is held static.

Noise Test 3

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76349	76370	76358.4	2.90229
CH 1	76559	76583	76571.5	3.14406
CH 2	76570	76590	76579.5	2.84402
CH 3	76698	76718	76708	3.24236
CH 4	76480	76500	76489.8	2.96207
CH 5	76834	76855	76843.6	3.0991
CH 6	76854	76874	76864.1	2.94387
CH 7	76870	76891	76880.6	3.09027
CH 8	76414	76433	76423.5	2.94491
CH 9	76929	76951	76938.8	3.11006
CH 10	76444	76466	76455.3	3.00816
CH 11	76972	76993	76982.8	3.0635

TEST #4: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition.

Noise Test 4

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76337	76360	76348.7	3.14875
CH 1	76563	76586	76574.4	3.12892
CH 2	76571	76595	76582.1	3.02442
CH 3	76696	76720	76708.7	3.27949
CH 4	76518	76539	76528.1	2.99637
CH 5	76820	76841	76830.6	3.08976
CH 6	76860	76883	76870.7	3.05278
CH 7	76836	76858	76847.8	3.16626
CH 8	76458	76480	76468.9	3.21961
CH 9	76840	76861	76850.4	3.13774
CH 10	76460	76484	76473.1	3.15864
CH 11	76929	76950	76939.4	3.26009

TEST #5: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the circuitry set to high GAIN.

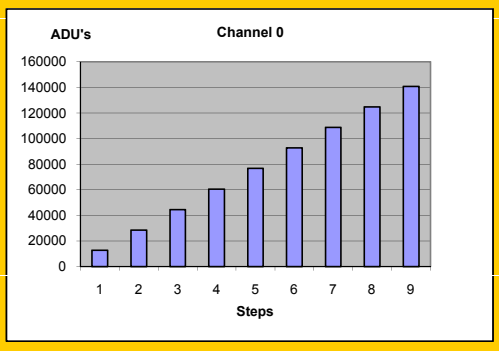
Noise Test 5

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76341	76367	76354.3	3.55388
CH 1	76575	76601	76587	3.73688
CH 2	76582	76610	76595.6	3.70694
CH 3	76700	76726	76714.5	3.71234
CH 4	76518	76544	76531.6	3.55023
CH 5	76816	76844	76829.5	3.62445
CH 6	76860	76884	76871.5	3.56489
CH 7	76835	76862	76849.5	3.70725
CH 8	76509	76534	76522.7	3.6351
CH 9	76836	76863	76849.8	3.7333
CH 10	76525	76553	76539.3	3.63819
CH 11	76926	76953	76939.1	3.71777

TEST #6A: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

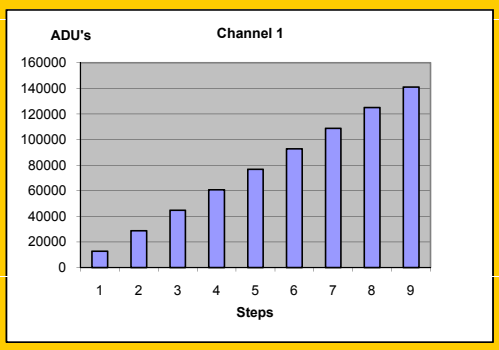
BrdTst6_006 / Channel 0					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12632	12656	12643.6	3.00932	10%
0x333	28618	28640	28628.9	3.07692	20%
0x4cc	44598	44622	44610.1	3.09289	30%
0x666	60625	60646	60634.5	3.15643	40%
0x800	76646	76667	76655.9	3.11204	50%
0x999	92630	92651	92640.5	3.18044	60%
0xb33	108654	108676	108666	3.14832	70%
0xccc	124638	124660	124649	3.14996	80%
0xe66	140661	140688	140675	3.00251	90%



TEST #6B: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

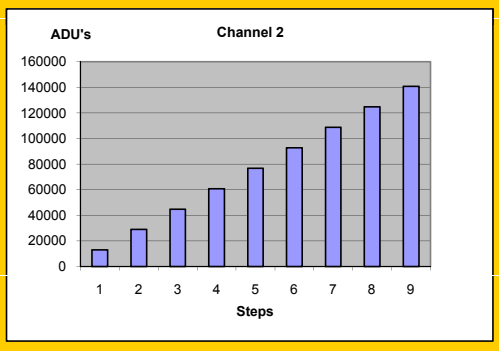
BrdTst6_006 / Channel 1					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12688	12714	12702.9	3.15263	10%
0x333	28702	28723	28713	3.21052	20%
0x4cc	44712	44738	44723.2	3.02894	30%
0x666	60762	60784	60773.3	3.21374	40%
0x800	76809	76831	76820.8	2.99912	50%
0x999	92824	92846	92834.5	3.10993	60%
0xb33	108871	108895	108884	3.15839	70%
0xccc	124885	124907	124897	3.03148	80%
0xe66	140937	140960	140948	3.18214	90%



TEST #6C: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

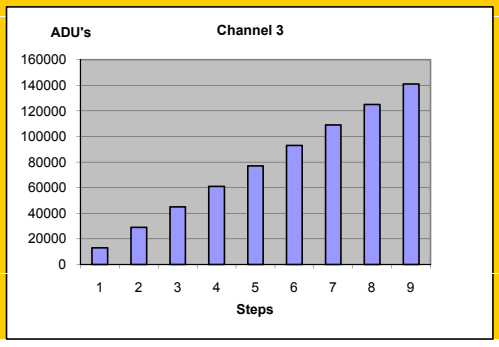
BrdTst6_006 / Channel 2					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12928	12950	12940.6	3.13996	10%
0x333	28897	28919	28908.6	3.125	20%
0x4cc	44864	44886	44874.6	3.15817	30%
0x666	60870	60893	60881.9	3.18135	40%
0x800	76874	76899	76886.2	3.21017	50%
0x999	92845	92868	92855.5	3.15505	60%
0xb33	108851	108873	108863	3.06669	70%
0xccc	124819	124842	124831	3.19518	80%
0xe66	140826	140853	140839	3.1229	90%



TEST #6D: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

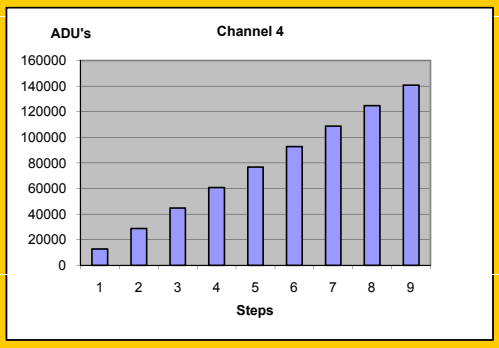
BrdTst6_006 / Channel 3					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12914	12938	12925	3.25433	10%
0x333	28902	28928	28914	3.22742	20%
0x4cc	44886	44908	44897.4	3.21208	30%
0x666	60915	60936	60925.9	3.19754	40%
0x800	76939	76961	76949.9	3.08841	50%
0x999	92929	92950	92939	3.19699	60%
0xb33	108955	108979	108967	3.1796	70%
0xccc	124941	124965	124953	3.23487	80%
0xe66	140969	140991	140981	3.07133	90%



TEST #6E: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

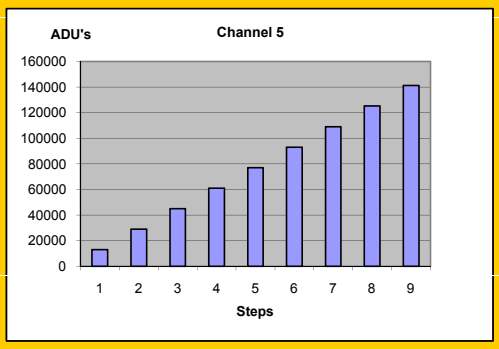
BrdTst6_006 / Channel 4					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12831	12856	12842	3.07627	10%
0x333	28806	28833	28819.1	3.03351	20%
0x4cc	44785	44808	44796.4	3.11201	30%
0x666	60801	60824	60812.4	3.11189	40%
0x800	76813	76837	76825.7	3.11431	50%
0x999	92790	92814	92802	3.27678	60%
0xb33	108806	108829	108818	3.14718	70%
0xccc	124786	124809	124797	3.13886	80%
0xe66	140804	140825	140815	3.09437	90%



TEST #6F: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

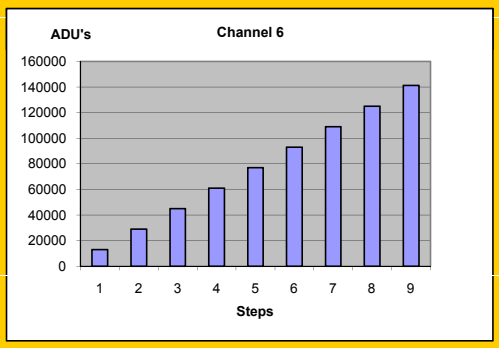
BrdTst6_006 / Channel 5					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12989	13011	12999.2	3.2074	10%
0x333	28991	29012	29001.6	3.13573	20%
0x4cc	44995	45015	45005.8	3.09999	30%
0x666	61036	61059	61046.5	3.18788	40%
0x800	77077	77100	77089.7	3.03438	50%
0x999	93083	93106	93094.2	3.1548	60%
0xb33	109124	109152	109136	3.20724	70%
0xccc	125132	125154	125142	3.15025	80%
0xe66	141174	141196	141185	3.1277	90%



TEST #6G: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

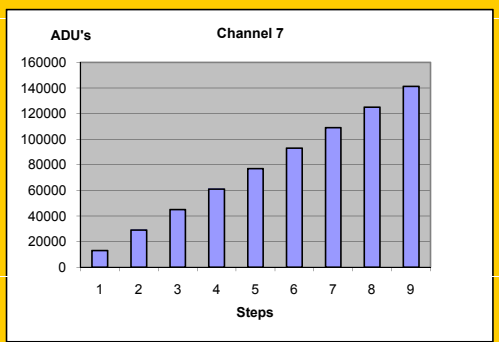
BrdTst6_006 / Channel 6					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13070	13093	13083.1	3.11363	10%
0x333	29062	29084	29071.9	3.14625	20%
0x4cc	45050	45070	45060.2	3.1858	30%
0x666	61076	61098	61086.9	3.11829	40%
0x800	77100	77124	77111.3	3.19269	50%
0x999	93089	93110	93100.1	3.17314	60%
0xb33	109114	109138	109126	3.15289	70%
0xccc	125106	125130	125118	3.14354	80%
0xe66	141132	141158	141145	3.20197	90%



TEST #6H: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

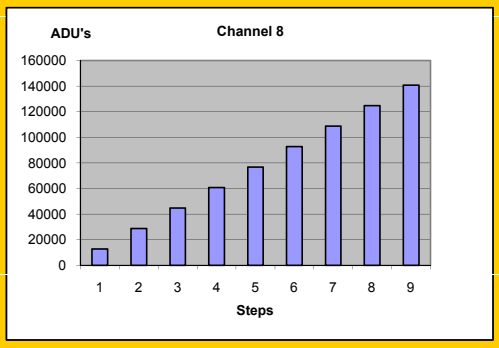
BrdTst6_006 / Channel 7					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12997	13018	13008.1	3.07607	10%
0x333	28994	29017	29005.9	3.19822	20%
0x4cc	44994	45017	45005.6	3.21612	30%
0x666	61031	61054	61042.3	3.1924	40%
0x800	77068	77092	77080.4	3.198	50%
0x999	93068	93092	93079.4	3.21777	60%
0xb33	109104	109128	109117	3.20518	70%
0xccc	125107	125130	125118	3.23784	80%
0xe66	141144	141168	141157	3.28869	90%



TEST #6I: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

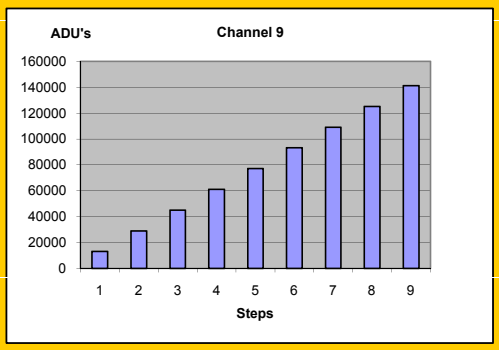
BrdTst6_006 / Channel 8					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12630	12651	12641	3.01248	10%
0x333	28636	28657	28646	3.08319	20%
0x4cc	44640	44662	44650.1	3.10981	30%
0x666	60683	60706	60694.6	2.97872	40%
0x800	76728	76748	76738.7	2.97407	50%
0x999	92736	92757	92745.9	3.10178	60%
0xb33	108779	108802	108791	3.06109	70%
0xccc	124788	124808	124798	3.10104	80%
0xe66	140830	140854	140843	3.12822	90%



TEST #6J: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

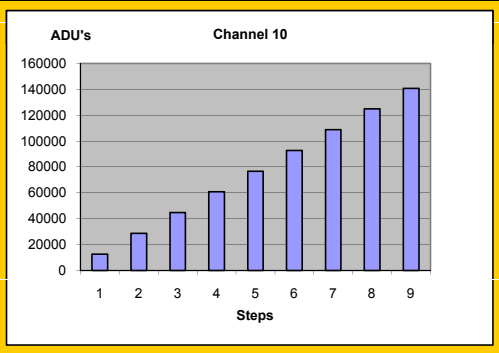
BrdTst6_006 / Channel 9					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13034	13057	13046.3	3.30297	10%
0x333	29031	29054	29043.8	3.24993	20%
0x4cc	45033	45057	45046.2	3.06983	30%
0x666	61072	61096	61083.2	3.21367	40%
0x800	77108	77131	77119.2	3.2673	50%
0x999	93110	93135	93121.6	3.1864	60%
0xb33	109148	109172	109159	3.20372	70%
0xccc	125150	125175	125163	3.22168	80%
0xe66	141188	141212	141201	3.10857	90%



TEST #6K: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

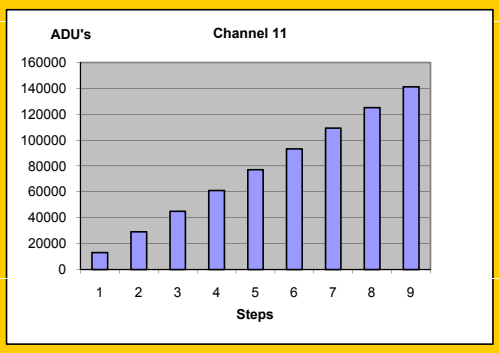
BrdTst6_006 / Channel 10					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12691	12712	12700.7	3.19835	10%
0x333	28685	28709	28697.4	3.15944	20%
0x4cc	44679	44705	44691.5	3.20787	30%
0x666	60716	60738	60726.2	3.10817	40%
0x800	76750	76774	76761.8	3.11666	50%
0x999	92750	92772	92760.6	3.15704	60%
0xb33	108785	108808	108796	3.18443	70%
0xccc	124782	124805	124792	3.13913	80%
0xe66	140817	140839	140829	3.21088	90%



TEST #6L: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

BrdTst6_006 / Channel 11					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13131	13154	13142	3.30409	10%
0x333	29125	29149	29138.3	3.00275	20%
0x4cc	45122	45146	45134.5	3.24903	30%
0x666	61157	61180	61169.4	3.15823	40%
0x800	77190	77212	77201	3.13069	50%
0x999	93187	93212	93198.4	3.22618	60%
0xb33	109221	109244	109233	3.27134	70%
0xccc	125221	125244	125232	3.24735	80%
0xe66	141256	141282	141267	3.28128	90%



Stage 13. Other Bit Tests. Table 11

Electronic Serial Number	0xDB6F9F		Board Serial Number	12
Firmware Version	0x193		Name Of Person Testing	S. Holm
Ident Register	0x502		Board passed Functional Tests	YES