DES 12 Channel Board - Functional Tests: CCD Acquisition Board Revision 1.0

Stage 1. Preparation of documentation and configuration settings - Table 1.

Board Part Number	25		Board Serial Number	0xDB8EC5
Date Of Tests	May 2010		Name Of Person Testing	S. Holm
Suggested Filename To Save	CCDACQ_12Ch_REPORT_BOARD25.xl		Sequence number: Test	

Stage 3. Power plane short test - Table 2.

Supply Name	Short test to ground: Impedance to ground	Test Point	
+1.2VD	45.30	TP43	~50 ohms
+1.8VD	2M	TPB12	> 1K ohm
+2.5VD	17k	TPB11	> 1K ohm
+3.3VD	5k	D13	> 1K ohm
+5VD	18k	D14	> 1K ohm
+5VA	4M	C267	> 1K ohm
-5VA	2M	C270	> 1K ohm
+15VA	100k	C288	> 1K ohm
-15VA	1.1M	C282	> 1K ohm
-28VA	2.6M	C307	> 1K ohm

Stage 4. Firmware programming tests - Table 3.

JTAG Order	Designator	Device	Load File	Check Sum or User Code
1	U122	XCF08PFS48C PROM	CcdAcqFpgaV41.mcs	0014ef670
2	U114	Spartan3 XC3S2000 FPGA	ccdacqfpgav41.bit	5102801

Stage 5. Power Consumption - Table 4.

Supply Name	Power Supply Consumption: Measured Voltage at test point	Measured Current on power supply	Test Point	
+1.2VD	1.21	N/A	TP43	
+1.8VD	1.80	N/A	TPB12	
+2.5VD	2.51	N/A	TPB11	
+3.3VD	3.29	0.112	D13	
+5VD	5.20	0.155	D14	
+5VA	4.99	0.667	C267	
-5VA	-4.85	0.433	C270	
+15VA	15.12	0.556	C288	
-15VA	-15.08	0.408	C282	
-28VA	-27.88	0.219	C307	
Vref 0+	10.03	N/A	R534	Vsub+ Reference(+10v)
Vref 0-	-2.50	N/A	R525	Vsub - Reference(-2.5v)
Vref Offset	2.50	N/A	R573	ADC Offset Reference(+2.5v)
Vclamp	1.87	N/A	VIA	ADC Clamp Voltage(+1.8v)
ADC Ref.	2.50	N/A	VIA	ADC Reference Voltage(+2.5v)
Vref 1+	2.50	N/A	R537	Vru and Vrl + Reference(+2.5v)
Vref 1-	-10.08	N/A	R535	Vru and Vrl - Reference(-10v)
Vref 2+	5.01	N/A	R563	Vog + Reference(+5v)
Vref 2-	-2.50	N/A	R555	Vog - Reference(-2.5v)
Vref 3+	2.50	N/A	R543	Vdd + Reference(+2.5v)
Vref 3-	-9.96	N/A	R571	Vdd - Reference(-10v)

Power Dissipation:
27.3 Watts

~27 watts +/- 5%

Stage 7. Basic Bus Transactions - **D**igital **Register** Tests - Table 5.

Register name	Put an X on any bit that has an error: 31-24 23-16 15-08 07-00	Function	Test name: Pattern	Walking 0's	Walking 1's
CDS Control	00000000 00000000	16 bit R/W			
Digital Output	00000000 00000000 00000000 00000000	32 bit R/W			
ADC Config.	0000 00000000	12 bit R/W			
Offset DAC	0000 00000000	12 bit R/W			
Bias DAC	0000 00000000	12 bit R/W			
Telemetry Config.	0000	4 bit R/W			
Auxilary Config.	00 00000000	10 bit R/W			
Redirect	0000	4 bit R/W			
Pixel Transfer	00000000	8 bit R/W			
Micro SEQ	00000000 00000000	16 bit R/W			
RAM Buffer	00000000 00000000	16 bit R/W			
LED Control	0000	4 bit R/W			
Control	00000000 00000000	16 bit R/W			
All Register Test	00000000 00000000 00000000 00000000	16 bit R/W	**Passed**	**Passed**	**Passed**

Stage 8. Bias Voltage settings and output enables testing - Table 8

DAC Value	Bias Voltage Test Data 410	2048	3686	50% rms Noise	10-90% Rise Time			
Signal	volts	volts	volts	uV	millisec.	Fanout Brd	Slope	Offset
Vru 0	-13.23	-5.68	1.86	<10	2	BIAS 3	217.10	3281.84
Vru 1	-13.23	-5.68	1.86	<10	2	BIAS 4	217.10	3281.84
Vru 2	-13.23	-5.68	1.86	<10	2	BIAS 5	217.10	3281.84
Vru 3	-13.23	-5.68	1.86	<10	2	BIAS 6	217.10	3281.84
Vru 4	-13.23	-5.68	1.86	<10	2	BIAS 7	217.10	3281.84
Vru 5	-13.23	-5.68	1.86	<10	2	BIAS 8	217.10	3281.84
Vru 6	-13.23	-5.68	1.86	NA	NA	BIAS 9	217.10	3281.84
Vru 7	-13.23	-5.68	1.86	NA	NA	BIAS 10	217.10	3281.84
Vrl 0	-13.23	-5.68	1.86	<10	2	BIAS 11	217.10	3281.84
Vrl 1	-13.23	-5.68	1.86	<10	2	BIAS 12	217.10	3281.84
Vrl 2	-13.23	-5.68	1.86	<10	2	BIAS 13	217.10	3281.84
Vrl 3	-13.23	-5.68	1.86	<10	2	BIAS 14	217.10	3281.84
Vrl 4	-13.23	-5.68	1.86	<10	2	BIAS 15	217.10	3281.84
Vrl 5	-13.23	-5.68	1.86	<10	2	BIAS 16	217.10	3281.84
Vrl 6	-13.23	-5.68	1.86	NA	NA	BIAS 17	217.10	3281.84
Vrl 7	-13.23	-5.68	1.86	NA	NA	BIAS 18	217.10	3281.84
Vog 0	-1.75	1.25	4.26	<10	2	BIAS 19	545.09	1364.82
Vog 1	-1.75	1.25	4.26	<10	2	BIAS 20	545.09	1364.82
Vog 2	-1.75	1.25	4.26	<10	2	BIAS 21	545.09	1364.82
Vog 3	-1.75	1.25	4.26	<10	2	BIAS 22	545.09	1364.82
Vog 4	-1.75	1.25	4.26	<10	2	BIAS 23	545.09	1364.82
Vog 5	-1.75	1.25	4.26	<10	2	BIAS 24	545.09	1364.82
Vog 6	-1.75	1.25	4.26	NA	NA	BIAS 25	545.09	1364.82
Vog 7	-1.75	1.25	4.26	NA	NA	BIAS 26	545.09	1364.82
Vdd 0	-21.84	-9.36	3.13	<10	20	BIAS 27	131.20	3275.57
Vdd 1	-21.79	-9.34	3.13	<10	20	BIAS 28	131.46	3274.97
Vdd 2	-21.80	-9.34	3.13	<10	20	BIAS 29	131.41	3274.91
Vdd 3	-21.77	-9.32	3.13	<10	20	BIAS 30	131.57	3274.20
Vdd 4	-21.92	-9.39	3.13	<10	20	BIAS 21	130.78	3276.45
Vdd 5	-21.93	-9.39	3.13	<10	20	BIAS 32	130.73	3276.39
Vdd 6	-21.78	-9.33	3.13	NA	NA	BIAS 33	131.51	3274.58
Vdd 7	-21.73	-9.31	3.13	NA	NA	BIAS 34	131.78	3273.97

Vru	Slope		Offset
Mean	217.10	Mean	3281.84
Stdev	2.842E-14	Stdev	0
Average	217.09738	Average	3281.836798
	Dac #	Average voltage	
	0	-15.0	
	4095	3.8	

Vrl	Slope		Offset
Mean	217.10	Mean	3281.84
Stdev	2.842E-14	Stdev	0
Average	217.09738	Average	3281.836798
	Dac #	Average voltage	
	0	-15.1	
	4095	3.8	

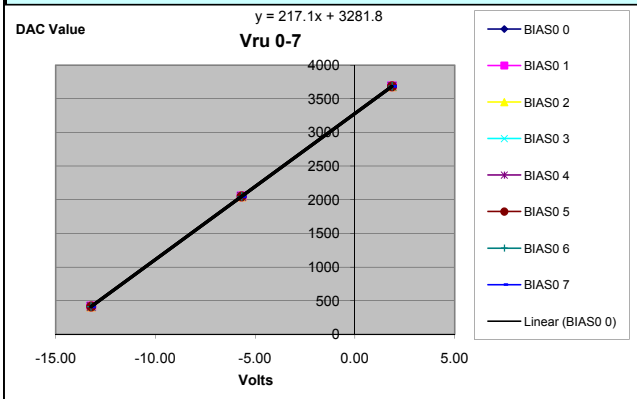
Vog	Slope		Offset
Mean	545.09	Mean	1364.82
Stdev	1.137E-13	Stdev	0
Average	545.09101	Average	1364.819266
	Dac #	Average voltage	
	0	-2.5	
	4095	5.0	

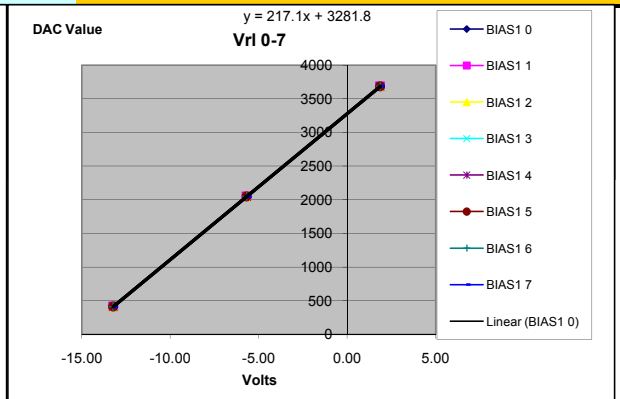
Vdd	Slope		Offset
Mean	131.30	Mean	3275.13
Stdev	0.3524892	Stdev	0.872821781
Average	131.30354	Average	3275.129824
	Dac #	Average voltage	
	0	-24.9	
	4095	6.3	

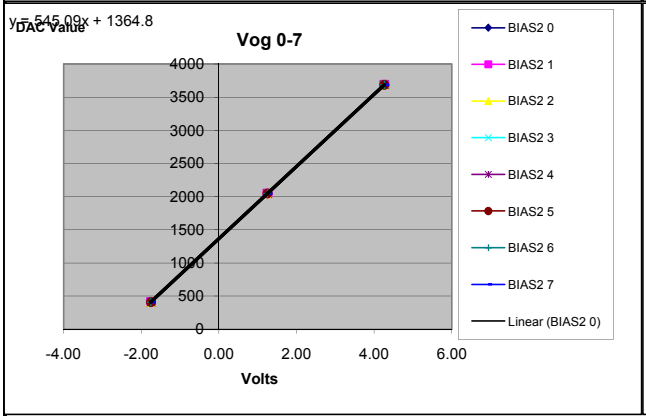
Notes and Observations

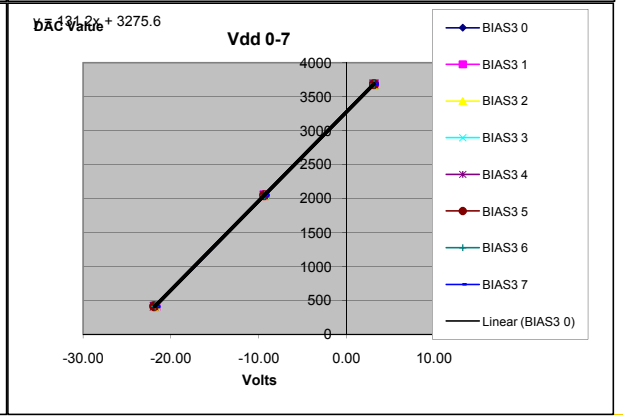
Checked for oscillations using a Agilent Oscilloscpe on AC.**OK**

average min & max voltages
(dac# -offset)/slope=voltage









Stage 8B. Telemetry System Tests - Table 7 (Bias Telemetry Tests)

DAC Value	410	3686	Bias Signals Set Volts		Resolved Values for Telemetry Channel	
	Telemetry Return Values					
Signal	10%	90%	10%	90%	Slope	Offset
Vru 0	-1748	422	-13.23	1.86	143.8038	154.52
Vru 1	-1749	422	-13.23	1.86	143.8701	154.40
Vru 2	-1752	422	-13.23	1.86	144.0689	154.03
Vru 3	-1747	422	-13.23	1.86	143.7376	154.65
Vru 4	-1753	422	-13.23	1.86	144.1352	153.91
Vru 5	-1748	422	-13.23	1.86	143.8038	154.52
Vru 6	-1750	422	-13.23	1.86	143.9364	154.28
Vru 7	-1750	422	-13.23	1.86	143.9364	154.28
Vrl 0	-1755	422	-13.23	1.86	144.2677	153.66
Vrl 1	-1755	422	-13.23	1.86	144.2677	153.66
Vrl 2	-1762	422	-13.23	1.86	144.7316	152.80
Vrl 3	-1762	422	-13.23	1.86	144.7316	152.80
Vrl 4	-1758	422	-13.23	1.86	144.4665	153.29
Vrl 5	-1759	422	-13.23	1.86	144.5328	153.17
Vrl 6	-1757	421	-13.23	1.86	144.3340	152.54
Vrl 7	-1757	421	-13.23	1.86	144.3340	152.54
Vog 0	-361	868	-1.75	4.26	204.4925	-3.14
Vog 1	-362	868	-1.75	4.26	204.6589	-3.85
Vog 2	-362	868	-1.75	4.26	204.6589	-3.85
Vog 3	-361	868	-1.75	4.26	204.4925	-3.14
Vog 4	-362	868	-1.75	4.26	204.6589	-3.85
Vog 5	-361	869	-1.75	4.26	204.6589	-2.85
Vog 6	-362	868	-1.75	4.26	204.6589	-3.85
Vog 7	-361	868	-1.75	4.26	204.4925	-3.14
Vdd 0	-1711	575	-21.84	3.13	91.5499	288.45
Vdd 1	-1706	575	-21.79	3.13	91.5329	288.50
Vdd 2	-1706	574	-21.80	3.13	91.4561	287.74
Vdd 3	-1703	574	-21.77	3.13	91.4458	287.77
Vdd 4	-1720	576	-21.92	3.13	91.6567	289.11
Vdd 5	-1717	576	-21.93	3.13	91.5004	289.60
Vdd 6	-1702	574	-21.78	3.13	91.3689	288.02
Vdd 7	-1701	574	-21.73	3.13	91.5125	287.57

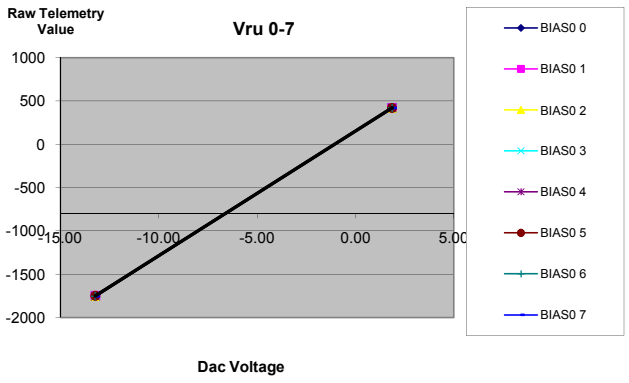
AVERAGE

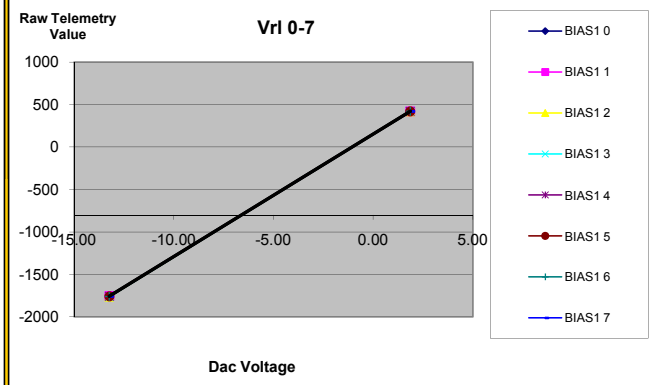
Vru	Slope		Offset
Mean	143.91	Mean	154.32
Stdev	0.1280618	Stdev	0.238195

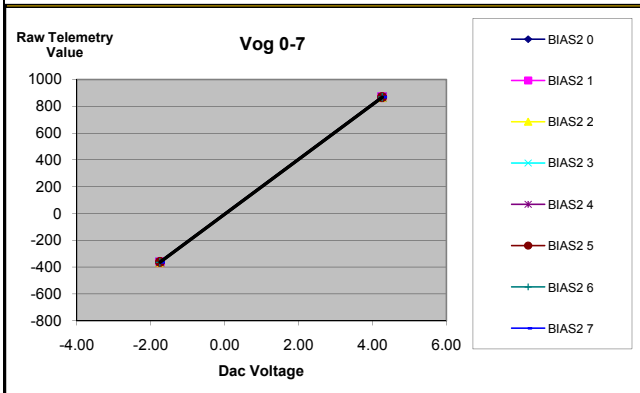
Vrl	Slope		Offset
Mean	144.46	Mean	153.06
Stdev	0.1797758	Stdev	0.4286669

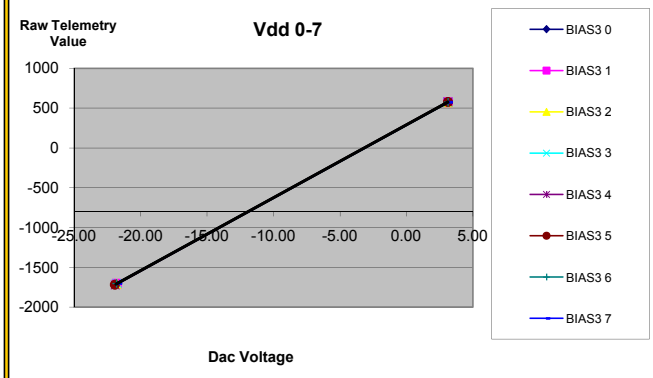
Vog	Slope		Offset
Mean	204.60	Mean	-3.46
Stdev	0.0805529	Stdev	0.4008477

Vdd	Slope		Offset
Mean	91.50	Mean	288.35
Stdev	0.0792598	Stdev	0.6723128









Stage 8C. Bias Voltage output enables testing - Table 8

Place a line through Bias Voltage name if enable/disable switch works

Vru 0	Vru 1	Vru 2	Vru 3	Vru 4	Vru 5
Vrl 0	Vrl 1	Vrl 2	Vrl 3	Vrl 4	Vrl 5
Vog 0	Vog 1	Vog 2	Vog 3	Vog 4	Vog 5
Vdd 0	Vdd 1	Vdd 2	Vdd 3	Vdd 4	Vdd 5

Stage 9. Vsub and Heater Control testing - Table 9

DAC Value	Vsub Measured Voltage Test Data 10%	50%	90%
Signal	volts	volts	volts
Vsub - rate	-1.26	3.76	8.78
Vsub - Limit	-1.27	3.75	8.79
Vsub0	0.00	3.75	8.75
	Vsub Enable Bit - pass		

DAC Value	Telemetery Readback Test Data 10%	50%	90%
Signal	dec	dec	dec
Vbias 0	153	324	455
Vbias 1	-27	695	1416
RTD1	220	NA	NA
RTD2	248	NA	NA
RTD3	275	NA	NA
RTD4	303	NA	NA
RTD5	324	NA	NA
RTD6	351	NA	NA
Reference 4096	836	NA	NA
eference buffere	836	NA	NA

Stage 10. Video Offset DAC Tests - Table 10.

	DAC Value 410				DAC Value 2048				DAC Value 3686			
ADC	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU
0	0.250	NA	NA	17011	1.250		NA	81089	2.250	NA	500ms	145160
1	0.250	NA	NA	17124	1.250		NA	81128	2.250	NA	500ms	145129
2	0.250	NA	NA	17025	1.250		NA	81045	2.250	NA	500ms	145055
3	0.250	NA	NA	16919	1.250		NA	80966	2.250	NA	500ms	145013
4	0.250	NA	NA	16999	1.250		NA	81069	2.250	NA	500ms	145142
5	0.250	NA	NA	16951	1.250		NA	81029	2.250	NA	500ms	145105
6	0.250	NA	NA	17010	1.250		NA	81080	2.250	NA	500ms	145156
7	0.250	NA	NA	17076	1.250		NA	81142	2.250	NA	500ms	145194
8	0.250	NA	NA	17088	1.250		NA	81130	2.250	NA	500ms	145156
9	0.250	NA	NA	17154	1.250		NA	81210	2.250	NA	500ms	145270
10	0.250	NA	NA	17184	1.250		NA	81232	2.250	NA	500ms	145270
11	0.250	NA	NA	17246	1.250		NA	81289	2.250	NA	500ms	145329

ADC	DC Volts		Data Set		
Channel	Slope	Offset	410	2048	3686
0	1638.000	0.500	0.250	1.250	2.250
1	1638.000	0.500	0.250	1.250	2.250
2	1638.000	0.500	0.250	1.250	2.250
3	1638.000	0.500	0.250	1.250	2.250
4	1638.000	0.500	0.250	1.250	2.250
5	1638.000	0.500	0.250	1.250	2.250
6	1638.000	0.500	0.250	1.250	2.250
7	1638.000	0.500	0.250	1.250	2.250
8	1638.000	0.500	0.250	1.250	2.250
9	1638.000	0.500	0.250	1.250	2.250
10	1638.000	0.500	0.250	1.250	2.250
11	1638.000	0.500	0.250	1.250	2.250

(dac# -offset)/slope=Voltage

ADC	ADU's		Data Set		
Channel	Slope	Offset	410	2048	3686
0	0.026	-24.90	17011	81089	145160
1	0.026	-28.26	17124	81128	145129
2	0.026	-25.67	17025	81045	145055
3	0.026	-22.70	16919	80966	145013
4	0.026	-24.57	16999	81069	145142
5	0.026	-23.33	16951	81029	145105
6	0.026	-24.83	17010	81080	145156
7	0.026	-26.70	17076	81142	145194
8	0.026	-27.18	17088	81130	145156
9	0.026	-28.62	17154	81210	145270
10	0.026	-29.55	17184	81232	145270
11	0.026	-31.12	17246	81289	145329

(dac# -offset)/slope=ADU

Notes and Observations

Checked for oscillations using a Agilent Oscilloscope on AC. OK

Stage 11. CDS Control Functions and Video Channel Performanc

TEST #1: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit is held static. The purpose of this test is to verify the correct operation of the ADC devices and measure the noise of the Offset voltage generators, ADC buffer amplifiers and ADC devices

Noise Test 1

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	81079	81094	81086.5	2.2407
CH 1	81116	81133	81124.8	2.36519
CH 2	81034	81051	81042.3	2.31349
CH 3	80957	80976	80966.7	2.3375
CH 4	81063	81080	81072	2.28577
CH 5	81016	81034	81025.6	2.34718
CH 6	81076	81092	81084	2.28321
CH 7	81130	81146	81138.1	2.32056
CH 8	81120	81135	81127	2.20869
CH 9	81204	81220	81212.4	2.31148
CH 10	81217	81233	81224.8	2.31079
CH 11	81280	81297	81288.1	2.40747

TEST #2: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the invert/non-invert and the DC Restore switches are held static.

Noise Test 2

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76466	76484	76474.9	2.7769
CH 1	76772	76796	76783	2.90863
CH 2	76220	76240	76230.3	2.8065
CH 3	76750	76772	76761.7	2.86319
CH 4	76344	76363	76353.3	2.83008
CH 5	76419	76439	76429.6	2.88675
CH 6	76775	76795	76786.2	2.71906
CH 7	76900	76918	76908.8	2.8447
CH 8	76553	76572	76563.3	2.6191
CH 9	77133	77152	77142.3	2.71439
CH 10	76701	76720	76711.1	2.83959
CH 11	76878	76897	76887.6	2.85489

TEST #3: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the DC Restore switch is held static.

Noise Test 3

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76461	76482	76470.6	2.88634
CH 1	76758	76782	76769.9	3.03396
CH 2	76195	76218	76205.8	3.0435
CH 3	76748	76772	76761	3.12363
CH 4	76343	76364	76354.2	3.03787
CH 5	76412	76432	76422	3.08397
CH 6	76771	76792	76782.2	2.9841
CH 7	76897	76920	76909.2	3.04667
CH 8	76558	76580	76568.4	2.99271
CH 9	77138	77161	77148.7	3.08619
CH 10	76695	76718	76705.9	2.90968
CH 11	76869	76892	76880.6	3.10401

TEST #4: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition.

Noise Test 4

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76449	76472	76461.6	3.08954
CH 1	76761	76784	76773.1	3.18591
CH 2	76197	76222	76210.4	3.15649
CH 3	76749	76772	76760.8	3.22479
CH 4	76385	76407	76395.7	3.08279
CH 5	76398	76422	76409.5	3.24466
CH 6	76783	76804	76792.9	3.10922
CH 7	76853	76877	76865.7	3.15185
CH 8	76602	76624	76613	2.93475
CH 9	77050	77073	77061.1	3.16983
CH 10	76712	76736	76724.3	3.02111
CH 11	76828	76850	76838.9	3.14128

TEST #5: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the circuitry set to high GAIN.

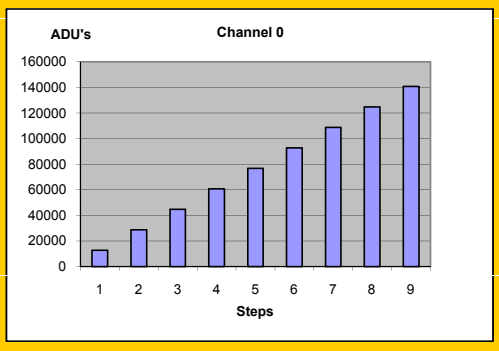
Noise Test 5

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76457	76483	76469.2	3.44432
CH 1	76773	76799	76785	3.71551
CH 2	76215	76237	76225.6	3.58354
CH 3	76754	76781	76766.9	3.67859
CH 4	76386	76410	76399.4	3.61003
CH 5	76394	76422	76408	3.79197
CH 6	76780	76807	76792.4	3.57453
CH 7	76853	76878	76865.7	3.70744
CH 8	76647	76674	76661.3	3.69233
CH 9	77046	77073	77060.6	3.75795
CH 10	76772	76801	76786.6	3.74377
CH 11	76825	76853	76838.1	3.54979

TEST #6A: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

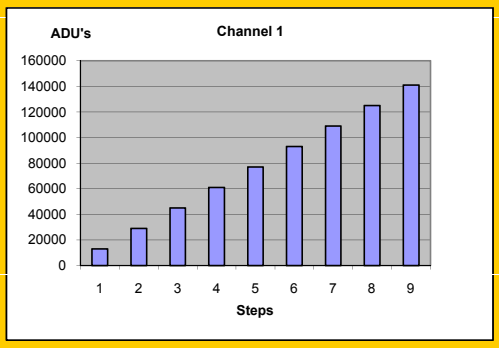
BrdTst6_006 / Channel 0					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12686	12708	12697.4	3.14391	10%
0x333	28687	28708	28697.5	3.14327	20%
0x4cc	44683	44706	44694.3	3.02032	30%
0x666	60722	60746	60733.2	3.12752	40%
0x800	76759	76780	76769.2	3.08194	50%
0x999	92757	92778	92767.5	3.14448	60%
0xb33	108798	108819	108808	3.14059	70%
0xccc	124796	124820	124807	3.07647	80%
0xe66	140835	140858	140847	3.12081	90%



TEST #6B: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

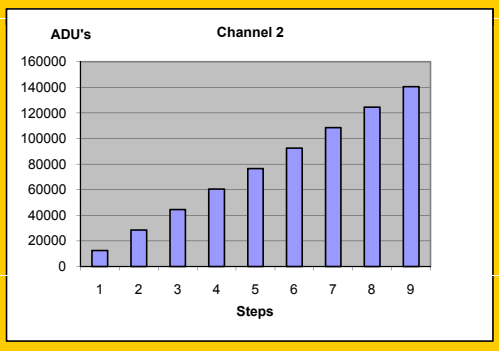
BrdTst6_006 / Channel 1					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13006	13027	13016.3	3.20135	10%
0x333	28986	29011	28998.9	3.22727	20%
0x4cc	44964	44988	44976.6	3.2529	30%
0x666	60987	61010	60997.4	3.09092	40%
0x800	77005	77027	77015.9	3.13785	50%
0x999	92987	93008	92997.1	3.09781	60%
0xb33	109008	109031	109018	3.15564	70%
0xccc	124986	125012	124999	3.18627	80%
0xe66	141009	141030	141020	3.18082	90%



TEST #6C: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

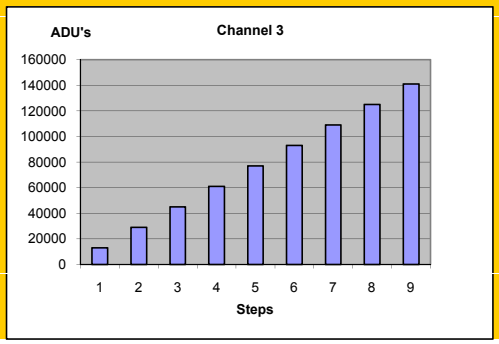
BrdTst6_006 / Channel 2					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12483	12504	12493.4	3.16046	10%
0x333	28466	28488	28477.2	3.14231	20%
0x4cc	44450	44472	44461.3	3.1509	30%
0x666	60472	60495	60484.1	3.21353	40%
0x800	76495	76516	76506	3.1417	50%
0x999	92481	92504	92492.8	3.1397	60%
0xb33	108506	108526	108516	3.16548	70%
0xccc	124494	124516	124504	3.12263	80%
0xe66	140515	140539	140528	3.07128	90%



TEST #6D: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

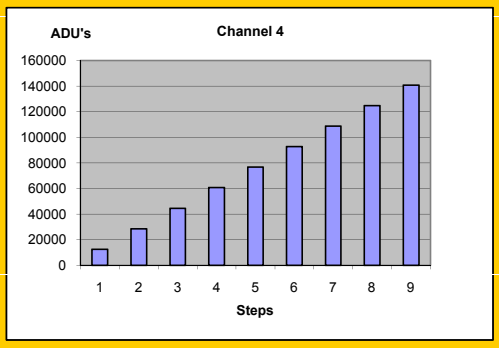
BrdTst6_006 / Channel 3					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12939	12962	12950.3	3.23548	10%
0x333	28931	28954	28942	3.17166	20%
0x4cc	44925	44948	44936.4	3.29397	30%
0x666	60957	60977	60966.6	3.13449	40%
0x800	76982	77005	76993.9	3.15276	50%
0x999	92974	92997	92985.4	3.20581	60%
0xb33	109007	109028	109018	3.12954	70%
0xccc	125000	125024	125012	3.23738	80%
0xe66	141033	141058	141045	3.25818	90%



TEST #6E: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

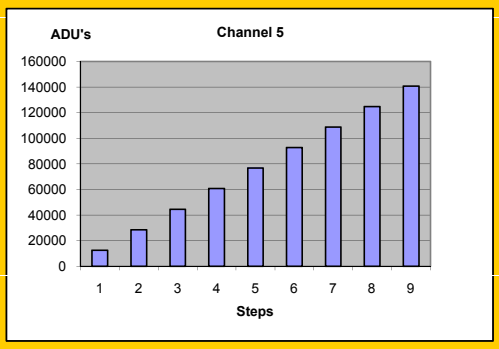
BrdTst6_006 / Channel 4					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12610	12634	12622.8	3.17407	10%
0x333	28613	28635	28623.9	3.19393	20%
0x4cc	44608	44630	44618.9	3.14934	30%
0x666	60647	60670	60658.5	3.02228	40%
0x800	76682	76704	76692.3	3.10494	50%
0x999	92679	92701	92689.8	3.15037	60%
0xb33	108719	108741	108731	3.09374	70%
0xccc	124716	124740	124728	3.22484	80%
0xe66	140755	140782	140769	3.18769	90%



TEST #6F: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

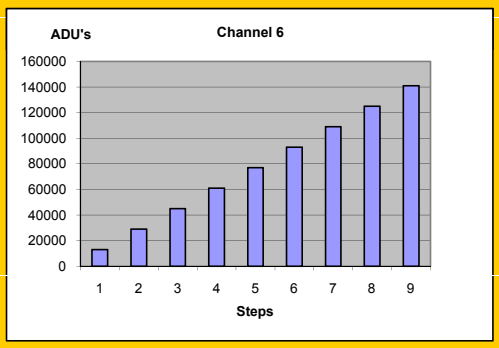
BrdTst6_006 / Channel 5					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12592	12615	12603.6	3.27286	10%
0x333	28592	28616	28602.4	3.17521	20%
0x4cc	44590	44613	44602.3	3.27473	30%
0x666	60626	60651	60638.7	3.20958	40%
0x800	76662	76685	76673.5	3.24164	50%
0x999	92662	92686	92674.5	3.31717	60%
0xb33	108701	108723	108712	3.2069	70%
0xccc	124704	124726	124714	3.21723	80%
0xe66	140742	140765	140753	3.21991	90%



TEST #6G: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

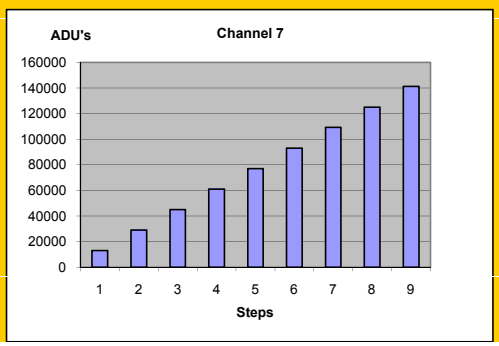
BrdTst6_006 / Channel 6					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12951	12974	12962.6	3.02219	10%
0x333	28947	28969	28958.7	3.09867	20%
0x4cc	44946	44971	44958.3	3.13188	30%
0x666	60983	61007	60993.5	3.06446	40%
0x800	77018	77041	77028.7	3.23321	50%
0x999	93017	93040	93028.2	3.18369	60%
0xb33	109053	109075	109064	3.12769	70%
0xccc	125054	125078	125064	3.11047	80%
0xe66	141089	141111	141100	3.18413	90%



TEST #6H: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

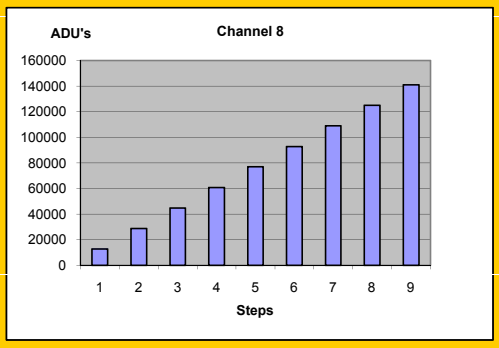
BrdTst6_006 / Channel 7					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13043	13067	13055.1	3.18044	10%
0x333	29035	29058	29047.2	3.11928	20%
0x4cc	44925	45056	45043.3	7.93257	30%
0x666	61067	61091	61078.2	3.19175	40%
0x800	77094	77120	77107.2	2.99086	50%
0x999	93091	93115	93102.2	3.17212	60%
0xb33	109125	109145	109135	3.13847	70%
0xccc	125124	125147	125136	3.15819	80%
0xe66	141158	141178	141168	3.09284	90%



TEST #6I: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

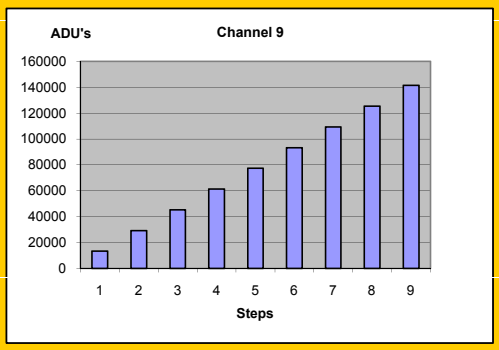
BrdTst6_006 / Channel 8					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12850	12873	12860.7	3.14524	10%
0x333	28839	28861	28849.9	3.12242	20%
0x4cc	44828	44850	44839.6	3.04672	30%
0x666	60857	60878	60867.6	3.1775	40%
0x800	76879	76901	76889.9	3.13211	50%
0x999	92869	92891	92879.5	3.07758	60%
0xb33	108898	108920	108909	3.1571	70%
0xccc	124888	124911	124900	3.0308	80%
0xe66	140918	140940	140930	3.03922	90%



TEST #6J: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

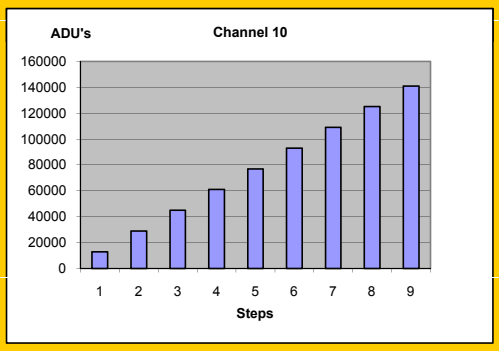
BrdTst6_006 / Channel 9					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13259	13284	13271.3	3.12354	10%
0x333	29254	29277	29266.6	2.98059	20%
0x4cc	45251	45273	45261.6	3.08864	30%
0x666	61284	61309	61295.9	3.10646	40%
0x800	77315	77336	77326	3.13058	50%
0x999	93310	93332	93321.3	3.23267	60%
0xb33	109344	109368	109356	3.16779	70%
0xccc	125341	125365	125353	3.23302	80%
0xe66	141377	141400	141388	3.186	90%



TEST #6K: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

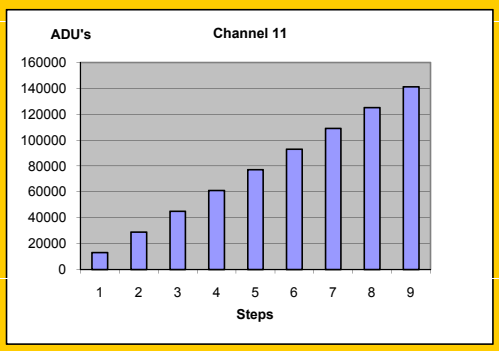
BrdTst6_006 / Channel 10					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12949	12971	12960.3	3.19091	10%
0x333	28937	28960	28948.7	3.25557	20%
0x4cc	44932	44955	44943.7	3.04563	30%
0x666	60962	60985	60971.6	3.10944	40%
0x800	76990	77014	77002.1	3.19331	50%
0x999	92984	93007	92995.4	3.03291	60%
0xb33	109013	109035	109025	3.14877	70%
0xccc	125011	125034	125022	3.20206	80%
0xe66	141038	141060	141050	3.17506	90%



TEST #6L: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

BrdTst6_006 / Channel 11					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13055	13080	13068	3.27412	10%
0x333	29050	29072	29059.9	3.25744	20%
0x4cc	45037	45063	45049.2	3.21466	30%
0x666	61067	61092	61079.7	3.24758	40%
0x800	77094	77118	77106.4	3.33291	50%
0x999	93089	93110	93099.7	3.20858	60%
0xb33	109120	109144	109131	3.26593	70%
0xccc	125111	125134	125122	3.35397	80%
0xe66	141140	141166	141153	3.13648	90%



Stage 13. Other Bit Tests. Table 11

Electronic Serial Number	0xDB8EC5		Board Serial Number	25
Firmware Version	0x193		Name Of Person Testing	S. Holm
Ident Register	0x502		Board passed Functional Tests	YES