DES 12 Channel Board - Functional Tests: CCD Acquisition Board Revision 1.0

Stage 1. Preparation of documentation and configuration settings - Table 1.

Board Part Number	29		Board Serial Number	0xDB8EBD
Date Of Tests	July 2010		Name Of Person Testing	S. Holm
Suggested Filename To Save	CCDACQ_12Ch_REPORT_BOARD6.xls		Sequence number: Test	

Stage 3. Power plane short test - Table 2.

Supply Name	Short test to ground: Impedance to ground	Test Point	
+1.2VD	40.70	TP43	~50 ohms
+1.8VD	2.5M	TPB12	> 1K ohm
+2.5VD	17K	TPB11	> 1K ohm
+3.3VD	5K	D13	> 1K ohm
+5VD	18K	D14	> 1K ohm
+5VA	4M	C267	> 1K ohm
-5VA	300K	C270	> 1K ohm
+15VA	500K	C288	> 1K ohm
-15VA	500K	C282	> 1K ohm
-28VA	2.8M	C307	> 1K ohm

Stage 4. Firmware programming tests - Table 3.

JTAG Order	Designator	Device	Load File	Check Sum or User Code
1	U122	XCF08PFS48C PROM	CcdAcqFpgaV41.mcs	0014ef670
2	U114	Spartan3 XC3S2000 FPGA	ccdacqfpgav41.bit	5102801

Stage 5. Power Consumption - Table 4.

Supply Name	Power Supply Consumption: Measured Voltage at test point	Measured Current on power supply	Test Point	
+1.2VD	1.20	N/A	TP43	
+1.8VD	1.80	N/A	TPB12	
+2.5VD	2.50	N/A	TPB11	
+3.3VD	3.30	0.219	D13	
+5VD	5.20	0.151	D14	
+5VA	5.30	0.591	C267	
-5VA	-4.80	0.437	C270	
+15VA	15.02	0.558	C288	
-15VA	-15.07	0.407	C282	
-28VA	-27.83	0.208	C307	
Vref 0+	10.08	N/A	R534	Vsub+ Reference(+10v)
Vref 0-	-2.50	N/A	R525	Vsub - Reference(-2.5v)
Vref Offset	2.50	N/A	R573	ADC Offset Reference(+2.5v)
Vclamp	1.87	N/A	VIA	ADC Clamp Voltage(+1.8v)
ADC Ref.	2.50	N/A	VIA	ADC Reference Voltage(+2.5v)
Vref 1+	2.50	N/A	R537	Vru and Vrl + Reference(+2.5v)
Vref 1-	-10.04	N/A	R535	Vru and Vrl - Reference(-10v)
Vref 2+	5.00	N/A	R563	Vog + Reference(+5v)
Vref 2-	-2.50	N/A	R555	Vog - Reference(-2.5v)
Vref 3+	2.50	N/A	R543	Vdd + Reference(+2.5v)
Vref 3-	-10.03	N/A	R571	Vdd - Reference(-10v)

Power Dissipation:
27.0 Watts

~27 watts +/- 5%

Stage 7. Basic Bus Transactions - **D**igital **Register** Tests - Table 5.

Register name	Put an X on any bit that has an error: 31-24	23-16	15-08	07-00	Function	Test name: Pattern	Walking 0's	Walking 1's
CDS Control			00000000	00000000	16 bit R/W			
Digital Output	00000000	00000000	00000000	00000000	32 bit R/W			
ADC Config.			0000	00000000	12 bit R/W			
Offset DAC			0000	00000000	12 bit R/W			
Bias DAC			0000	00000000	12 bit R/W			
Telemetry Config.				0000	4 bit R/W			
Auxilary Config.				00 00000000	10 bit R/W			
Redirect				0000	4 bit R/W			
Pixel Transfer				00000000	8 bit R/W			
Micro SEQ			00000000	00000000	16 bit R/W			
RAM Buffer			00000000	00000000	16 bit R/W			
LED Control				0000	4 bit R/W			
Control			00000000	00000000	16 bit R/W			
All Register Test	00000000	00000000	00000000	00000000	16 bit R/W	**Passed**	**Passed**	**Passed**

Stage 8. Bias Voltage settings and output enables testing - Table 8

DAC Bias Voltage Test Data 50% 10-90%

Value	410	2048	3686	rms Noise	Rise Time			
Signal	volts	volts	volts	uV	millisec.	Fanout Brd	Slope	Offset
Vru 0	-13.19	-5.66	1.87	<10	1	BIAS 3	217.53	3279.22
Vru 1	-13.19	-5.66	1.87	<10	1	BIAS 4	217.53	3279.22
Vru 2	-13.19	-5.66	1.87	<10	1	BIAS 5	217.53	3279.22
Vru 3	-13.17	-5.66	1.87	<10	1	BIAS 6	217.82	3279.40
Vru 4	-13.21	-5.66	1.87	<10	1	BIAS 7	217.24	3279.03
Vru 5	-13.20	-5.66	1.87	<10	1	BIAS 8	217.39	3279.13
Vru 6	-13.16	-5.66	1.87	NA	NA	BIAS 9	217.96	3279.50
Vru 7	-13.19	-5.66	1.87	NA	NA	BIAS 10	217.53	3279.22
Vrl 0	-13.20	-5.66	1.87	<10	1	BIAS 11	217.39	3279.13
Vrl 1	-13.19	-5.66	1.87	<10	1	BIAS 12	217.53	3279.22
Vrl 2	-13.20	-5.66	1.87	<10	1	BIAS 13	217.39	3279.13
Vrl 3	-13.19	-5.66	1.87	<10	1	BIAS 14	217.53	3279.22
Vrl 4	-13.19	-5.66	1.87	<10	1	BIAS 15	217.53	3279.22
Vrl 5	-13.19	-5.66	1.87	<10	1	BIAS 16	217.53	3279.22
Vrl 6	-13.19	-5.66	1.87	NA	NA	BIAS 17	217.53	3279.22
Vrl 7	-13.18	-5.66	1.87	NA	NA	BIAS 18	217.67	3279.31
Vog 0	-1.75	1.25	4.25	<10	1	BIAS 19	546.00	1365.50
Vog 1	-1.75	1.25	4.25	<10	1	BIAS 20	546.00	1365.50
Vog 2	-1.75	1.25	4.25	<10	1	BIAS 21	546.00	1365.50
Vog 3	-1.75	1.25	4.25	<10	1	BIAS 22	546.00	1365.50
Vog 4	-1.75	1.25	4.25	<10	1	BIAS 23	546.00	1365.50
Vog 5	-1.75	1.25	4.25	<10	1	BIAS 24	546.00	1365.50
Vog 6	-1.75	1.25	4.25	NA	NA	BIAS 25	546.00	1365.50
Vog 7	-1.75	1.25	4.25	NA	NA	BIAS 26	546.00	1365.50
Vdd 0	-21.93	-9.41	3.11	<10	20	BIAS 27	130.83	3279.12
Vdd 1	-21.94	-9.42	3.11	<10	20	BIAS 28	130.78	3279.50
Vdd 2	-21.98	-9.44	3.11	<10	20	BIAS 29	130.57	3280.15
Vdd 3	-22.00	-9.44	3.11	<10	20	BIAS 30	130.47	3280.03
Vdd 4	-21.96	-9.42	3.11	<10	20	BIAS 21	130.67	3279.39
Vdd 5	-21.96	-9.43	3.11	<10	20	BIAS 32	130.67	3279.82
Vdd 6	-21.99	-9.44	3.11	NA	NA	BIAS 33	130.52	3280.09
Vdd 7	-21.95	-9.42	3.11	NA	NA	BIAS 34	130.73	3279.44

Vru	Slope		Offset
Mean	217.57	Mean	3279.24
Stdev	0.2137491	Stdev	0.136506109
Average	217.56613	Average	3279.241965
	Dac #	Average voltage	
	0	-15.0	
	4095	3.8	

Vrl	Slope		Offset
Mean	217.51	Mean	3279.21
Stdev	0.0865817	Stdev	0.055433101
Average	217.51185	Average	3279.207523
	Dac #	Average voltage	
	0	-15.1	
	4095	3.8	

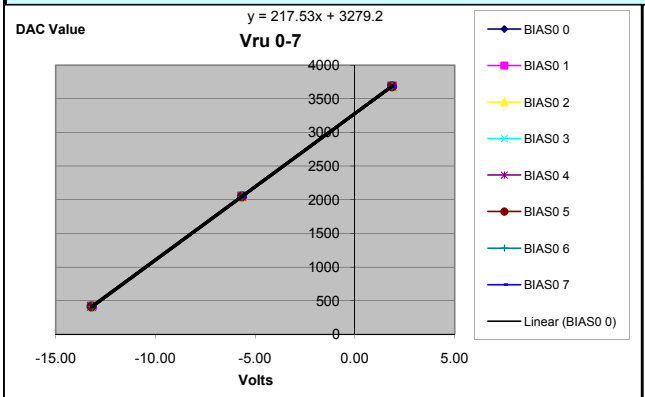
Vog	Slope		Offset
Mean	546.00	Mean	1365.50
Stdev	0	Stdev	0
Average	546	Average	1365.5
	Dac #	Average voltage	
	0	-2.5	
	4095	5.0	

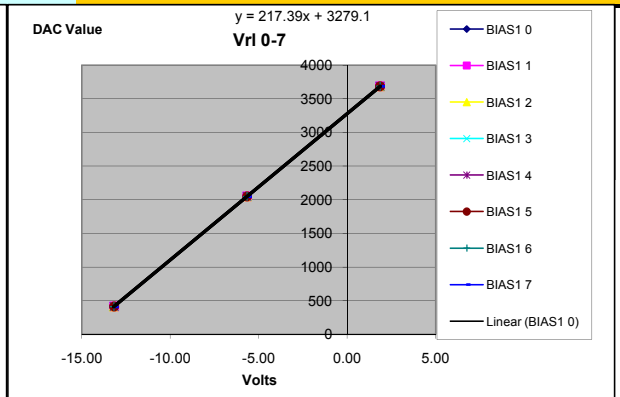
Vdd	Slope		Offset
Mean	130.65	Mean	3279.69
Stdev	0.1192003	Stdev	0.357431735
Average	130.65467	Average	3279.691178
	Dac #	Average voltage	
	0	-25.1	
	4095	6.2	

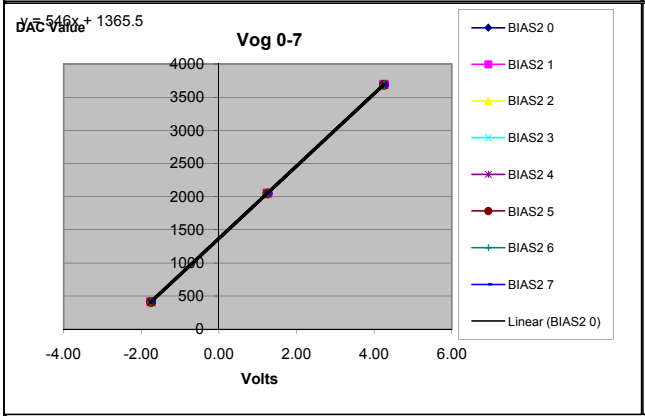
Notes and Observations

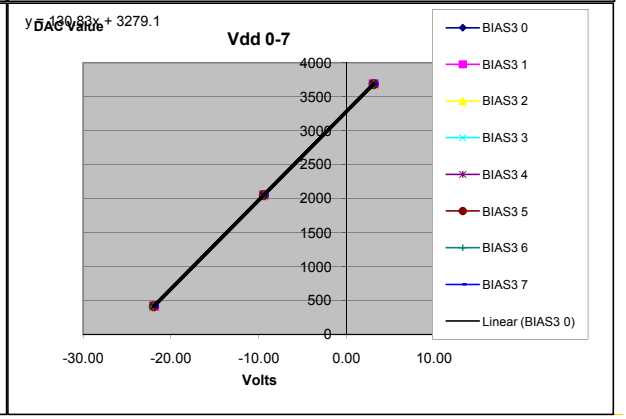
Checked for oscillations using a Agilent Oscilloscpe on AC.**OK**

average min & max voltages
(dac# -offset)/slope=voltage









Stage 8B. Telemetry System Tests - Table 7 (Bias Telemetry Tests)

DAC Value	410	3686	Bias Signals Set Volts		Resolved Values for Telemetry Channel	
	Telemetry Return Values					
Signal	10%	90%	10%	90%	Slope	Offset
Vru 0	-1754	423	-13.19	1.87	144.5551	152.68
Vru 1	-1754	422	-13.19	1.87	144.4887	151.81
Vru 2	-1757	423	-13.19	1.87	144.7543	152.31
Vru 3	-1754	422	-13.17	1.87	144.6809	151.45
Vru 4	-1758	422	-13.21	1.87	144.5623	151.67
Vru 5	-1757	422	-13.20	1.87	144.5919	151.61
Vru 6	-1759	423	-13.16	1.87	145.1763	151.52
Vru 7	-1755	422	-13.19	1.87	144.5551	151.68
Vrl 0	-1760	422	-13.20	1.87	144.7910	151.24
Vrl 1	-1757	422	-13.19	1.87	144.6879	151.43
Vrl 2	-1758	423	-13.20	1.87	144.7246	152.36
Vrl 3	-1760	422	-13.19	1.87	144.8871	151.06
Vrl 4	-1759	423	-13.19	1.87	144.8871	152.06
Vrl 5	-1754	422	-13.19	1.87	144.4887	151.81
Vrl 6	-1761	422	-13.19	1.87	144.9535	150.94
Vrl 7	-1758	423	-13.18	1.87	144.9169	152.01
Vog 0	-361	868	-1.75	4.25	204.8333	-2.54
Vog 1	-362	867	-1.75	4.25	204.8333	-3.54
Vog 2	-362	868	-1.75	4.25	205.0000	-3.25
Vog 3	-361	868	-1.75	4.25	204.8333	-2.54
Vog 4	-361	868	-1.75	4.25	204.8333	-2.54
Vog 5	-362	868	-1.75	4.25	205.0000	-3.25
Vog 6	-362	868	-1.75	4.25	205.0000	-3.25
Vog 7	-361	868	-1.75	4.25	204.8333	-2.54
Vdd 0	-1723	573	-21.93	3.11	91.6933	287.83
Vdd 1	-1718	574	-21.94	3.11	91.4970	289.44
Vdd 2	-1730	574	-21.98	3.11	91.8294	288.41
Vdd 3	-1719	574	-22.00	3.11	91.3182	290.00
Vdd 4	-1728	574	-21.96	3.11	91.8229	288.43
Vdd 5	-1725	574	-21.96	3.11	91.7032	288.80
Vdd 6	-1729	574	-21.99	3.11	91.7530	288.65
Vdd 7	-1724	574	-21.95	3.11	91.6999	288.81

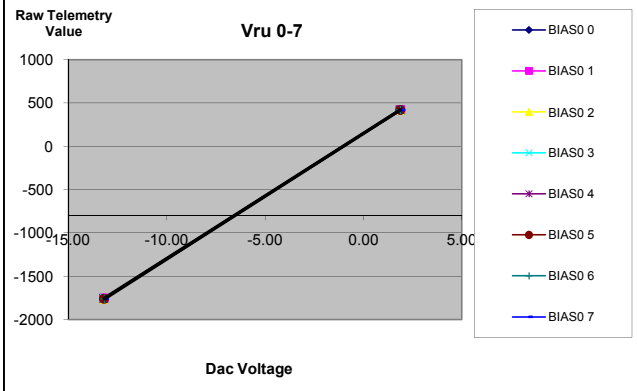
AVERAGE

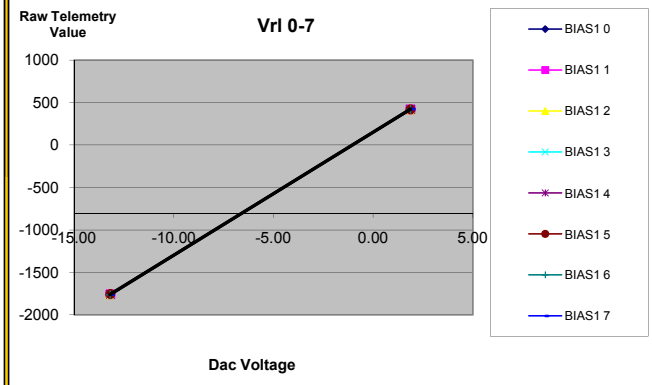
Vru	Slope		Offset
Mean	144.67	Mean	151.84
Stdev	0.2063166	Stdev	0.4020356

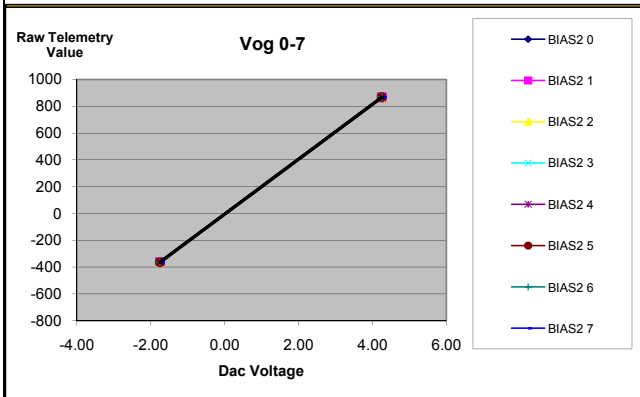
Vrl	Slope		Offset
Mean	144.79	Mean	151.61
Stdev	0.144548	Stdev	0.4860277

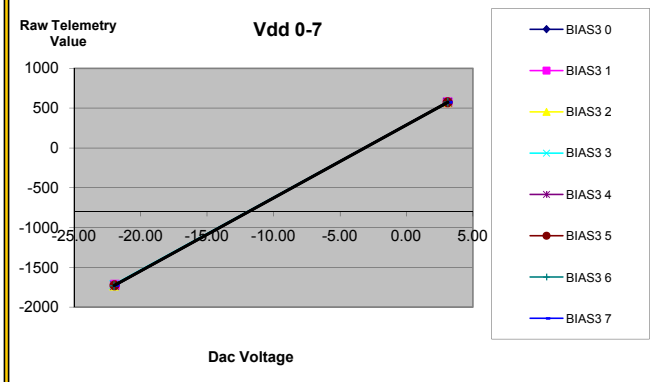
Vog	Slope		Offset
Mean	204.90	Mean	-2.93
Stdev	0.0806872	Stdev	0.4007033

Vdd	Slope		Offset
Mean	91.66	Mean	288.80
Stdev	0.1626643	Stdev	0.6225662









Stage 8C. Bias Voltage output enables testing - Table 8

Place a line through Bias Voltage name if enable/disable switch works

Vru 0	Vru 1	Vru 2	Vru 3	Vru 4	Vru 5
Vrl 0	Vrl 1	Vrl 2	Vrl 3	Vrl 4	Vrl 5
Vog 0	Vog 1	Vog 2	Vog 3	Vog 4	Vog 5
Vdd 0	Vdd 1	Vdd 2	Vdd 3	Vdd 4	Vdd 5

Stage 9. Vsub and Heater Control testing - Table 9

DAC Value	Vsub Measured Voltage Test Data 10%	50%	90%
Signal	volts	volts	volts
Vsub - rate	-1.24	3.79	8.82
Vsub - Limit	-1.24	3.79	8.82
Vsub0	0.00	0.00	0.00
	Vsub Enable Bit - pass		

DAC Value	Telemetery Readback Test Data 10%	50%	90%
Signal	dec	dec	dec
Vbias 0	155	279	449
Vbias 1	-27	700	1427
RTD1	219	NA	NA
RTD2	247	NA	NA
RTD3	274	NA	NA
RTD4	302	NA	NA
RTD5	327	NA	NA
RTD6	352	NA	NA
Reference 4096	836	NA	NA
eference buffere	836	NA	NA

Stage 10. Video Offset DAC Tests - Table 10.

	DAC Value 410				DAC Value 2048				DAC Value 3686			
ADC	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU
0	0.250	NA	NA	17008	1.250		NA	81046	2.250	NA	500ms	145084
1	0.250	NA	NA	17070	1.250		NA	81088	2.250	NA	500ms	145110
2	0.250	NA	NA	17076	1.250		NA	81124	2.250	NA	500ms	145183
3	0.250	NA	NA	17340	1.250		NA	81246	2.250	NA	500ms	145144
4	0.250	NA	NA	17173	1.250		NA	81152	2.250	NA	500ms	145136
5	0.250	NA	NA	17167	1.250		NA	81213	2.250	NA	500ms	145251
6	0.250	NA	NA	17023	1.250		NA	81107	2.250	NA	500ms	145196
7	0.250	NA	NA	17051	1.250		NA	81136	2.250	NA	500ms	145220
8	0.250	NA	NA	17159	1.250		NA	81204	2.250	NA	500ms	145249
9	0.250	NA	NA	17125	1.250		NA	81144	2.250	NA	500ms	145170
10	0.250	NA	NA	17207	1.250		NA	81240	2.250	NA	500ms	145273
11	0.250	NA	NA	17021	1.250		NA	81037	2.250	NA	500ms	145057

ADC	DC Volts		Data Set		
Channel	Slope	Offset	410	2048	3686
0	1638.000	0.500	0.250	1.250	2.250
1	1638.000	0.500	0.250	1.250	2.250
2	1638.000	0.500	0.250	1.250	2.250
3	1638.000	0.500	0.250	1.250	2.250
4	1638.000	0.500	0.250	1.250	2.250
5	1638.000	0.500	0.250	1.250	2.250
6	1638.000	0.500	0.250	1.250	2.250
7	1638.000	0.500	0.250	1.250	2.250
8	1638.000	0.500	0.250	1.250	2.250
9	1638.000	0.500	0.250	1.250	2.250
10	1638.000	0.500	0.250	1.250	2.250
11	1638.000	0.500	0.250	1.250	2.250

(dac# -offset)/slope=Voltage

ADC	ADU's		Data Set		
Channel	Slope	Offset	410	2048	3686
0	0.026	-25.04	17008	81046	145084
1	0.026	-26.73	17070	81088	145110
2	0.026	-26.63	17076	81124	145183
3	0.026	-34.51	17340	81246	145144
4	0.026	-29.63	17173	81152	145136
5	0.026	-29.11	17167	81213	145251
6	0.026	-25.07	17023	81107	145196
7	0.026	-25.83	17051	81136	145220
8	0.026	-28.85	17159	81204	145249
9	0.026	-28.11	17125	81144	145170
10	0.026	-30.16	17207	81240	145273
11	0.026	-25.49	17021	81037	145057

(dac# -offset)/slope=ADU

Notes and Observations

Checked for oscillations using a Agilent Oscilloscope on AC. OK

Stage 11. CDS Control Functions and Video Channel Performanc

TEST #1: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit is held static. The purpose of this test is to verify the correct operation of the ADC devices and measure the noise of the Offset voltage generators, ADC buffer amplifiers and ADC devices

Noise Test 1

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	81034	81052	81043.1	2.30483
CH 1	81082	81098	81090	2.27335
CH 2	81117	81133	81124.4	2.23147
CH 3	81236	81253	81243.6	2.37727
CH 4	81146	81162	81154	2.10598
CH 5	81198	81215	81206.3	2.31995
CH 6	81095	81113	81105.6	2.27609
CH 7	81129	81144	81136.3	2.37212
CH 8	81197	81212	81204.2	2.20018
CH 9	81139	81157	81148	2.29906
CH 10	81232	81249	81239.9	2.30099
CH 11	81030	81049	81038.7	2.36419

TEST #2: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the invert/non-invert and the DC Restore switches are held static.

Noise Test 2

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76340	76360	76348.7	2.75196
CH 1	76626	76647	76636.8	2.84961
CH 2	76513	76532	76522.8	2.81449
CH 3	77179	77199	77188.9	2.74369
CH 4	76478	76496	76486.7	2.69928
CH 5	76917	76936	76927.1	2.70275
CH 6	76875	76895	76884.9	2.80762
CH 7	77006	77026	77016.4	2.82909
CH 8	76391	76410	76400.5	2.78089
CH 9	77121	77141	77131.6	2.84022
CH 10	76595	76615	76604.8	2.78598
CH 11	76731	76752	76742.6	2.87497

TEST #3: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the DC Restore switch is held static.

Noise Test 3

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76343	76364	76353.6	2.99182
CH 1	76625	76646	76635.6	3.04726
CH 2	76507	76529	76516.5	3.02344
CH 3	77185	77206	77195.4	3.05865
CH 4	76471	76491	76481.6	2.94309
CH 5	76914	76936	76925.1	3.02279
CH 6	76864	76883	76874.1	3.01938
CH 7	77008	77029	77019.6	3.0066
CH 8	76384	76406	76394.8	3.03578
CH 9	77125	77145	77135.4	2.97657
CH 10	76599	76622	76610.4	3.01503
CH 11	76727	76749	76738.2	3.08184

TEST #4: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition.

Noise Test 4

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76329	76349	76339.7	2.86995
CH 1	76625	76646	76635.9	3.16003
CH 2	76508	76530	76519.2	3.17398
CH 3	77184	77205	77195.1	3.15222
CH 4	76514	76536	76524.9	3.12912
CH 5	76896	76919	76905.8	3.16802
CH 6	76876	76899	76887.8	3.15718
CH 7	76957	76978	76967.1	3.13864
CH 8	76432	76456	76444.8	3.18378
CH 9	77018	77040	77027.9	2.99677
CH 10	76617	76640	76629.1	3.16088
CH 11	76677	76700	76687.4	3.12671

TEST #5: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the circuitry set to high GAIN.

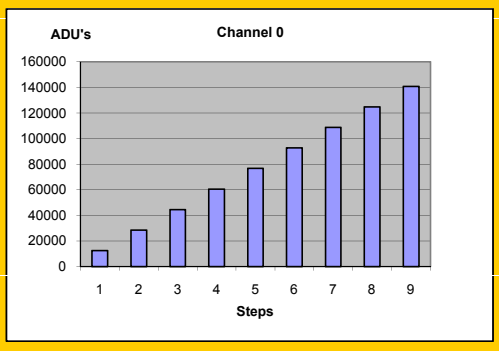
Noise Test 5

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76325	76351	76339.1	3.5496
CH 1	76640	76666	76654.5	3.72016
CH 2	76513	76542	76528.5	3.62703
CH 3	77184	77211	77197.1	3.70467
CH 4	76515	76542	76529.5	3.82714
CH 5	76889	76918	76904.1	3.6004
CH 6	76876	76901	76888.4	3.67469
CH 7	76954	76983	76969.2	3.72402
CH 8	76494	76524	76507.9	3.78402
CH 9	77017	77046	77028.6	3.5006
CH 10	76686	76712	76698.8	3.73933
CH 11	76672	76699	76687.2	3.59577

TEST #6A: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

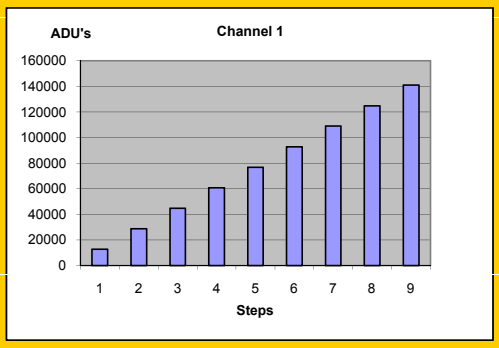
BrdTst6_006 / Channel 0					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12602	12626	12614	3.15787	10%
0x333	28590	28612	28602	3.11889	20%
0x4cc	44584	44610	44594.7	3.0339	30%
0x666	60610	60634	60622.4	3.11912	40%
0x800	76642	76664	76654.1	3.10786	50%
0x999	92634	92656	92644.5	2.90511	60%
0xb33	108661	108684	108673	3.15588	70%
0xccc	124656	124680	124669	3.12661	80%
0xe66	140686	140707	140697	3.15984	90%



TEST #6B: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

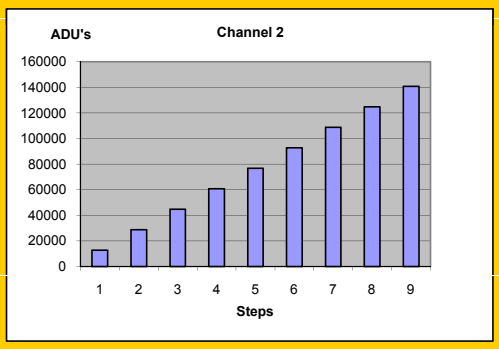
BrdTst6_006 / Channel 1					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12855	12879	12867.2	3.24665	10%
0x333	28841	28865	28852.7	3.16635	20%
0x4cc	44825	44848	44836.7	3.15221	30%
0x666	60847	60870	60860.1	3.17525	40%
0x800	76872	76893	76882	3.05519	50%
0x999	92855	92880	92868.7	3.12867	60%
0xb33	108880	108903	108892	3.20541	70%
0xccc	124868	124892	124879	3.30718	80%
0xe66	140892	140914	140903	3.20781	90%



TEST #6C: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

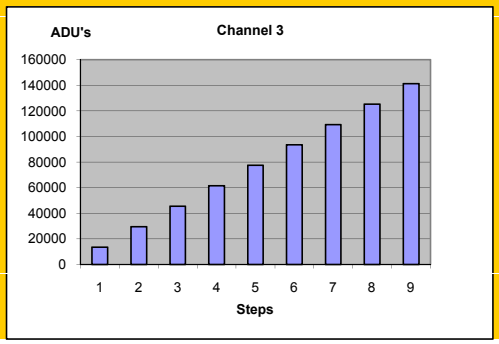
BrdTst6_006 / Channel 2					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12756	12780	12767.5	3.12587	10%
0x333	28748	28770	28759	3.13865	20%
0x4cc	44741	44766	44753.9	3.21352	30%
0x666	60773	60797	60785.3	3.07471	40%
0x800	76809	76831	76820.1	3.06555	50%
0x999	92805	92826	92815.9	3.13042	60%
0xb33	108837	108860	108848	3.14522	70%
0xccc	124834	124857	124846	3.14765	80%
0xe66	140865	140890	140879	3.19942	90%



TEST #6D: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

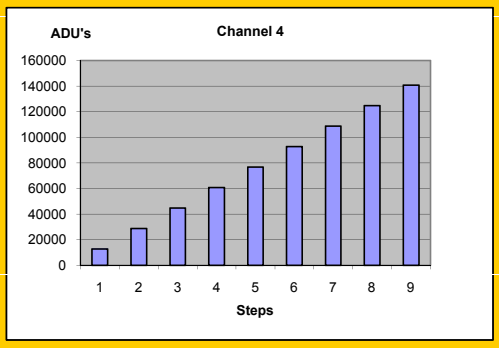
BrdTst6_006 / Channel 3					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13522	13544	13533.4	3.20405	10%
0x333	29477	29501	29488.7	3.23158	20%
0x4cc	45431	45457	45444.7	3.16707	30%
0x666	61428	61449	61438	3.09839	40%
0x800	77422	77444	77433	3.21221	50%
0x999	93376	93398	93387.3	3.16426	60%
0xb33	109370	109392	109382	3.07594	70%
0xccc	125328	125351	125340	3.18744	80%
0xe66	141324	141347	141335	3.16625	90%



TEST #6E: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

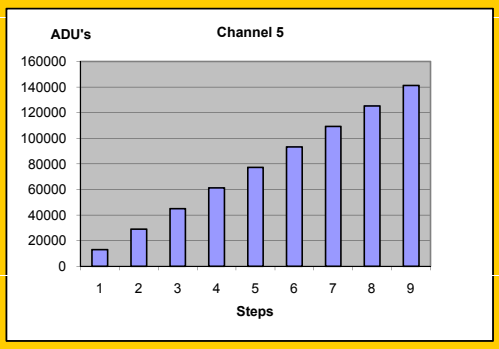
BrdTst6_006 / Channel 4					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12832	12853	12843.1	3.15849	10%
0x333	28805	28829	28818.5	3.16206	20%
0x4cc	44779	44803	44791.8	3.08919	30%
0x666	60796	60820	60806.8	3.1078	40%
0x800	76813	76835	76824.2	3.16736	50%
0x999	92792	92813	92802.8	2.99104	60%
0xb33	108805	108828	108818	2.98506	70%
0xccc	124782	124806	124794	3.22201	80%
0xe66	140799	140822	140809	3.15543	90%



TEST #6F: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

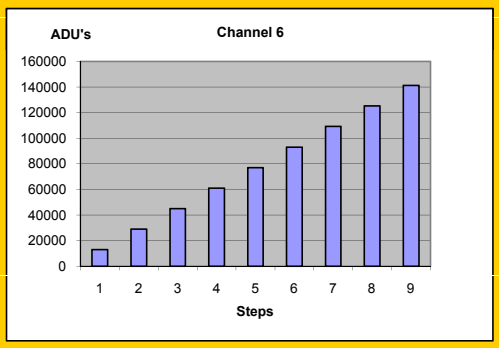
BrdTst6_006 / Channel 5					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13121	13144	13133.4	3.14484	10%
0x333	29115	29136	29125.6	3.0363	20%
0x4cc	45100	45125	45111.7	3.1072	30%
0x666	61132	61154	61142.8	3.08925	40%
0x800	77158	77180	77169	3.14157	50%
0x999	93150	93172	93159.8	3.07467	60%
0xb33	109180	109202	109192	3.21239	70%
0xccc	125168	125192	125180	3.18065	80%
0xe66	141202	141223	141212	3.23163	90%



TEST #6G: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

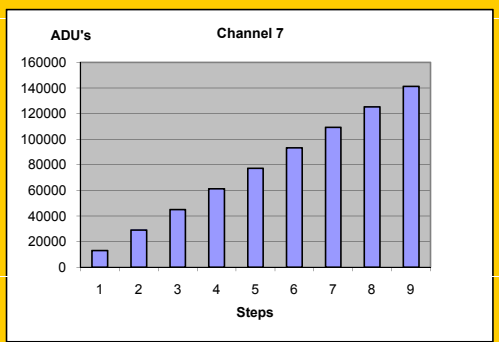
BrdTst6_006 / Channel 6					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13029	13050	13039.5	3.08469	10%
0x333	29029	29053	29040.4	3.16225	20%
0x4cc	45030	45051	45041	3.11241	30%
0x666	61069	61092	61080.1	3.12984	40%
0x800	77109	77133	77120.7	3.08461	50%
0x999	93113	93137	93123.4	3.17633	60%
0xb33	109151	109174	109163	3.17248	70%
0xccc	125156	125178	125166	3.15939	80%
0xe66	141194	141218	141207	3.21739	90%



TEST #6H: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

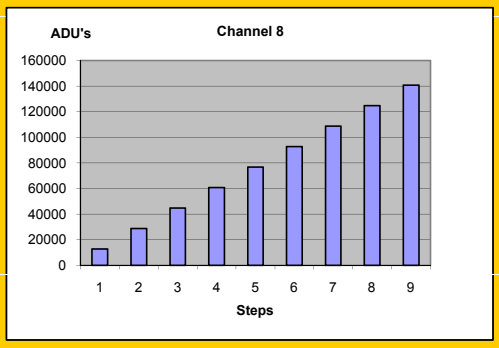
BrdTst6_006 / Channel 7					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13120	13143	13132.1	3.20283	10%
0x333	29122	29144	29133.6	3.09433	20%
0x4cc	45123	45146	45134.5	3.0704	30%
0x666	61163	61186	61174.7	3.16014	40%
0x800	77202	77225	77213.8	3.11976	50%
0x999	93204	93226	93215.1	3.06158	60%
0xb33	109245	109267	109256	3.07906	70%
0xccc	125249	125273	125261	3.16924	80%
0xe66	141290	141314	141301	3.18994	90%



TEST #6I: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

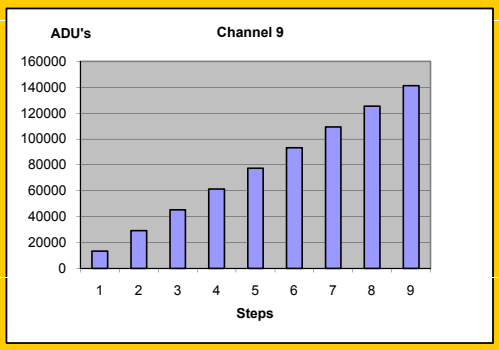
BrdTst6_006 / Channel 8					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12681	12706	12692.2	3.19472	10%
0x333	28675	28697	28684.9	3.18162	20%
0x4cc	44664	44686	44674.2	3.09208	30%
0x666	60692	60715	60704.1	3.18051	40%
0x800	76724	76746	76735.5	3.21282	50%
0x999	92714	92739	92728.9	3.23292	60%
0xb33	108749	108774	108761	3.23214	70%
0xccc	124742	124766	124753	3.17351	80%
0xe66	140774	140796	140785	3.20022	90%



TEST #6J: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

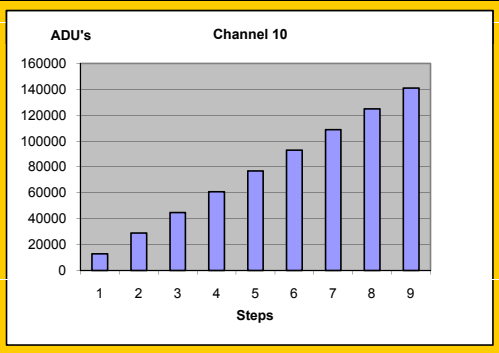
BrdTst6_006 / Channel 9					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13269	13291	13279.9	3.20916	10%
0x333	29255	29277	29265.8	2.99974	20%
0x4cc	45241	45263	45250.8	2.96639	30%
0x666	61264	61286	61276	3.13703	40%
0x800	77288	77312	77300	2.95429	50%
0x999	93275	93300	93288.7	3.1946	60%
0xb33	109305	109327	109316	3.13022	70%
0xccc	125290	125314	125303	3.18263	80%
0xe66	141318	141340	141329	3.08182	90%



TEST #6K: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

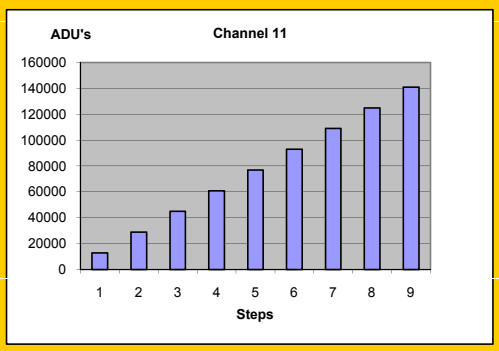
BrdTst6_006 / Channel 10					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12866	12891	12879.1	3.08365	10%
0x333	28858	28880	28869.3	3.06736	20%
0x4cc	44842	44865	44853.8	3.19724	30%
0x666	60871	60894	60882.1	3.15366	40%
0x800	76905	76928	76914.7	3.09178	50%
0x999	92896	92919	92907.7	3.15597	60%
0xb33	108926	108948	108937	3.09741	70%
0xccc	124914	124936	124924	3.14595	80%
0xe66	140942	140964	140954	3.16912	90%



TEST #6L: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

BrdTst6_006 / Channel 11					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12934	12960	12947.1	3.06488	10%
0x333	28922	28945	28933	3.13373	20%
0x4cc	44906	44930	44916.9	3.08457	30%
0x666	60931	60954	60941.8	3.22935	40%
0x800	76952	76974	76963.4	2.93521	50%
0x999	92938	92964	92951.1	3.14849	60%
0xb33	108965	108989	108977	3.03836	70%
0xccc	124950	124976	124964	3.08728	80%
0xe66	140978	141000	140989	3.2242	90%



Stage 13. Other Bit Tests. Table 11

Electronic Serial Number	0xDB8EBD		Board Serial Number	29
Firmware Version	0x193		Name Of Person Testing	S. Holm
Ident Register	0x502		Board passed Functional Tests	YES