DES 12 Channel Board - Functional Tests: CCD Acquisition Board Revision 1.0

Stage 1. Preparation of documentation and configuration settings - Table 1.

Board Part Number	15	Board Serial Number	0xDB8F6C
Date Of Tests	August 2010	Name Of Person Testing	S. Holm
Suggested Filename To Save	CCDACQ_12Ch_REPORT_BOARD12.xl	Sequence number: Test	

Stage 3. Power plane short test - Table 2.

Supply Name	Short test to ground: Impedance to ground	Test Point	
+1.2VD	33.00	TP43	~50 ohms
+1.8VD	2M	TPB12	> 1K ohm
+2.5VD	18k	TPB11	> 1K ohm
+3.3VD	6k	D13	> 1K ohm
+5VD	18k	D14	> 1K ohm
+5VA	4M	C267	> 1K ohm
-5VA	300K	C270	> 1K ohm
+15VA	500K	C288	> 1K ohm
-15VA	500K	C282	> 1K ohm
-28VA	2.5M	C307	> 1K ohm

Stage 4. Firmware programming tests - Table 3.

JTAG Order	Designator	Device	Load File	Check Sum or User Code
1	U122	XCF08PFS48C PROM	CcdAcqFpgaV41.mcs	0014ef670
2	U114	Spartan3 XC3S2000 FPGA	ccdacqfpgav41.bit	5102801

Stage 5. Power Consumption - Table 4.

Supply Name	Power Supply Consumption: Measured Voltage at test point	Measured Current on power supply	Test Point	
+1.2VD	1.20	N/A	TP43	
+1.8VD	1.80	N/A	TPB12	
+2.5VD	2.50	N/A	TPB11	
+3.3VD	3.29	0.258	D13	
+5VD	5.20	0.163	D14	
+5VA	4.89	0.596	C267	
-5VA	-5.00	0.437	C270	
+15VA	14.96	0.558	C288	
-15VA	-15.06	0.437	C282	
-28VA	-27.84	0.219	C307	
Vref 0+	10.07	N/A	R534	Vsub+ Reference(+10v)
Vref 0-	-2.51	N/A	R525	Vsub - Reference(-2.5v)
Vref Offset	2.50	N/A	R573	ADC Offset Reference(+2.5v)
Vclamp	1.87	N/A	VIA	ADC Clamp Voltage(+1.8v)
ADC Ref.	2.50	N/A	VIA	ADC Reference Voltage(+2.5v)
Vref 1+	2.50	N/A	R537	Vru and Vrl + Reference(+2.5v)
Vref 1-	-10.07	N/A	R535	Vru and Vrl - Reference(-10v)
Vref 2+	5.01	N/A	R563	Vog + Reference(+5v)
Vref 2-	-2.51	N/A	R555	Vog - Reference(-2.5v)
Vref 3+	2.50	N/A	R543	Vdd + Reference(+2.5v)
Vref 3-	-10.10	N/A	R571	Vdd - Reference(-10v)

Power Dissipation:
27.8 Watts

~27 watts +/- 5%

Stage 7. Basic Bus Transactions - **D**igital **Register** Tests - Table 5.

Register name	Put an X on any bit that has an error: 31-24	23-16	15-08	07-00	Function	Test name: Pattern	Walking 0's	Walking 1's
CDS Control			00000000	00000000	16 bit R/W			
Digital Output	00000000	00000000	00000000	00000000	32 bit R/W			
ADC Config.			0000	00000000	12 bit R/W			
Offset DAC			0000	00000000	12 bit R/W			
Bias DAC			0000	00000000	12 bit R/W			
Telemetry Config.				0000	4 bit R/W			
Auxilary Config.			00	00000000	10 bit R/W			
Redirect				0000	4 bit R/W			
Pixel Transfer				00000000	8 bit R/W			
Micro SEQ			00000000	00000000	16 bit R/W			
RAM Buffer			00000000	00000000	16 bit R/W			
LED Control				0000	4 bit R/W			
Control			00000000	00000000	16 bit R/W			
All Register Test	00000000	00000000	00000000	00000000	16 bit R/W	**Passed**	**Passed**	**Passed**

Stage 8. Bias Voltage settings and output enables testing - Table 8

DAC Value	410	Bias Voltage Test Data 2048	3686	50% rms Noise	10-90% Rise Time			
Signal	volts	volts	volts	uV	millisec.	Fanout Brd	Slope	Offset
Vru 0	-13.23	-5.68	1.86	<10	1	BIAS 3	217.10	3281.84
Vru 1	-13.23	-5.68	1.86	<10	1	BIAS 4	217.10	3281.84
Vru 2	-13.23	-5.68	1.86	<10	1	BIAS 5	217.10	3281.84
Vru 3	-13.23	-5.68	1.86	<10	1	BIAS 6	217.10	3281.84
Vru 4	-13.23	-5.68	1.86	<10	1	BIAS 7	217.10	3281.84
Vru 5	-13.23	-5.68	1.86	<10	1	BIAS 8	217.10	3281.84
Vru 6	-13.23	-5.68	1.86	NA	NA	BIAS 9	217.10	3281.84
Vru 7	-13.23	-5.68	1.86	NA	NA	BIAS 10	217.10	3281.84
Vrl 0	-13.23	-5.68	1.86	<10	1	BIAS 11	217.10	3281.84
Vrl 1	-13.23	-5.68	1.86	<10	1	BIAS 12	217.10	3281.84
Vrl 2	-13.23	-5.68	1.86	<10	1	BIAS 13	217.10	3281.84
Vrl 3	-13.23	-5.68	1.86	<10	1	BIAS 14	217.10	3281.84
Vrl 4	-13.23	-5.68	1.86	<10	1	BIAS 15	217.10	3281.84
Vrl 5	-13.23	-5.68	1.86	<10	1	BIAS 16	217.10	3281.84
Vrl 6	-13.23	-5.68	1.86	NA	NA	BIAS 17	217.10	3281.84
Vrl 7	-13.23	-5.68	1.86	NA	NA	BIAS 18	217.10	3281.84
Vog 0	-1.76	1.25	4.26	<10	1	BIAS 19	544.19	1367.77
Vog 1	-1.76	1.25	4.26	<10	1	BIAS 20	544.19	1367.77
Vog 2	-1.76	1.25	4.26	<10	1	BIAS 21	544.19	1367.77
Vog 3	-1.76	1.25	4.26	<10	1	BIAS 22	544.19	1367.77
Vog 4	-1.76	1.25	4.26	<10	1	BIAS 23	544.19	1367.77
Vog 5	-1.76	1.25	4.26	<10	1	BIAS 24	544.19	1367.77
Vog 6	-1.76	1.25	4.26	NA	NA	BIAS 25	544.19	1367.77
Vog 7	-1.76	1.25	4.26	NA	NA	BIAS 26	544.19	1367.77
Vdd 0	-22.11	-9.51	3.09	<10	20	BIAS 27	130.00	3284.30
Vdd 1	-22.17	-9.54	3.10	<10	20	BIAS 28	129.64	3284.33
Vdd 2	-22.17	-9.54	3.10	<10	20	BIAS 29	129.64	3284.33
Vdd 3	-22.08	-9.50	3.09	<10	20	BIAS 30	130.15	3284.04
Vdd 4	-22.10	-9.51	3.10	<10	20	BIAS 21	130.00	3283.43
Vdd 5	-22.05	-9.48	3.09	<10	20	BIAS 32	130.31	3283.34
Vdd 6	-22.05	-9.48	3.09	NA	NA	BIAS 33	130.31	3283.34
Vdd 7	-22.10	-9.50	3.10	NA	NA	BIAS 34	130.00	3283.00

Vru	Slope		Offset
Mean	217.10	Mean	3281.84
Stdev	2.842E-14	Stdev	0
Average	217.09738	Average	3281.836798
	Dac #	Average voltage	
	0	-15.0	
	4095	3.8	

Vrl	Slope		Offset
Mean	217.10	Mean	3281.84
Stdev	2.842E-14	Stdev	0
Average	217.09738	Average	3281.836798
	Dac #	Average voltage	
	0	-15.1	
	4095	3.8	

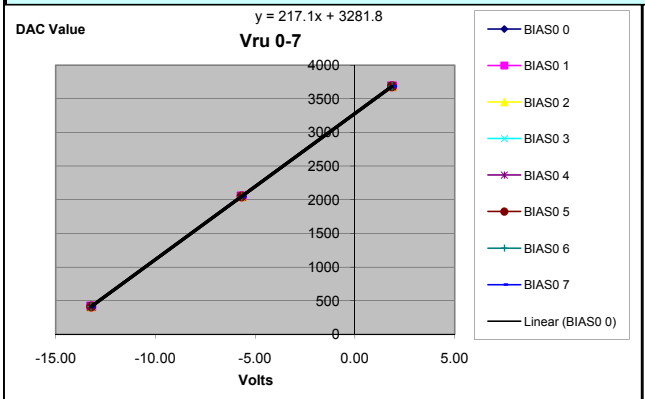
Vog	Slope		Offset
Mean	544.19	Mean	1367.77
Stdev	0	Stdev	2.27374E-13
Average	544.18605	Average	1367.767442
	Dac #	Average voltage	
	0	-2.5	
	4095	5.0	

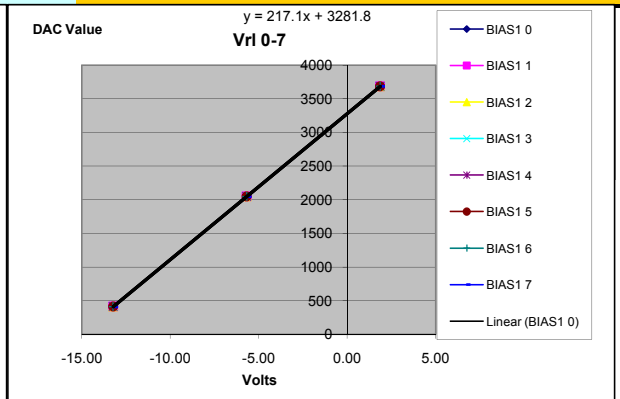
Vdd	Slope		Offset
Mean	130.01	Mean	3283.76
Stdev	0.2438033	Stdev	0.507323733
Average	130.0069	Average	3283.764802
	Dac #	Average voltage	
	0	-25.3	
	4095	6.2	

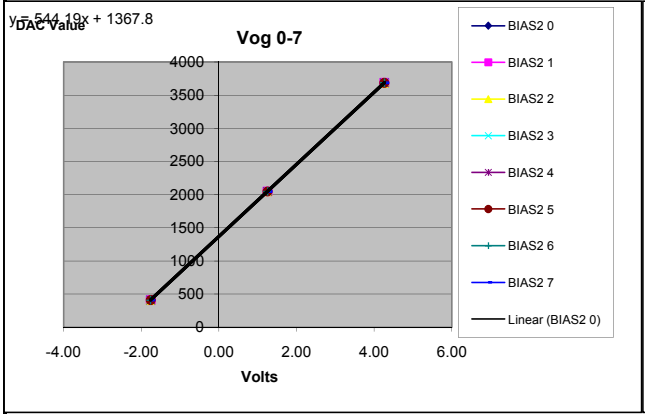
Notes and Observations

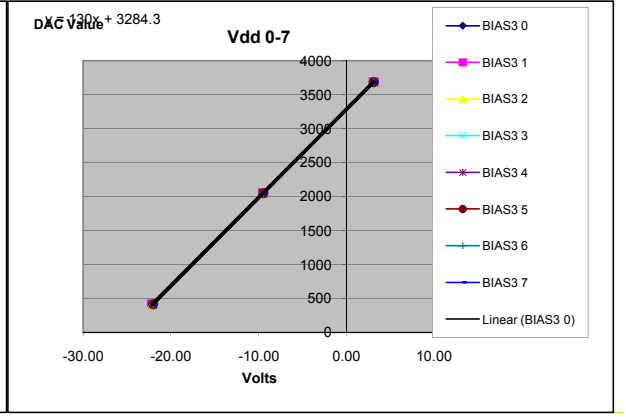
Checked for oscillations using a Agilent Oscilloscpe on AC.**OK**

average min & max voltages
(dac# -offset)/slope=voltage









Stage 8B. Telemetry System Tests - Table 7 (Bias Telemetry Tests)

DAC Value	410	3686	Bias Signals Set Volts		Resolved Values for Telemetry Channel	
	Telemetry Return Values					
Signal	10%	90%	10%	90%	Slope	Offset
Vru 0	-1757	422	-13.23	1.86	144.4003	153.42
Vru 1	-1760	422	-13.23	1.86	144.5991	153.05
Vru 2	-1757	422	-13.23	1.86	144.4003	153.42
Vru 3	-1759	422	-13.23	1.86	144.5328	153.17
Vru 4	-1757	422	-13.23	1.86	144.4003	153.42
Vru 5	-1762	422	-13.23	1.86	144.7316	152.80
Vru 6	-1760	422	-13.23	1.86	144.5991	153.05
Vru 7	-1762	422	-13.23	1.86	144.7316	152.80
Vrl 0	-1760	422	-13.23	1.86	144.5991	153.05
Vrl 1	-1762	422	-13.23	1.86	144.7316	152.80
Vrl 2	-1759	421	-13.23	1.86	144.4665	152.29
Vrl 3	-1759	422	-13.23	1.86	144.5328	153.17
Vrl 4	-1762	422	-13.23	1.86	144.7316	152.80
Vrl 5	-1762	422	-13.23	1.86	144.7316	152.80
Vrl 6	-1761	422	-13.23	1.86	144.6653	152.92
Vrl 7	-1763	422	-13.23	1.86	144.7979	152.68
Vog 0	-364	870	-1.76	4.26	204.9834	-3.23
Vog 1	-363	871	-1.76	4.26	204.9834	-2.23
Vog 2	-364	871	-1.76	4.26	205.1495	-2.94
Vog 3	-363	871	-1.76	4.26	204.9834	-2.23
Vog 4	-364	871	-1.76	4.26	205.1495	-2.94
Vog 5	-364	871	-1.76	4.26	205.1495	-2.94
Vog 6	-363	871	-1.76	4.26	204.9834	-2.23
Vog 7	-364	871	-1.76	4.26	205.1495	-2.94
Vdd 0	-1736	572	-22.11	3.09	91.5873	289.00
Vdd 1	-1740	573	-22.17	3.10	91.5315	289.25
Vdd 2	-1740	573	-22.17	3.10	91.5315	289.25
Vdd 3	-1734	572	-22.08	3.09	91.6170	288.90
Vdd 4	-1735	572	-22.10	3.10	91.5476	288.20
Vdd 5	-1739	572	-22.05	3.09	91.9252	287.95
Vdd 6	-1726	572	-22.05	3.09	91.4081	289.55
Vdd 7	-1739	573	-22.10	3.10	91.7460	288.59

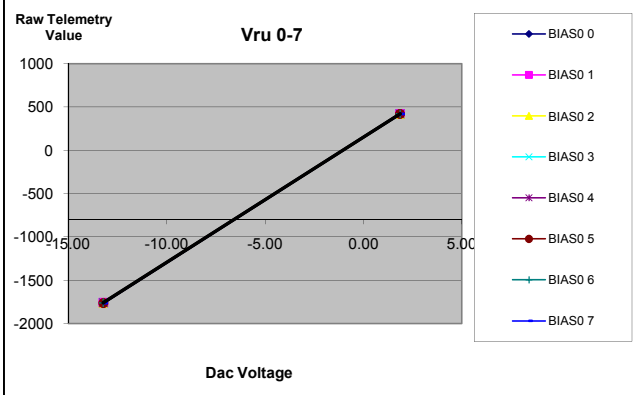
AVERAGE

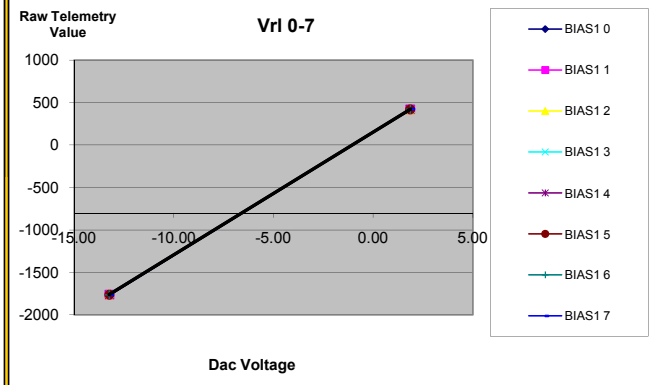
Vru	Slope		Offset
Mean	144.55	Mean	153.14
Stdev	0.1314986	Stdev	0.2445873

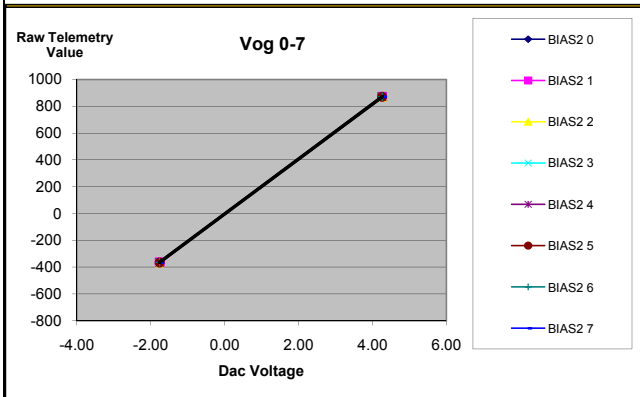
Vrl	Slope		Offset
Mean	144.66	Mean	152.81
Stdev	0.1070481	Stdev	0.2458173

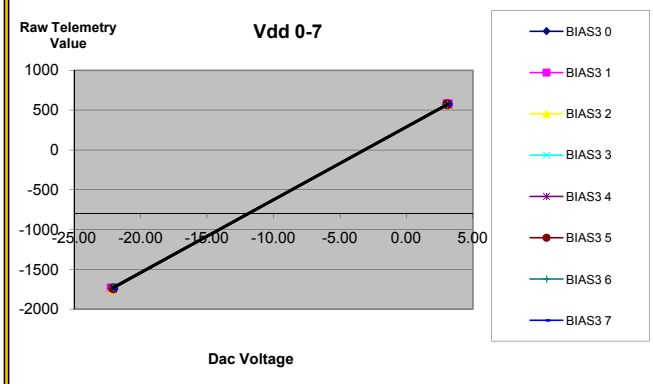
Vog	Slope		Offset
Mean	205.07	Mean	-2.71
Stdev	0.0830565	Stdev	0.3822419

Vdd	Slope		Offset
Mean	91.61	Mean	288.84
Stdev	0.1480678	Stdev	0.516174









Stage 8C. Bias Voltage output enables testing - Table 8

Place a line through Bias Voltage name if enable/disable switch works

Vru 0	Vru 1	Vru 2	Vru 3	Vru 4	Vru 5
Vrl 0	Vrl 1	Vrl 2	Vrl 3	Vrl 4	Vrl 5
Vog 0	Vog 1	Vog 2	Vog 3	Vog 4	Vog 5
Vdd 0	Vdd 1	Vdd 2	Vdd 3	Vdd 4	Vdd 5

Stage 9. Vsub and Heater Control testing - Table 9

DAC Value	Vsub Measured Voltage Test Data 10%	50%	90%
Signal	volts	volts	volts
Vsub - rate	-1.25	3.77	8.78
Vsub - Limit	-1.25	3.77	8.78
Vsub0	0.00	0.00	0.00
	Vsub Enable Bit - pass		

DAC Value	Telemetery Readback Test Data 10%	50%	90%
Signal	dec	dec	dec
Vbias 0	155	276	458
Vbias 1	-27	698	1422
RTD1	219	NA	NA
RTD2	248	NA	NA
RTD3	276	NA	NA
RTD4	301	NA	NA
RTD5	326	NA	NA
RTD6	351	NA	NA
Reference 4096	836	NA	NA
eference buffere	836	NA	NA

Stage 10. Video Offset DAC Tests - Table 10.

	DAC Value 410				DAC Value 2048				DAC Value 3686			
ADC	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU
0	0.250	NA	NA	17365	1.250		NA	81374	2.250	NA	500ms	145386
1	0.250	NA	NA	16912	1.250		NA	80986	2.250	NA	500ms	145070
2	0.250	NA	NA	17150	1.250		NA	81160	2.250	NA	500ms	145173
3	0.250	NA	NA	17039	1.250		NA	81038	2.250	NA	500ms	145040
4	0.250	NA	NA	16915	1.250		NA	81011	2.250	NA	500ms	145101
5	0.250	NA	NA	17074	1.250		NA	81059	2.250	NA	500ms	145039
6	0.250	NA	NA	16989	1.250		NA	81070	2.250	NA	500ms	145137
7	0.250	NA	NA	17081	1.250		NA	81150	2.250	NA	500ms	145211
8	0.250	NA	NA	17248	1.250		NA	81237	2.250	NA	500ms	145228
9	0.250	NA	NA	17093	1.250		NA	81155	2.250	NA	500ms	145222
10	0.250	NA	NA	17237	1.250		NA	81175	2.250	NA	500ms	145113
11	0.250	NA	NA	17145	1.250		NA	81152	2.250	NA	500ms	145163

ADC	DC Volts		Data Set		
Channel	Slope	Offset	410	2048	3686
0	1638.000	0.500	0.250	1.250	2.250
1	1638.000	0.500	0.250	1.250	2.250
2	1638.000	0.500	0.250	1.250	2.250
3	1638.000	0.500	0.250	1.250	2.250
4	1638.000	0.500	0.250	1.250	2.250
5	1638.000	0.500	0.250	1.250	2.250
6	1638.000	0.500	0.250	1.250	2.250
7	1638.000	0.500	0.250	1.250	2.250
8	1638.000	0.500	0.250	1.250	2.250
9	1638.000	0.500	0.250	1.250	2.250
10	1638.000	0.500	0.250	1.250	2.250
11	1638.000	0.500	0.250	1.250	2.250

(dac# -offset)/slope=Voltage

ADC	ADU's		Data Set		
Channel	Slope	Offset	410	2048	3686
0	0.026	-34.35	17365	81374	145386
1	0.026	-22.27	16912	80986	145070
2	0.026	-28.84	17150	81160	145173
3	0.026	-26.08	17039	81038	145040
4	0.026	-22.32	16915	81011	145101
5	0.026	-27.13	17074	81059	145039
6	0.026	-22.89	16989	81070	145330
7	0.026	-27.59	17081	81150	145103
8	0.026	-32.35	17248	81237	145118
9	0.026	-26.94	17093	81155	145232
10	0.026	-31.22	17237	81175	145161
11	0.026	-28.86	17145	81152	145146

(dac# -offset)/slope=ADU

Notes and Observations

Checked for oscillations using a Agilent Oscilloscope on AC. OK

Stage 11. CDS Control Functions and Video Channel Performanc

TEST #1: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit is held static. The purpose of this test is to verify the correct operation of the ADC devices and measure the noise of the Offset voltage generators, ADC buffer amplifiers and ADC devices

Noise Test 1

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	81371	8.14E+04	81380	2.32795
CH 1	80979	8.10E+04	80988.4	2.34685
CH 2	81154	8.12E+04	81161.4	2.32909
CH 3	81030	8.10E+04	81038.9	2.3313
CH 4	81004	8.10E+04	81012.3	2.30344
CH 5	81047	8.11E+04	81057.6	2.26299
CH 6	81059	8.11E+04	81067.8	2.37681
CH 7	81138	8.12E+04	81146.7	2.41402
CH 8	81230	8.12E+04	81238.2	2.17323
CH 9	81148	81168	81156.8	2.37548
CH 10	81170	81186	81178.3	2.28751
CH 11	81148	81164	81155.4	2.17934

TEST #2: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the invert/non-invert and the DC Restore switches are held static.

Noise Test 2

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76800	7.68E+04	76809.6	2.74513
CH 1	76922	7.69E+04	76931.9	2.71052
CH 2	76633	7.67E+04	76643.8	2.71476
CH 3	76893	7.69E+04	76902.7	2.7594
CH 4	76341	7.64E+04	76350.6	2.75074
CH 5	76785	7.68E+04	76795.8	2.85236
CH 6	76835	7.69E+04	76846	2.86331
CH 7	77146	7.72E+04	77155.8	2.78082
CH 8	76767	7.68E+04	76777.3	2.71345
CH 9	76886	76908	76896.4	2.75449
CH 10	76704	76723	76713.8	2.75567
CH 11	77033	77052	77042.2	2.70721

TEST #3: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the DC Restore switch is held static.

Noise Test 3

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76796	7.68E+04	76806.4	2.93602
CH 1	76918	7.69E+04	76928.8	2.88412
CH 2	76621	7.66E+04	76636.5	3.0782
CH 3	76889	7.69E+04	76899.7	2.85413
CH 4	76345	7.64E+04	76355	3.07454
CH 5	76776	7.68E+04	76786.7	3.08029
CH 6	76826	7.68E+04	76837.5	2.87943
CH 7	77145	7.72E+04	77156.3	3.00462
CH 8	76765	7.68E+04	76777	2.99736
CH 9	76888	76911	76899.2	2.97965
CH 10	76701	76721	76711.3	2.99363
CH 11	77031	77050	77041.1	2.86854

TEST #4: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition.

Noise Test 4

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76788	7.68E+04	76799	3.07662
CH 1	76922	7.69E+04	76931.8	3.04642
CH 2	76626	7.67E+04	76640.7	3.15923
CH 3	76890	7.69E+04	76900.2	2.94642
CH 4	76379	7.64E+04	76392.2	3.07705
CH 5	76767	7.68E+04	76776.8	3.12256
CH 6	76834	7.69E+04	76845.7	3.22569
CH 7	77105	7.71E+04	77116.5	3.18011
CH 8	76804	7.68E+04	76816	3.01306
CH 9	76811	76834	76822.3	3.07477
CH 10	76719	76742	76729	3.11692
CH 11	76994	77016	77004.8	3.09513

TEST #5: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the circuitry set to high GAIN.

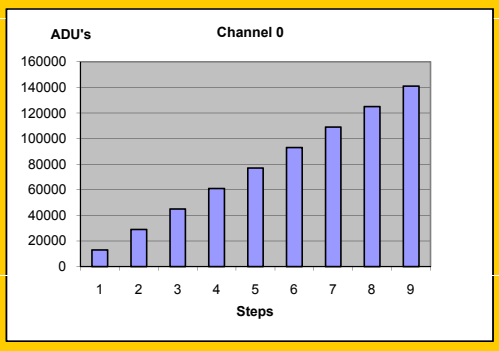
Noise Test 5

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76797	7.68E+04	76809.9	3.7304
CH 1	76932	7.70E+04	76944.2	3.63767
CH 2	76646	7.67E+04	76658.1	3.51257
CH 3	76894	7.69E+04	76905.9	3.63242
CH 4	76383	7.64E+04	76396.3	3.65572
CH 5	76762	7.68E+04	76775.9	3.65217
CH 6	76836	7.69E+04	76849.4	3.68796
CH 7	77106	7.71E+04	77118	3.65145
CH 8	76853	7.69E+04	76866.9	3.56716
CH 9	76809	76835	76822.6	3.55654
CH 10	76778	76804	76791.4	3.66367
CH 11	76988	77017	77004.6	3.62879

TEST #6A: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

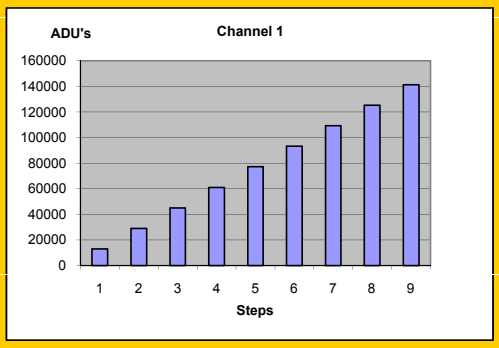
BrdTst6_006 / Channel 0					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13084	13104	13093.6	3.07574	10%
0x333	29067	29092	29078.6	3.10644	20%
0x4cc	45047	45069	45057.4	3.06873	30%
0x666	61070	61092	61081.3	3.13025	40%
0x800	77089	77113	77100.7	3.18498	50%
0x999	93071	93095	93084.1	3.0853	60%
0xb33	109098	109120	109109	3.00698	70%
0xccc	125079	125104	125091	3.22355	80%
0xe66	141104	141129	141116	3.16441	90%



TEST #6B: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

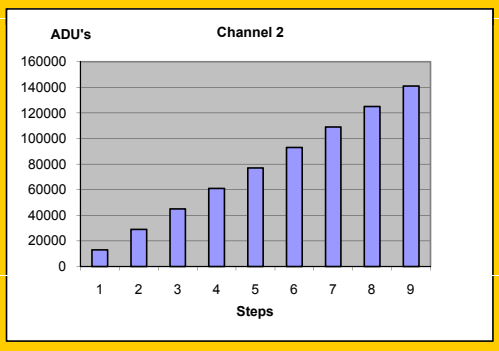
BrdTst6_006 / Channel 1					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13087	13110	13098.7	3.10212	10%
0x333	29089	29109	29099.1	3.15059	20%
0x4cc	45085	45110	45096.2	3.10965	30%
0x666	61124	61146	61134.8	3.16193	40%
0x800	77162	77184	77173.1	3.09348	50%
0x999	93163	93186	93174.5	2.97266	60%
0xb33	109203	109226	109214	3.14729	70%
0xccc	125202	125224	125214	3.14248	80%
0xe66	141244	141265	141254	3.14678	90%



TEST #6C: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

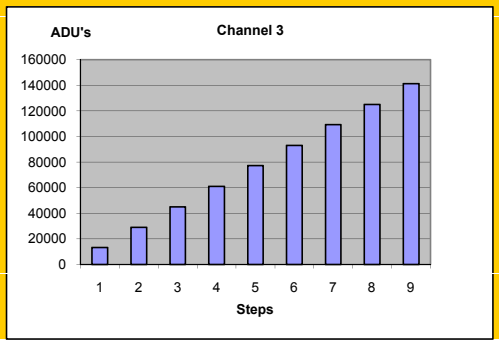
BrdTst6_006 / Channel 2					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12917	12941	12930	3.11455	10%
0x333	28903	28925	28914.4	3.14943	20%
0x4cc	44884	44906	44895	3.14501	30%
0x666	60906	60930	60918.1	3.08336	40%
0x800	76929	76952	76940.3	3.09583	50%
0x999	92914	92936	92924.7	3.15432	60%
0xb33	108938	108959	108948	3.1839	70%
0xccc	124920	124945	124932	3.03318	80%
0xe66	140945	140966	140956	3.18617	90%



TEST #6D: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

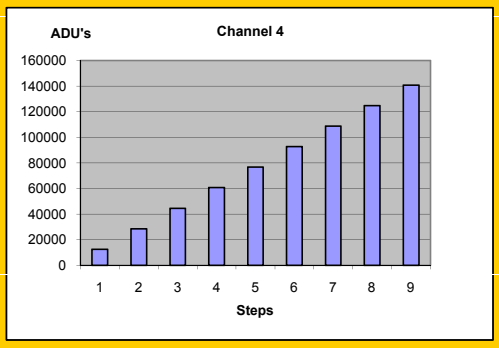
BrdTst6_006 / Channel 3					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13134	13157	13146.4	3.1501	10%
0x333	29113	29135	29124.5	3.08082	20%
0x4cc	45090	45115	45103.9	3.07539	30%
0x666	61112	61134	61123	3.0077	40%
0x800	77132	77153	77141.8	3.17058	50%
0x999	93110	93131	93120.8	3.16751	60%
0xb33	109128	109150	109140	3.03932	70%
0xccc	125109	125134	125120	3.11502	80%
0xe66	141128	141150	141139	3.19966	90%



TEST #6E: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

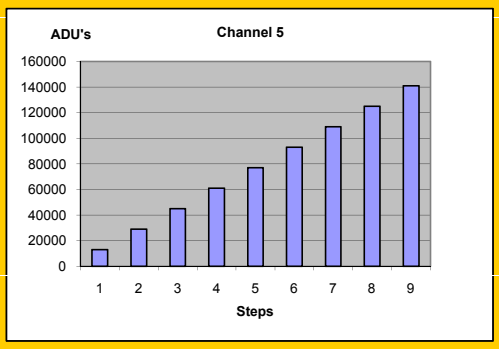
BrdTst6_006 / Channel 4					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12587	12609	12598.3	3.06258	10%
0x333	28590	28612	28601.7	3.12758	20%
0x4cc	44594	44617	44605.9	3.10579	30%
0x666	60636	60658	60647.5	3.08745	40%
0x800	76675	76697	76686.9	3.15157	50%
0x999	92676	92701	92690.3	3.1643	60%
0xb33	108722	108744	108732	3.1434	70%
0xccc	124728	124750	124739	3.15679	80%
0xe66	140772	140794	140783	3.13188	90%



TEST #6F: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

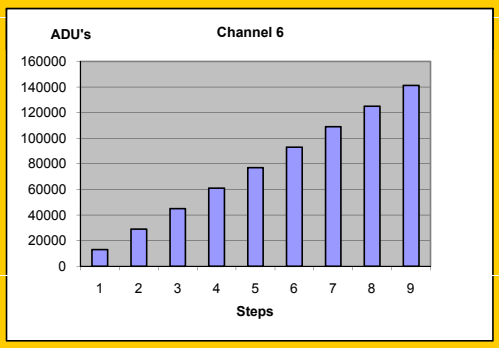
BrdTst6_006 / Channel 5					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13043	13065	13053.7	3.15886	10%
0x333	29017	29040	29028.3	2.98955	20%
0x4cc	44993	45015	45003	3.12851	30%
0x666	61005	61028	61016.8	3.13801	40%
0x800	77017	77042	77030	3.12491	50%
0x999	92993	93015	93003.3	3.11468	60%
0xb33	109004	109028	109018	3.14598	70%
0xccc	124983	125008	124995	3.04387	80%
0xe66	140997	141021	141009	3.19527	90%



TEST #6G: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

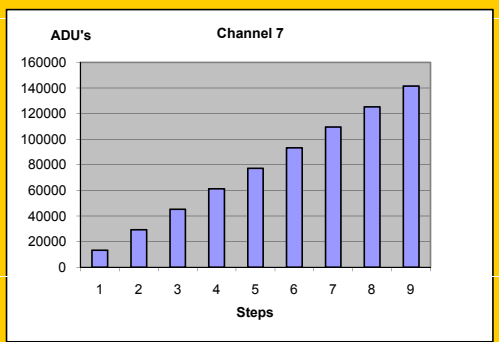
BrdTst6_006 / Channel 6					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13005	13029	13016.8	3.17622	10%
0x333	29001	29027	29014.8	3.15237	20%
0x4cc	44998	45020	45009.2	3.04581	30%
0x666	61035	61059	61046.1	3.21461	40%
0x800	77074	77096	77084.5	3.21782	50%
0x999	93073	93095	93084.1	3.13244	60%
0xb33	109111	109133	109122	3.18337	70%
0xccc	125108	125131	125119	3.1587	80%
0xe66	141146	141167	141157	3.09301	90%



TEST #6H: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

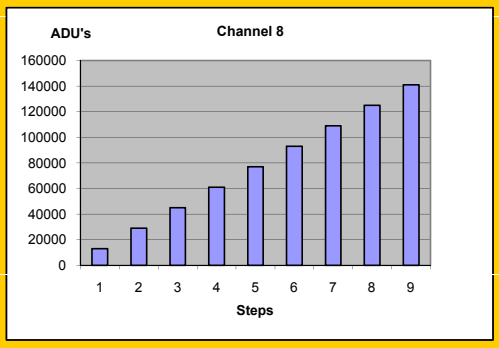
BrdTst6_006 / Channel 7					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13286	13308	13297.3	3.16952	10%
0x333	29284	29306	29295.7	3.17251	20%
0x4cc	45273	45296	45285.6	2.99412	30%
0x666	61311	61335	61324	3.23127	40%
0x800	77347	77370	77357.5	3.16991	50%
0x999	93341	93365	93352.1	3.1528	60%
0xb33	109378	109402	109390	3.12811	70%
0xccc	125371	125394	125383	3.22363	80%
0xe66	141410	141433	141421	3.15061	90%



TEST #6I: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

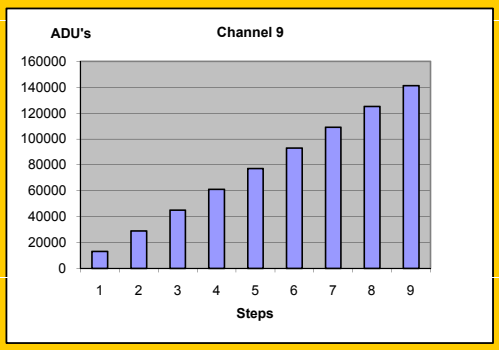
BrdTst6_006 / Channel 8					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13091	13113	13100.6	3.10692	10%
0x333	29064	29088	29076.5	3.18554	20%
0x4cc	45043	45065	45054.7	3.05177	30%
0x666	61059	61083	61069.5	3.10577	40%
0x800	77077	77098	77087.7	3.05051	50%
0x999	93055	93078	93066.6	3.13016	60%
0xb33	109073	109097	109084	3.13348	70%
0xccc	125051	125073	125063	3.02218	80%
0xe66	141069	141090	141080	3.08325	90%



TEST #6J: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

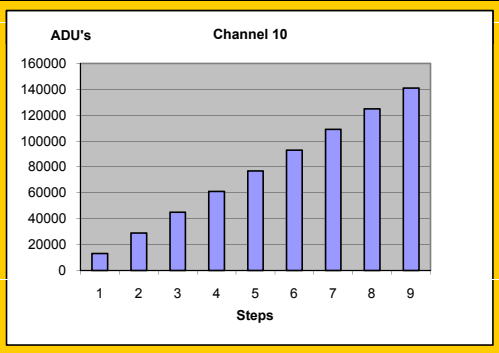
BrdTst6_006 / Channel 9					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13026	13046	13036.1	3.0754	10%
0x333	29021	29044	29032	3.10151	20%
0x4cc	45016	45037	45026.6	3.06335	30%
0x666	61049	61071	61060.9	3.10962	40%
0x800	77087	77108	77097.4	3.08612	50%
0x999	93084	93107	93095	3.13692	60%
0xb33	109118	109141	109129	3.09826	70%
0xccc	125114	125137	125126	3.02675	80%
0xe66	141151	141173	141162	3.14757	90%



TEST #6K: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

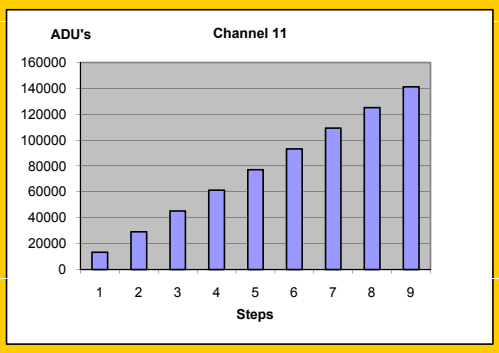
BrdTst6_006 / Channel 10					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13057	13079	13066.7	3.15108	10%
0x333	29018	29040	29029.9	2.98636	20%
0x4cc	44982	45008	44995.2	3.10075	30%
0x666	60986	61008	60997.5	2.96579	40%
0x800	76992	77013	77001.7	3.137	50%
0x999	92956	92981	92969.1	3.04351	60%
0xb33	108960	108985	108973	3.14588	70%
0xccc	124928	124951	124940	3.09141	80%
0xe66	140932	140954	140944	3.23551	90%



TEST #6L: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

BrdTst6_006 / Channel 11					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13253	13276	13265.9	3.16168	10%
0x333	29235	29256	29245.5	3.10906	20%
0x4cc	45218	45243	45229.8	3.07885	30%
0x666	61237	61260	61249.7	3.02196	40%
0x800	77260	77282	77271.2	3.142	50%
0x999	93241	93265	93253.1	3.11471	60%
0xb33	109260	109284	109273	3.1898	70%
0xccc	125249	125272	125260	3.11496	80%
0xe66	141270	141292	141281	3.15651	90%



Stage 13. Other Bit Tests. Table 11

Electronic Serial Number	0xDB8F6C		Board Serial Number	15
Firmware Version	0x193		Name Of Person Testing	S. Holm
Ident Register	0x502		Board passed Functional Tests	YES