DES 12 Channel Board - Functional Tests: CCD Acquisition Board Revision 1.0

Stage 1. Preparation of documentation and configuration settings - Table 1.

Board Part Number	6		Board Serial Number	0xDB8F71
Date Of Tests	July 2010		Name Of Person Testing	S. Holm
Suggested Filename To Save	CCDACQ_12Ch_REPORT_BOARD6.xls		Sequence number: Test	

Stage 3. Power plane short test - Table 2.

Supply Name	Short test to ground: Impedance to ground	Test Point	
+1.2VD	59.70	TP43	~50 ohms
+1.8VD	2.2M	TPB12	> 1K ohm
+2.5VD	19k	TPB11	> 1K ohm
+3.3VD	19k	D13	> 1K ohm
+5VD	6k	D14	> 1K ohm
+5VA	4M	C267	> 1K ohm
-5VA	300K	C270	> 1K ohm
+15VA	500K	C288	> 1K ohm
-15VA	500K	C282	> 1K ohm
-28VA	2.5M	C307	> 1K ohm

Stage 4. Firmware programming tests - Table 3.

JTAG Order	Designator	Device	Load File	Check Sum or User Code
1	U122	XCF08PFS48C PROM	CcdAcqFpgaV41.mcs	0014ef670
2	U114	Spartan3 XC3S2000 FPGA	ccdacqfpgav41.bit	5102801

Stage 5. Power Consumption - Table 4.

Supply Name	Power Supply Consumption: Measured Voltage at test point	Measured Current on power supply	Test Point	
+1.2VD	1.20	N/A	TP43	
+1.8VD	1.80	N/A	TPB12	
+2.5VD	2.50	N/A	TPB11	
+3.3VD	3.30	0.101	D13	
+5VD	5.20	0.152	D14	
+5VA	5.37	0.678	C267	
-5VA	-4.90	0.437	C270	
+15VA	15.04	0.561	C288	
-15VA	-15.07	0.409	C282	
-28VA	-27.78	0.219	C307	
Vref 0+	9.99	N/A	R534	Vsub+ Reference(+10v)
Vref 0-	-2.52	N/A	R525	Vsub - Reference(-2.5v)
Vref Offset	2.50	N/A	R573	ADC Offset Reference(+2.5v)
Vclamp	1.88	N/A	VIA	ADC Clamp Voltage(+1.8v)
ADC Ref.	2.50	N/A	VIA	ADC Reference Voltage(+2.5v)
Vref 1+	2.50	N/A	R537	Vru and Vrl + Reference(+2.5v)
Vref 1-	-10.13	N/A	R535	Vru and Vrl - Reference(-10v)
Vref 2+	5.00	N/A	R563	Vog + Reference(+5v)
Vref 2-	-2.52	N/A	R555	Vog - Reference(-2.5v)
Vref 3+	2.50	N/A	R543	Vdd + Reference(+2.5v)
Vref 3-	-10.10	N/A	R571	Vdd - Reference(-10v)

Power Dissipation:
27.6 Watts

~27 watts +/- 5%

Stage 7. Basic Bus Transactions - **D**igital **Register** Tests - Table 5.

Register name	Put an X on any bit that has an error: 31-24	23-16	15-08	07-00	Function	Test name: Pattern	Walking 0's	Walking 1's
CDS Control			00000000	00000000	16 bit R/W			
Digital Output	00000000	00000000	00000000	00000000	32 bit R/W			
ADC Config.			0000	00000000	12 bit R/W			
Offset DAC			0000	00000000	12 bit R/W			
Bias DAC			0000	00000000	12 bit R/W			
Telemetry Config.				0000	4 bit R/W			
Auxilary Config.				00 00000000	10 bit R/W			
Redirect				0000	4 bit R/W			
Pixel Transfer				00000000	8 bit R/W			
Micro SEQ			00000000	00000000	16 bit R/W			
RAM Buffer			00000000	00000000	16 bit R/W			
LED Control				0000	4 bit R/W			
Control			00000000	00000000	16 bit R/W			
All Register Test	00000000	00000000	00000000	00000000	16 bit R/W	**Passed**	**Passed**	**Passed**

Stage 8. Bias Voltage settings and output enables testing - Table 8

DAC Value	Bias Voltage Test Data 410	2048	3686	50% rms Noise	10-90% Rise Time			
Signal	volts	volts	volts	uV	millisec.	Fanout Brd	Slope	Offset
Vru 0	-13.30	-5.72	1.85	<10	1	BIAS 3	216.24	3285.60
Vru 1	-13.32	-5.73	1.85	<10	1	BIAS 4	215.95	3286.13
Vru 2	-13.32	-5.73	1.85	<10	1	BIAS 5	215.95	3286.13
Vru 3	-13.31	-5.73	1.85	<10	1	BIAS 6	216.09	3286.22
Vru 4	-13.30	-5.73	1.85	<10	1	BIAS 7	216.24	3286.32
Vru 5	-13.31	-5.73	1.85	<10	1	BIAS 8	216.09	3286.22
Vru 6	-13.32	-5.73	1.85	NA	NA	BIAS 9	215.95	3286.13
Vru 7	-13.30	-5.73	1.85	NA	NA	BIAS 10	216.24	3286.32
Vrl 0	-13.32	-5.73	1.85	<10	1	BIAS 11	215.95	3286.13
Vrl 1	-13.29	-5.73	1.85	<10	1	BIAS 12	216.38	3286.42
Vrl 2	-13.31	-5.73	1.85	<10	1	BIAS 13	216.09	3286.22
Vrl 3	-13.33	-5.73	1.85	<10	1	BIAS 14	215.81	3286.03
Vrl 4	-13.32	-5.73	1.85	<10	1	BIAS 15	215.95	3286.13
Vrl 5	-13.34	-5.73	1.85	<10	1	BIAS 16	215.67	3285.93
Vrl 6	-13.32	-5.73	1.85	NA	NA	BIAS 17	215.95	3286.13
Vrl 7	-13.33	-5.73	1.85	NA	NA	BIAS 18	215.81	3286.03
Vog 0	-1.77	1.23	4.24	<10	1	BIAS 19	545.09	1375.72
Vog 1	-1.77	1.24	4.24	<10	1	BIAS 20	545.09	1373.90
Vog 2	-1.77	1.24	4.24	<10	1	BIAS 21	545.09	1373.90
Vog 3	-1.77	1.24	4.24	<10	1	BIAS 22	545.09	1373.90
Vog 4	-1.77	1.24	4.24	<10	1	BIAS 23	545.09	1373.90
Vog 5	-1.77	1.24	4.24	<10	1	BIAS 24	545.09	1373.90
Vog 6	-1.77	1.24	4.24	NA	NA	BIAS 25	545.09	1373.90
Vog 7	-1.77	1.24	4.24	NA	NA	BIAS 26	545.09	1373.90
Vdd 0	-22.08	-9.50	3.09	<10	20	BIAS 27	130.15	3284.04
Vdd 1	-22.17	-9.54	3.10	<10	20	BIAS 28	129.64	3284.33
Vdd 2	-22.14	-9.53	3.09	<10	20	BIAS 29	129.85	3284.99
Vdd 3	-22.13	-9.52	3.09	<10	20	BIAS 30	129.90	3284.62
Vdd 4	-22.14	-9.52	3.10	<10	20	BIAS 21	129.79	3283.64
Vdd 5	-22.08	-9.50	3.10	<10	20	BIAS 32	130.10	3283.11
Vdd 6	-22.14	-9.52	3.10	NA	NA	BIAS 33	129.79	3283.64
Vdd 7	-22.17	-9.54	3.10	NA	NA	BIAS 34	129.64	3284.33

Vru	Slope		Offset
Mean	216.10	Mean	3286.13
Stdev	0.1234457	Stdev	0.215468679
Average	216.09503	Average	3286.134088
	Dac #	Average voltage	
	0	-15.0	
	4095	3.7	

Vrl	Slope		Offset
Mean	215.95	Mean	3286.13
Stdev	0.2015085	Stdev	0.136548623
Average	215.95263	Average	3286.127473
	Dac #	Average voltage	
	0	-15.2	
	4095	3.8	

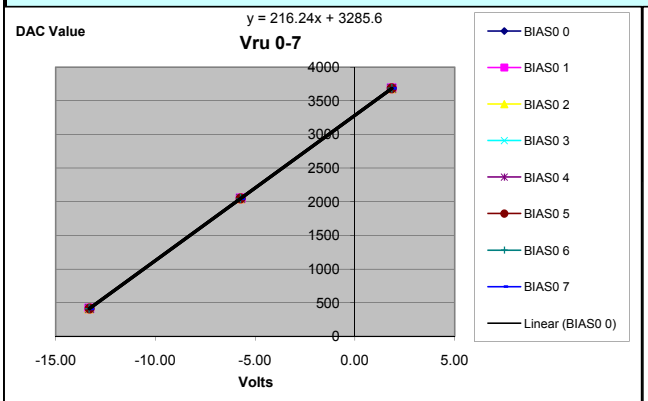
Vog	Slope		Offset
Mean	545.09	Mean	1374.13
Stdev	4.019E-14	Stdev	0.600906357
Average	545.09101	Average	1374.131238
	Dac #	Average voltage	
	0	-2.5	
	4095	5.0	

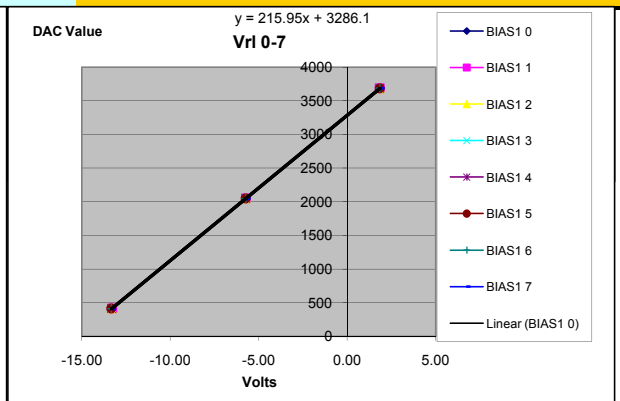
Vdd	Slope		Offset
Mean	129.86	Mean	3284.09
Stdev	0.1779496	Stdev	0.567670995
Average	129.85853	Average	3284.088247
	Dac #	Average voltage	
	0	-25.3	
	4095	6.3	

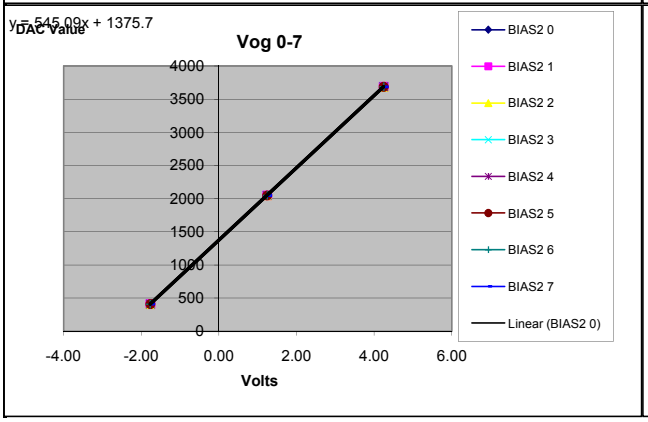
Notes and Observations

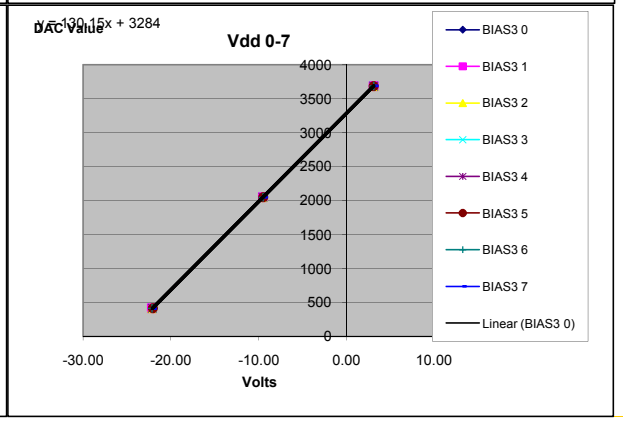
Checked for oscillations using a Agilent Oscilloscpe on AC.**OK**

average min & max voltages
(dac# -offset)/slope=voltage









Stage 8B. Telemetry System Tests - Table 7 (Bias Telemetry Tests)

DAC Value	410	3686	Bias Signals Set Volts		Resolved Values for Telemetry Channel	
	Telemetry Return Values					
Signal	10%	90%	10%	90%	Slope	Offset
Vru 0	-1766	420	-13.30	1.85	144.2904	153.06
Vru 1	-1767	420	-13.32	1.85	144.1661	153.29
Vru 2	-1767	420	-13.32	1.85	144.1661	153.29
Vru 3	-1766	420	-13.31	1.85	144.1953	153.24
Vru 4	-1769	420	-13.30	1.85	144.4884	152.70
Vru 5	-1766	419	-13.31	1.85	144.1293	152.36
Vru 6	-1767	420	-13.32	1.85	144.1661	153.29
Vru 7	-1771	420	-13.30	1.85	144.6205	152.45
Vrl 0	-1766	420	-13.32	1.85	144.1002	153.41
Vrl 1	-1770	420	-13.29	1.85	144.6499	152.40
Vrl 2	-1765	420	-13.31	1.85	144.1293	153.36
Vrl 3	-1769	420	-13.33	1.85	144.2029	153.22
Vrl 4	-1767	420	-13.32	1.85	144.1661	153.29
Vrl 5	-1767	420	-13.34	1.85	143.9763	153.64
Vrl 6	-1770	420	-13.32	1.85	144.3639	152.93
Vrl 7	-1770	420	-13.33	1.85	144.2688	153.10
Vog 0	-366	867	-1.77	4.24	205.1581	-2.87
Vog 1	-366	867	-1.77	4.24	205.1581	-2.87
Vog 2	-366	867	-1.77	4.24	205.1581	-2.87
Vog 3	-366	867	-1.77	4.24	205.1581	-2.87
Vog 4	-366	867	-1.77	4.24	205.1581	-2.87
Vog 5	-366	867	-1.77	4.24	205.1581	-2.87
Vog 6	-365	867	-1.77	4.24	204.9917	-2.16
Vog 7	-365	868	-1.77	4.24	205.1581	-1.87
Vdd 0	-1715	570	-22.08	3.09	90.7827	289.48
Vdd 1	-1725	571	-22.17	3.10	90.8587	289.34
Vdd 2	-1719	572	-22.14	3.09	90.8046	291.41
Vdd 3	-1718	572	-22.13	3.09	90.8010	291.43
Vdd 4	-1724	572	-22.14	3.10	90.9667	290.00
Vdd 5	-1720	572	-22.08	3.10	91.0246	289.82
Vdd 6	-1723	572	-22.14	3.10	90.9271	290.13
Vdd 7	-1722	573	-22.17	3.10	90.8192	291.46

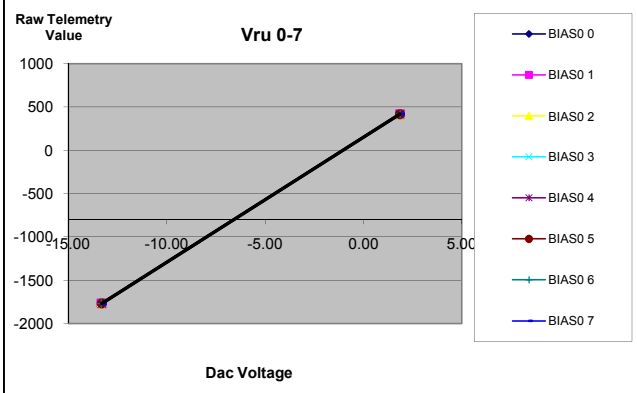
AVERAGE

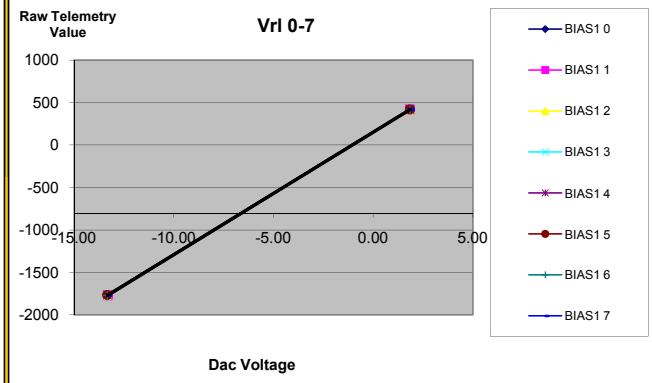
Vru	Slope		Offset
Mean	144.28	Mean	152.96
Stdev	0.1689079	Stdev	0.3719427

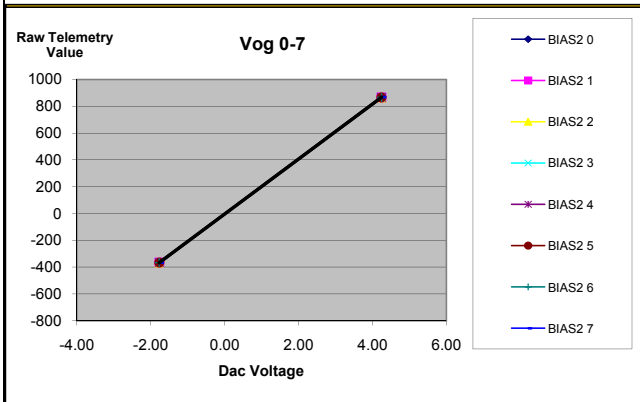
Vrl	Slope		Offset
Mean	144.23	Mean	153.17
Stdev	0.1910182	Stdev	0.3533837

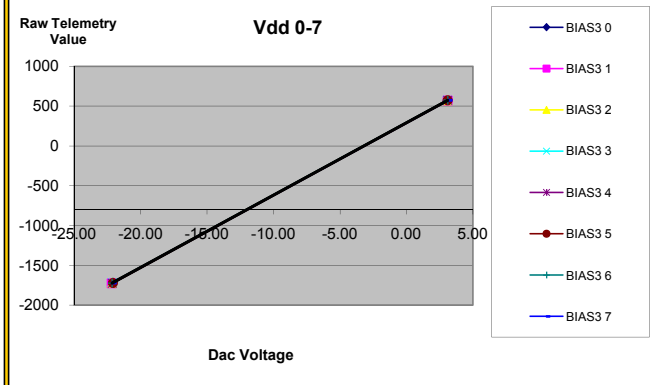
Vog	Slope		Offset
Mean	205.14	Mean	-2.66
Stdev	0.0550281	Stdev	0.3765186

Vdd	Slope		Offset
Mean	90.87	Mean	290.38
Stdev	0.0835395	Stdev	0.8468804









Stage 8C. Bias Voltage output enables testing - Table 8

Place a line through Bias Voltage name if enable/disable switch works

Vru 0	Vru 1	Vru 2	Vru 3	Vru 4	Vru 5
Vrl 0	Vrl 1	Vrl 2	Vrl 3	Vrl 4	Vrl 5
Vog 0	Vog 1	Vog 2	Vog 3	Vog 4	Vog 5
Vdd 0	Vdd 1	Vdd 2	Vdd 3	Vdd 4	Vdd 5

Stage 9. Vsub and Heater Control testing - Table 9

DAC Value	Vsub Measured Voltage Test Data 10%	50%	90%
Signal	volts	volts	volts
Vsub - rate	-1.27	3.73	8.74
Vsub - Limit	-1.27	3.73	8.74
Vsub0	0.00	0.00	0.00
	Vsub Enable Bit - pass		

DAC Value	Telemetery Readback Test Data 10%	50%	90%
Signal	dec	dec	dec
Vbias 0	154	266	444
Vbias 1	-29	691	1412
RTD1	220	NA	NA
RTD2	248	NA	NA
RTD3	274	NA	NA
RTD4	302	NA	NA
RTD5	327	NA	NA
RTD6	350	NA	NA
Reference 4096	837	NA	NA
eference buffere	837	NA	NA

Stage 10. Video Offset DAC Tests - Table 10.

	DAC Value 410				DAC Value 2048				DAC Value 3686			
ADC	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU
0	0.250	NA	NA	16859	1.250		NA	81013	2.250	NA	500ms	145164
1	0.250	NA	NA	16836	1.250		NA	80950	2.250	NA	500ms	145050
2	0.250	NA	NA	16972	1.250		NA	81065	2.250	NA	500ms	145148
3	0.250	NA	NA	17329	1.250		NA	81253	2.250	NA	500ms	145177
4	0.250	NA	NA	17013	1.250		NA	80986	2.250	NA	500ms	144953
5	0.250	NA	NA	17093	1.250		NA	81098	2.250	NA	500ms	145096
6	0.250	NA	NA	17008	1.250		NA	81085	2.250	NA	500ms	145155
7	0.250	NA	NA	17278	1.250		NA	81256	2.250	NA	500ms	145239
8	0.250	NA	NA	17140	1.250		NA	81220	2.250	NA	500ms	145296
9	0.250	NA	NA	17213	1.250		NA	81180	2.250	NA	500ms	145141
10	0.250	NA	NA	17143	1.250		NA	81155	2.250	NA	500ms	145160
11	0.250	NA	NA	17275	1.250		NA	81234	2.250	NA	500ms	145174

ADC	DC Volts		Data Set		
Channel	Slope	Offset	410	2048	3686
0	1638.000	0.500	0.250	1.250	2.250
1	1638.000	0.500	0.250	1.250	2.250
2	1638.000	0.500	0.250	1.250	2.250
3	1638.000	0.500	0.250	1.250	2.250
4	1638.000	0.500	0.250	1.250	2.250
5	1638.000	0.500	0.250	1.250	2.250
6	1638.000	0.500	0.250	1.250	2.250
7	1638.000	0.500	0.250	1.250	2.250
8	1638.000	0.500	0.250	1.250	2.250
9	1638.000	0.500	0.250	1.250	2.250
10	1638.000	0.500	0.250	1.250	2.250
11	1638.000	0.500	0.250	1.250	2.250

(dac# -offset)/slope=Voltage

ADC	ADU's		Data Set		
Channel	Slope	Offset	410	2048	3686
0	0.026	-20.47	16859	81013	145164
1	0.026	-20.24	16836	80950	145050
2	0.026	-23.82	16972	81065	145148
3	0.026	-34.04	17329	81253	145177
4	0.026	-25.66	17013	80986	144953
5	0.026	-27.49	17093	81098	145096
6	0.026	-24.83	17008	81085	145155
7	0.026	-32.32	17278	81256	145239
8	0.026	-28.16	17140	81220	145296
9	0.026	-30.82	17213	81180	145141
10	0.026	-28.73	17143	81155	145160
11	0.026	-32.56	17275	81234	145174

(dac# -offset)/slope=ADU

Notes and Observations

Checked for oscillations using a Agilent Oscilloscope on AC. OK

Stage 11. CDS Control Functions and Video Channel Performanc

TEST #1: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit is held static. The purpose of this test is to verify the correct operation of the ADC devices and measure the noise of the Offset voltage generators, ADC buffer amplifiers and ADC devices

Noise Test 1

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	81006	81021	81013.5	2.1403
CH 1	80939	80956	80947.3	2.40303
CH 2	81054	81069	81060.8	2.23015
CH 3	81246	81262	81254	2.32655
CH 4	80978	80995	80985.8	2.31566
CH 5	81088	81105	81096.6	2.39592
CH 6	81076	81093	81085	2.37471
CH 7	81250	81267	81258.4	2.42924
CH 8	81213	81230	81220.8	2.18752
CH 9	81171	81188	81180.8	2.46213
CH 10	81145	81164	81153.5	2.28618
CH 11	81220	81239	81228.8	2.45872

TEST #2: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the invert/non-invert and the DC Restore switches are held static.

Noise Test 2

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76148	76168	76158.9	2.76438
CH 1	76725	76747	76736.5	2.73248
CH 2	76421	76441	76430.7	2.87571
CH 3	77370	77389	77379.2	2.71121
CH 4	76184	76205	76195	2.90852
CH 5	76832	76853	76842.2	2.96601
CH 6	76698	76721	76709.1	2.82686
CH 7	77078	77097	77086.8	2.92136
CH 8	76785	76804	76794.6	2.89239
CH 9	77197	77219	77207.8	2.95654
CH 10	76561	76582	76571.7	2.98101
CH 11	76857	76880	76868.6	2.95184

TEST #3: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the DC Restore switch is held static.

Noise Test 3

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76082	76103	76092	3.05407
CH 1	76685	76705	76694.6	2.98926
CH 2	76366	76388	76376.3	3.09348
CH 3	77353	77376	77364.1	2.98703
CH 4	76119	76142	76131.5	2.9911
CH 5	76783	76807	76795.9	3.11911
CH 6	76670	76693	76681.3	3.08364
CH 7	77042	77062	77051.5	3.16262
CH 8	76738	76761	76750.6	3.04783
CH 9	77166	77189	77177.3	3.19224
CH 10	76510	76535	76522	3.23361
CH 11	76833	76854	76842.9	3.18162

TEST #4: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition.

Noise Test 4

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76062	76084	76073.7	3.2353
CH 1	76680	76701	76691.1	3.0562
CH 2	76363	76386	76373.9	3.17502
CH 3	77351	77373	77362.2	3.1685
CH 4	76150	76174	76162.5	3.29519
CH 5	76760	76784	76773	3.22949
CH 6	76673	76698	76685.5	3.25163
CH 7	77001	77024	77012	3.12317
CH 8	76780	76804	76792.1	3.20519
CH 9	77074	77098	77086	3.34537
CH 10	76520	76544	76532.6	3.34953
CH 11	76779	76803	76791.2	3.34594

TEST #5: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the circuitry set to high GAIN.

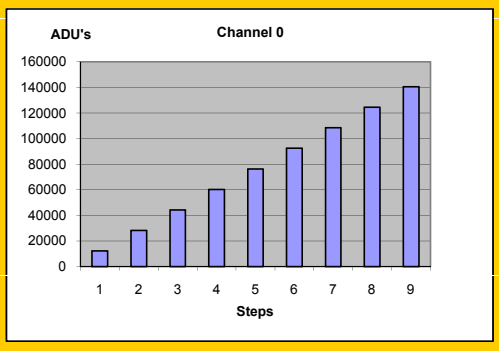
Noise Test 5

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76070	76097	76083.5	3.51411
CH 1	76692	76721	76706.7	3.70378
CH 2	76379	76406	76392.1	3.77062
CH 3	77353	77381	77367.8	3.68468
CH 4	76156	76184	76169.7	3.74153
CH 5	76760	76787	76773.6	3.67735
CH 6	76675	76703	76689.6	3.74976
CH 7	77005	77031	77017.5	3.73954
CH 8	76841	76868	76853.2	3.61708
CH 9	77072	77102	77087.6	3.95827
CH 10	76589	76617	76603.6	3.7569
CH 11	76780	76804	76792.2	3.7522

TEST #6A: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

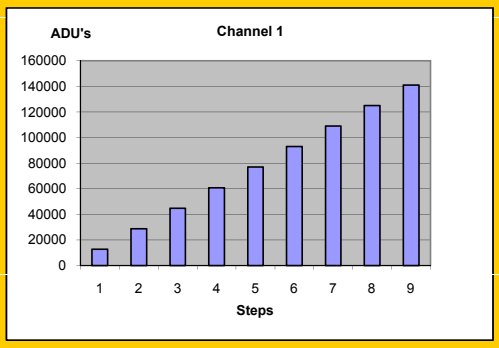
BrdTst6_006 / Channel 0					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12219	12244	12230.7	3.06023	10%
0x333	28228	28254	28242.9	3.28065	20%
0x4cc	44243	44276	44261.1	5.02293	30%
0x666	60299	60321	60309.3	3.09512	40%
0x800	76339	76362	76351.4	3.14047	50%
0x999	92380	92405	92392.8	3.11529	60%
0xb33	108414	108437	108425	3.0345	70%
0xccc	124422	124444	124433	3.13354	80%
0xe66	140486	140507	140496	3.09294	90%



TEST #6B: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

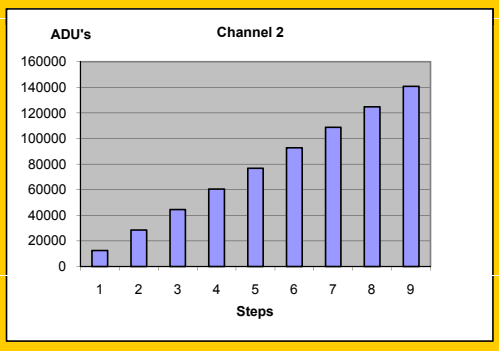
BrdTst6_006 / Channel 1					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12827	12848	12837.1	3.11674	10%
0x333	28826	28849	28837.1	3.22169	20%
0x4cc	44831	44858	44844.4	4.0524	30%
0x666	60869	60894	60882.4	3.12699	40%
0x800	76903	76925	76914.4	3.08334	50%
0x999	92925	92948	92936.9	3.13215	60%
0xb33	108951	108973	108963	3.19431	70%
0xccc	124947	124975	124963	3.08686	80%
0xe66	141000	141021	141011	2.99053	90%



TEST #6C: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

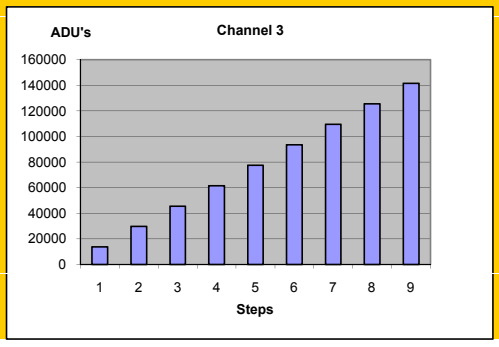
BrdTst6_006 / Channel 2					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12572	12596	12583.4	3.25606	10%
0x333	28567	28590	28578.6	3.35571	20%
0x4cc	44566	44595	44581.9	4.29293	30%
0x666	60605	60627	60615.8	3.1385	40%
0x800	76633	76658	76644.5	3.18623	50%
0x999	92657	92678	92668.1	3.15768	60%
0xb33	108678	108698	108689	3.1463	70%
0xccc	124669	124694	124683	3.23885	80%
0xe66	140717	140741	140730	3.26424	90%



TEST #6D: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

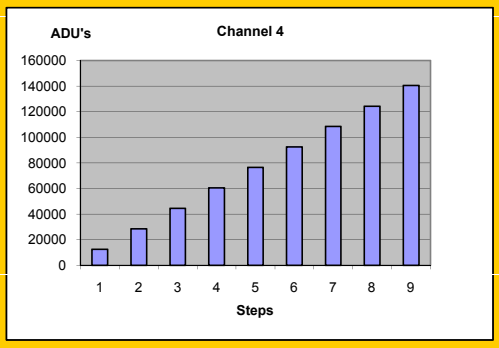
BrdTst6_006 / Channel 3					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13664	13691	13677.9	3.15416	10%
0x333	29626	29650	29637.3	3.07718	20%
0x4cc	45588	45613	45599.6	3.49031	30%
0x666	61585	61606	61595	3.15991	40%
0x800	77573	77597	77585.9	3.1367	50%
0x999	93542	93568	93555.6	3.15197	60%
0xb33	109536	109557	109547	3.18835	70%
0xccc	125493	125519	125506	3.14968	80%
0xe66	141495	141520	141508	3.07515	90%



TEST #6E: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

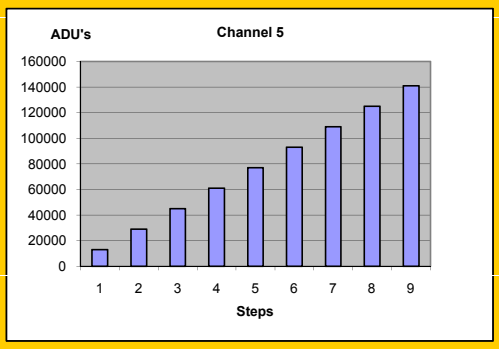
BrdTst6_006 / Channel 4					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12478	12505	12490.8	3.21959	10%
0x333	28445	28470	28457.2	3.24484	20%
0x4cc	44414	44444	44430.6	4.45111	30%
0x666	60425	60445	60434.6	3.01663	40%
0x800	76417	76442	76429.6	3.18353	50%
0x999	92413	92437	92424.6	3.2062	60%
0xb33	108402	108424	108413	3.17243	70%
0xccc	124368	124389	124378	3.16956	80%
0xe66	140383	140408	140396	3.23639	90%



TEST #6F: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

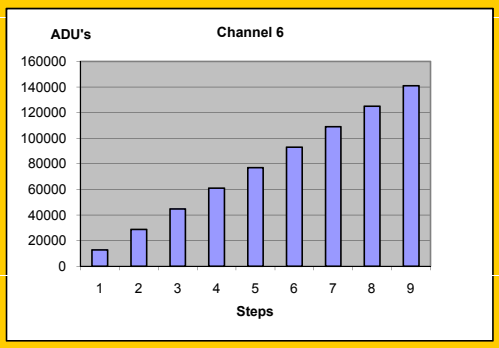
BrdTst6_006 / Channel 5					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13027	13055	13038.2	3.28537	10%
0x333	29000	29024	29012.9	3.22384	20%
0x4cc	44975	45005	44991	4.37962	30%
0x666	60988	61012	61000.9	3.29468	40%
0x800	76992	77017	77004.1	3.32934	50%
0x999	92991	93015	93003.8	3.20894	60%
0xb33	108989	109011	109001	3.23973	70%
0xccc	124958	124980	124969	3.17665	80%
0xe66	140980	141008	140993	3.26688	90%



TEST #6G: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

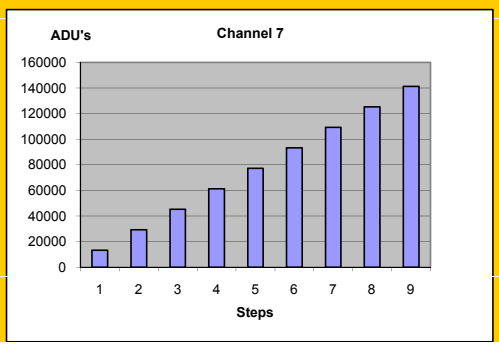
BrdTst6_006 / Channel 6					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12857	12882	12867.1	3.23547	10%
0x333	28853	28876	28864.9	3.22007	20%
0x4cc	44848	44873	44860.2	3.39838	30%
0x666	60885	60909	60895.1	3.17991	40%
0x800	76912	76935	76924.2	3.18744	50%
0x999	92921	92943	92932.6	2.99644	60%
0xb33	108950	108974	108962	3.15126	70%
0xccc	124946	124968	124956	3.24901	80%
0xe66	140985	141008	140996	3.22453	90%



TEST #6H: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

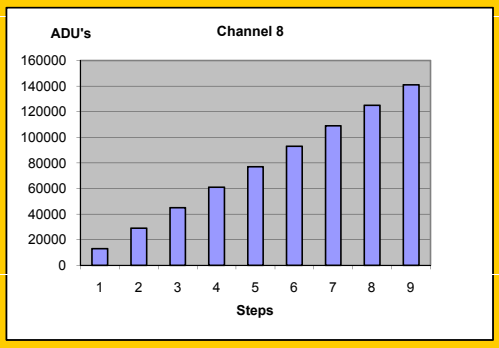
BrdTst6_006 / Channel 7					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13265	13287	13276.1	3.28703	10%
0x333	29235	29257	29246.4	3.23849	20%
0x4cc	45208	45237	45222.8	3.64505	30%
0x666	61221	61243	61232.1	3.19432	40%
0x800	77222	77246	77234.3	3.12075	50%
0x999	93209	93231	93219.8	2.94718	60%
0xb33	109211	109237	109223	3.23634	70%
0xccc	125183	125206	125197	3.25867	80%
0xe66	141200	141224	141213	3.31729	90%



TEST #6I: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

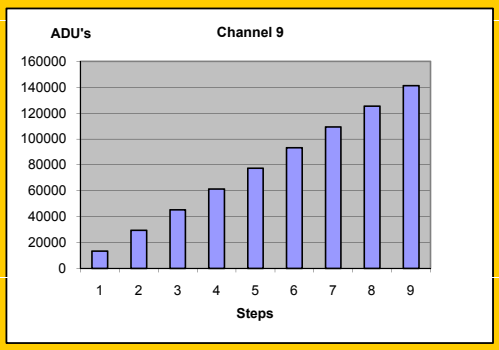
BrdTst6_006 / Channel 8					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12980	13003	12991.8	3.28402	10%
0x333	28974	28996	28985.8	3.21403	20%
0x4cc	44974	44999	44987.7	3.62372	30%
0x666	61007	61028	61017.8	3.17325	40%
0x800	77035	77059	77047.3	3.19488	50%
0x999	93051	93076	93064	3.24039	60%
0xb33	109075	109097	109085	3.13483	70%
0xccc	125070	125096	125082	3.22519	80%
0xe66	141111	141136	141123	3.23922	90%



TEST #6J: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

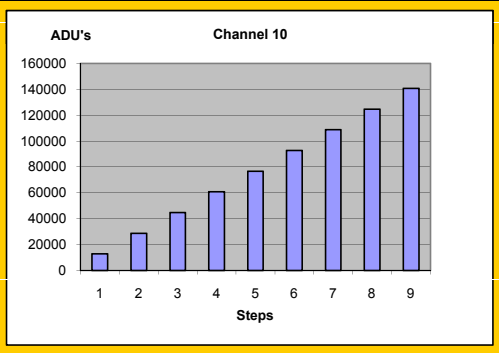
BrdTst6_006 / Channel 9					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13395	13420	13407.5	3.38392	10%
0x333	29361	29386	29373.9	3.29829	20%
0x4cc	45328	45357	45343.7	4.08522	30%
0x666	61337	61360	61348.8	3.27863	40%
0x800	77338	77361	77349.5	3.30821	50%
0x999	93321	93345	93334.2	3.25332	60%
0xb33	109318	109344	109330	3.32825	70%
0xccc	125286	125312	125299	3.22141	80%
0xe66	141299	141324	141310	3.35117	90%



TEST #6K: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

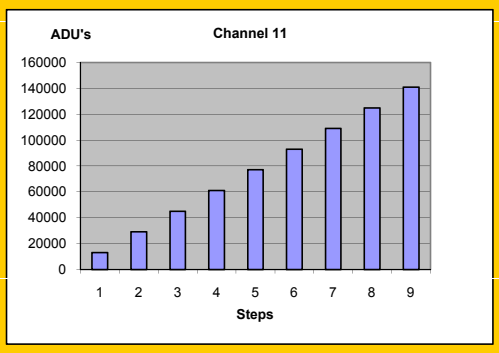
BrdTst6_006 / Channel 10					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12792	12815	12803.8	3.19976	10%
0x333	28768	28792	28779.3	3.33045	20%
0x4cc	44752	44780	44766.6	4.56595	30%
0x666	60768	60792	60779.6	3.29181	40%
0x800	76773	76798	76785.7	3.12554	50%
0x999	92776	92799	92788.1	3.29048	60%
0xb33	108776	108799	108788	3.26245	70%
0xccc	124756	124780	124768	3.22687	80%
0xe66	140782	140804	140793	3.2815	90%



TEST #6L: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

BrdTst6_006 / Channel 11					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13107	13131	13120.2	3.18577	10%
0x333	29074	29097	29084.3	3.27328	20%
0x4cc	45036	45064	45050.4	4.12865	30%
0x666	61043	61064	61053.3	3.26487	40%
0x800	77039	77063	77051.8	3.26732	50%
0x999	93017	93040	93028.8	3.19958	60%
0xb33	109011	109034	109023	3.21336	70%
0xccc	124974	125000	124986	3.22363	80%
0xe66	140983	141009	140996	3.37484	90%



Stage 13. Other Bit Tests. Table 11

Electronic Serial Number	0xDB8F71		Board Serial Number	6
Firmware Version	0x193		Name Of Person Testing	S. Holm
Ident Register	0x502		Board passed Functional Tests	YES