DES 12 Channel Board - Functional Tests: CCD Acquisition Board Revision 1.0

Stage 1. Preparation of documentation and configuration settings - Table 1.

Board Part Number	7		Board Serial Number	0xDB8F8A
Date Of Tests	August 2010		Name Of Person Testing	S. Holm
Suggested Filename To Save	CCDACQ_12Ch_REPORT_BOARD12.xl		Sequence number: Test	

Stage 3. Power plane short test - Table 2.

Supply Name	Short test to ground: Impedance to ground	Test Point	
+1.2VD	69.00	TP43	~50 ohms
+1.8VD	2M	TPB12	> 1K ohm
+2.5VD	17K	TPB11	> 1K ohm
+3.3VD	5K	D13	> 1K ohm
+5VD	500K	D14	> 1K ohm
+5VA	4M	C267	> 1K ohm
-5VA	300K	C270	> 1K ohm
+15VA	500K	C288	> 1K ohm
-15VA	500K	C282	> 1K ohm
-28VA	2.7M	C307	> 1K ohm

Stage 4. Firmware programming tests - Table 3.

JTAG Order	Designator	Device	Load File	Check Sum or User Code
1	U122	XCF08PFS48C PROM	CcdAcqFpgaV41.mcs	0014ef670
2	U114	Spartan3 XC3S2000 FPGA	ccdacqfpgav41.bit	5102801

Stage 5. Power Consumption - Table 4.

Supply Name	Power Supply Consumption: Measured Voltage at test point	Measured Current on power supply	Test Point	
+1.2VD	1.20	N/A	TP43	
+1.8VD	1.80	N/A	TPB12	
+2.5VD	2.50	N/A	TPB11	
+3.3VD	3.30	0.23	D13	
+5VD	5.20	0.15	D14	
+5VA	4.85	0.58	C267	
-5VA	-5.01	0.43	C270	
+15VA	14.97	0.56	C288	
-15VA	-14.96	0.41	C282	
-28VA	-27.89	0.199	C307	
Vref 0+	9.96	N/A	R534	Vsub+ Reference(+10v)
Vref 0-	-2.49	N/A	R525	Vsub - Reference(-2.5v)
Vref Offset	2.50	N/A	R573	ADC Offset Reference(+2.5v)
Vclamp	1.87	N/A	VIA	ADC Clamp Voltage(+1.8v)
ADC Ref.	2.50	N/A	VIA	ADC Reference Voltage(+2.5v)
Vref 1+	2.50	N/A	R537	Vru and Vrl + Reference(+2.5v)
Vref 1-	-10.01	N/A	R535	Vru and Vrl - Reference(-10v)
Vref 2+	5.01	N/A	R563	Vog + Reference(+5v)
Vref 2-	-2.49	N/A	R555	Vog - Reference(-2.5v)
Vref 3+	2.50	N/A	R543	Vdd + Reference(+2.5v)
Vref 3-	-10.00	N/A	R571	Vdd - Reference(-10v)

Power Dissipation:
26.6 Watts

~27 watts +/- 5%

Stage 7. Basic Bus Transactions - **D**igital **Register** Tests - Table 5.

Register name	Put an X on any bit that has an error: 31-24	23-16	15-08	07-00	Function	Test name: Pattern	Walking 0's	Walking 1's
CDS Control			00000000	00000000	16 bit R/W			
Digital Output	00000000	00000000	00000000	00000000	32 bit R/W			
ADC Config.			0000	00000000	12 bit R/W			
Offset DAC			0000	00000000	12 bit R/W			
Bias DAC			0000	00000000	12 bit R/W			
Telemetry Config.				0000	4 bit R/W			
Auxilary Config.			00	00000000	10 bit R/W			
Redirect				0000	4 bit R/W			
Pixel Transfer				00000000	8 bit R/W			
Micro SEQ			00000000	00000000	16 bit R/W			
RAM Buffer			00000000	00000000	16 bit R/W			
LED Control				0000	4 bit R/W			
Control			00000000	00000000	16 bit R/W			
All Register Test	00000000	00000000	00000000	00000000	16 bit R/W	**Passed**	**Passed**	**Passed**

Stage 8. Bias Voltage settings and output enables testing - Table 8

DAC Value	Bias Voltage Test Data 410	2048	3686	50% rms Noise	10-90% Rise Time	Fanout Brd	Slope	Offset
Signal	volts	volts	volts	uV	millisec.			
Vru 0	-13.15	-5.64	1.87	<10	1	BIAS 3	218.11	3278.14
Vru 1	-13.16	-5.64	1.87	<10	1	BIAS 4	217.96	3278.04
Vru 2	-13.15	-5.64	1.87	<10	1	BIAS 5	218.11	3278.14
Vru 3	-13.14	-5.64	1.87	<10	1	BIAS 6	218.25	3278.23
Vru 4	-13.13	-5.64	1.87	<10	1	BIAS 7	218.40	3278.32
Vru 5	-13.14	-5.64	1.87	<10	1	BIAS 8	218.25	3278.23
Vru 6	-13.14	-5.64	1.87	NA	NA	BIAS 9	218.25	3278.23
Vru 7	-13.14	-5.64	1.87	NA	NA	BIAS 10	218.25	3278.23
Vrl 0	-13.15	-5.64	1.87	<10	1	BIAS 11	218.11	3278.14
Vrl 1	-13.16	-5.64	1.87	<10	1	BIAS 12	217.96	3278.04
Vrl 2	-13.13	-5.64	1.87	<10	1	BIAS 13	218.40	3278.32
Vrl 3	-13.16	-5.64	1.87	<10	1	BIAS 14	217.96	3278.04
Vrl 4	-13.15	-5.64	1.87	<10	1	BIAS 15	218.11	3278.14
Vrl 5	-13.11	-5.64	1.87	<10	1	BIAS 16	218.65	3278.47
Vrl 6	-13.15	-5.64	1.87	NA	NA	BIAS 17	218.11	3278.14
Vrl 7	-13.15	-5.64	1.87	NA	NA	BIAS 18	218.11	3278.14
Vog 0	-1.74	1.26	4.26	<10	1	BIAS 19	546.00	1360.04
Vog 1	-1.74	1.26	4.26	<10	1	BIAS 20	546.00	1360.04
Vog 2	-1.74	1.26	4.26	<10	1	BIAS 21	546.00	1360.04
Vog 3	-1.74	1.26	4.26	<10	1	BIAS 22	546.00	1360.04
Vog 4	-1.74	1.26	4.26	<10	1	BIAS 23	546.00	1360.04
Vog 5	-1.74	1.26	4.26	<10	1	BIAS 24	546.00	1360.04
Vog 6	-1.74	1.26	4.26	NA	NA	BIAS 25	546.00	1360.04
Vog 7	-1.74	1.26	4.26	NA	NA	BIAS 26	546.00	1360.04
Vdd 0	-21.86	-9.37	3.11	<10	20	BIAS 27	131.20	3277.76
Vdd 1	-21.97	-9.42	3.13	<10	20	BIAS 28	130.52	3277.48
Vdd 2	-21.84	-9.37	3.11	<10	20	BIAS 29	131.30	3277.87
Vdd 3	-21.90	-9.39	3.12	<10	20	BIAS 30	130.94	3277.48
Vdd 4	-21.93	-9.40	3.13	<10	20	BIAS 21	130.73	3276.83
Vdd 5	-21.92	-9.40	3.12	<10	20	BIAS 32	130.83	3277.81
Vdd 6	-21.85	-9.37	3.12	NA	NA	BIAS 33	131.20	3276.88
Vdd 7	-21.80	-9.35	3.10	NA	NA	BIAS 34	131.57	3278.14

Vru	Slope		Offset
Mean	218.20	Mean	3278.19
Stdev	0.1244914	Stdev	0.078717668
Average	218.20002	Average	3278.193163
	Dac #	Average voltage	
	0	-15.0	
	4095	3.7	

Vrl	Slope		Offset
Mean	218.18	Mean	3278.18
Stdev	0.2179457	Stdev	0.137389582
Average	218.17651	Average	3278.178056
	Dac #	Average voltage	
	0	-15.0	
	4095	3.7	

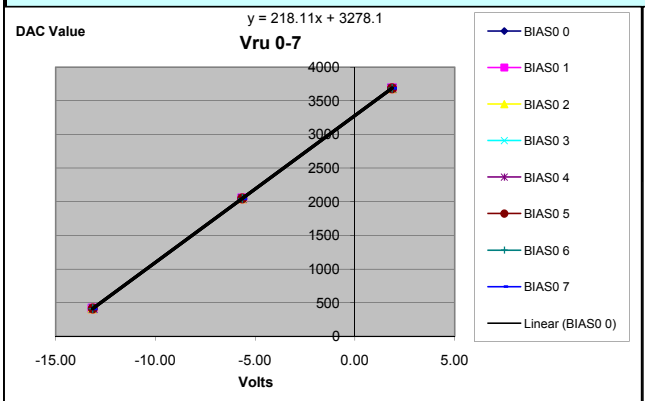
Vog	Slope		Offset
Mean	546.00	Mean	1360.04
Stdev	0	Stdev	0
Average	546	Average	1360.04
	Dac #	Average voltage	
	0	-2.5	
	4095	5.0	

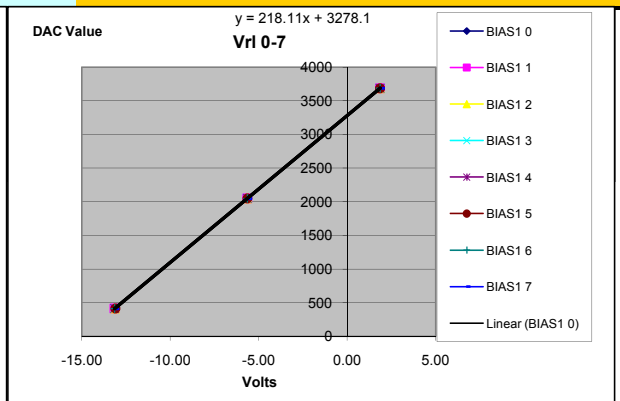
Vdd	Slope		Offset
Mean	131.03	Mean	3277.53
Stdev	0.3203512	Stdev	0.43865304
Average	131.03423	Average	3277.531013
	Dac #	Average voltage	
	0	-25.0	
	4095	6.2	

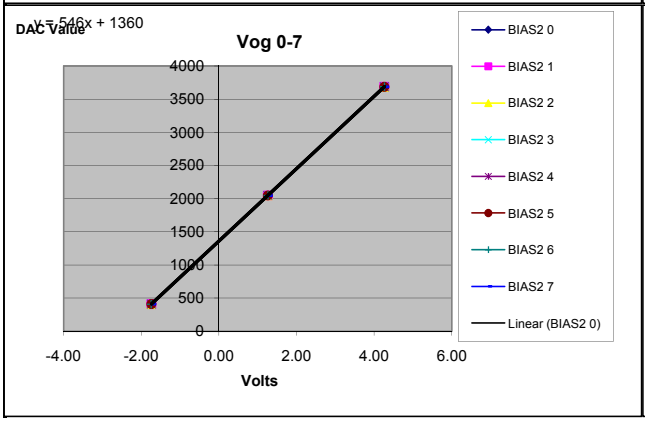
Notes and Observations

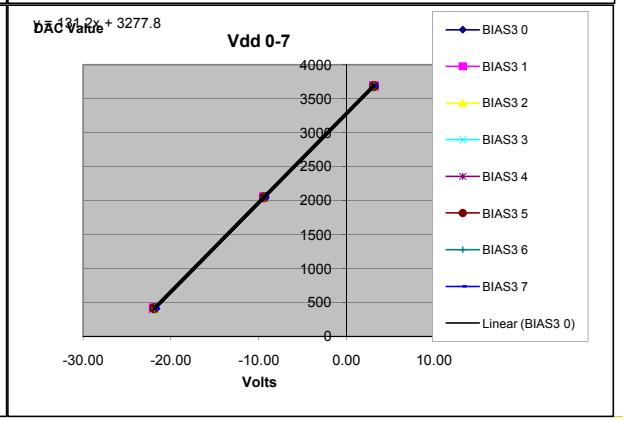
Checked for oscillations using a Agilent Oscilloscpe on AC.**OK**

average min & max voltages
(dac# -offset)/slope=voltage









Stage 8B. Telemetry System Tests - Table 7 (Bias Telemetry Tests)

DAC Value: 410 / 3686

Signal	Telemetry Return Values 10%	90%	Bias Signals Set Volts 10%	90%	Resolved Values for Telemetry Channel Slope	Offset
Vru 0	-1753	423	-13.15	1.87	144.8735	152.09
Vru 1	-1755	423	-13.16	1.87	144.9102	152.02
Vru 2	-1750	423	-13.15	1.87	144.6738	152.46
Vru 3	-1754	422	-13.14	1.87	144.9700	150.91
Vru 4	-1752	423	-13.13	1.87	145.0000	151.85
Vru 5	-1753	423	-13.14	1.87	144.9700	151.91
Vru 6	-1758	422	-13.14	1.87	145.2365	150.41
Vru 7	-1753	423	-13.14	1.87	144.9700	151.91
Vrl 0	-1746	423	-13.15	1.87	144.4075	152.96
Vrl 1	-1748	423	-13.16	1.87	144.4444	152.89
Vrl 2	-1744	423	-13.13	1.87	144.4667	152.85
Vrl 3	-1745	423	-13.16	1.87	144.2448	153.26
Vrl 4	-1745	423	-13.15	1.87	144.3409	153.08
Vrl 5	-1744	423	-13.11	1.87	144.6306	152.54
Vrl 6	-1746	423	-13.15	1.87	144.4075	152.96
Vrl 7	-1747	423	-13.15	1.87	144.4740	152.83
Vog 0	-360	869	-1.74	4.26	204.8333	-3.59
Vog 1	-360	868	-1.74	4.26	204.6667	-3.88
Vog 2	-360	869	-1.74	4.26	204.8333	-3.59
Vog 3	-360	869	-1.74	4.26	204.8333	-3.59
Vog 4	-360	869	-1.74	4.26	204.8333	-3.59
Vog 5	-361	869	-1.74	4.26	205.0000	-4.30
Vog 6	-360	869	-1.74	4.26	204.8333	-3.59
Vog 7	-360	869	-1.74	4.26	204.8333	-3.59
Vdd 0	-1729	574	-21.86	3.11	92.2307	287.16
Vdd 1	-1745	575	-21.97	3.13	92.4303	285.69
Vdd 2	-1728	574	-21.84	3.11	92.2645	287.06
Vdd 3	-1741	575	-21.90	3.12	92.5659	286.19
Vdd 4	-1737	575	-21.93	3.13	92.2586	286.23
Vdd 5	-1737	575	-21.92	3.12	92.3323	286.92
Vdd 6	-1737	574	-21.85	3.12	92.5511	285.24
Vdd 7	-1731	574	-21.80	3.10	92.5703	287.03

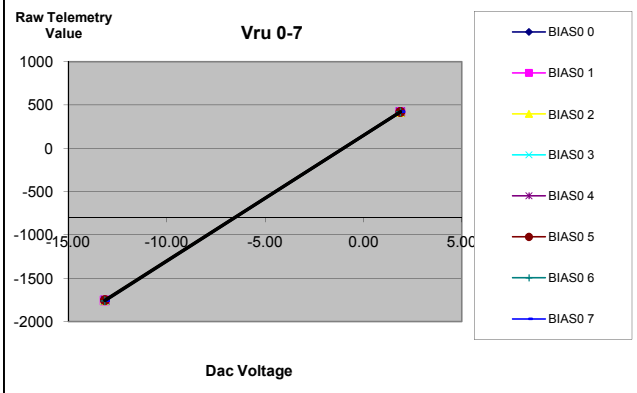
AVERAGE

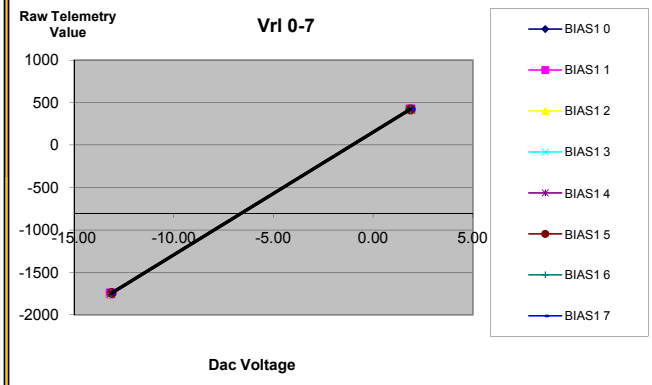
Vru	Slope		Offset
Mean	144.95	Mean	151.69
Stdev	0.1455719	Stdev	0.6359528

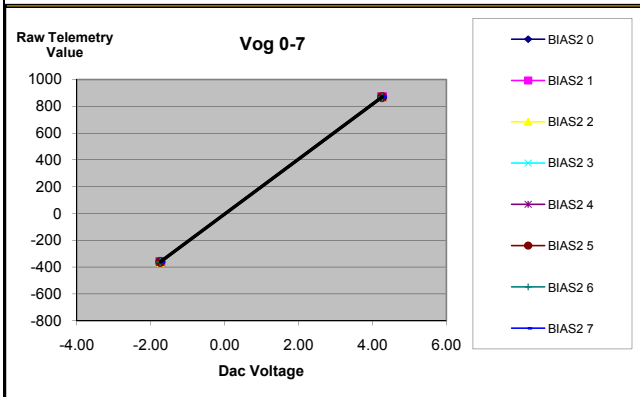
Vrl	Slope		Offset
Mean	144.43	Mean	152.92
Stdev	0.1042215	Stdev	0.1948943

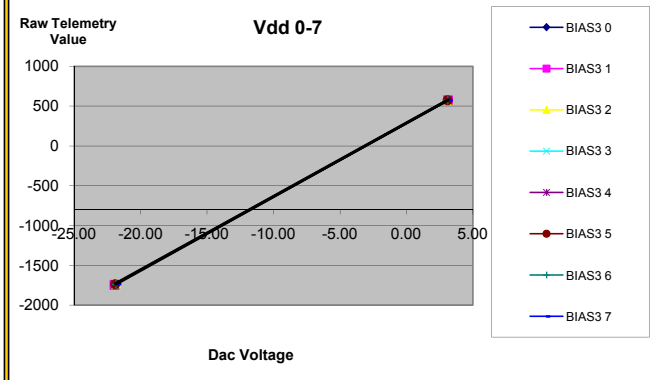
Vog	Slope		Offset
Mean	204.83	Mean	-3.72
Stdev	0.0833333	Stdev	0.2406242

Vdd	Slope		Offset
Mean	92.40	Mean	286.44
Stdev	0.1377856	Stdev	0.6696692









Stage 8C. Bias Voltage output enables testing - Table 8

Place a line through Bias Voltage name if enable/disable switch works

Vru 0	Vru 1	Vru 2	Vru 3	Vru 4	Vru 5
Vrl 0	Vrl 1	Vrl 2	Vrl 3	Vrl 4	Vrl 5
Vog 0	Vog 1	Vog 2	Vog 3	Vog 4	Vog 5
Vdd 0	Vdd 1	Vdd 2	Vdd 3	Vdd 4	Vdd 5

Stage 9. Vsub and Heater Control testing - Table 9

DAC Value	Vsub Measured Voltage Test Data 10%	50%	90%
Signal	volts	volts	volts
Vsub - rate	-1.25	3.73	8.71
Vsub - Limit	-1.25	3.73	8.71
Vsub0	0.00	0.00	0.00
	Vsub Enable Bit - pass		

DAC Value	Telemetery Readback Test Data 10%	50%	90%
Signal	dec	dec	dec
Vbias 0	154	270	453
Vbias 1	-28	691	1411
RTD1	219	NA	NA
RTD2	247	NA	NA
RTD3	275	NA	NA
RTD4	302	NA	NA
RTD5	325	NA	NA
RTD6	349	NA	NA
Reference 4096	836	NA	NA
eference buffere	836	NA	NA

Stage 10. Video Offset DAC Tests - Table 10.

	DAC Value 410				DAC Value 2048				DAC Value 3686			
ADC	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU
0	0.250	NA	NA	17193	1.250		NA	81161	2.250	NA	500ms	145121
1	0.250	NA	NA	16908	1.250		NA	80914	2.250	NA	500ms	144922
2	0.250	NA	NA	17092	1.250		NA	81129	2.250	NA	500ms	145165
3	0.250	NA	NA	17087	1.250		NA	81153	2.250	NA	500ms	145220
4	0.250	NA	NA	17172	1.250		NA	81147	2.250	NA	500ms	145128
5	0.250	NA	NA	17118	1.250		NA	81141	2.250	NA	500ms	145167
6	0.250	NA	NA	17025	1.250		NA	81088	2.250	NA	500ms	145145
7	0.250	NA	NA	16874	1.250		NA	80961	2.250	NA	500ms	145044
8	0.250	NA	NA	17130	1.250		NA	81110	2.250	NA	500ms	145082
9	0.250	NA	NA	17061	1.250		NA	81040	2.250	NA	500ms	145026
10	0.250	NA	NA	17280	1.250		NA	81219	2.250	NA	500ms	145148
11	0.250	NA	NA	16977	1.250		NA	81088	2.250	NA	500ms	145206

ADC	DC Volts		Data Set		
Channel	Slope	Offset	410	2048	3686
0	1638.000	0.500	0.250	1.250	2.250
1	1638.000	0.500	0.250	1.250	2.250
2	1638.000	0.500	0.250	1.250	2.250
3	1638.000	0.500	0.250	1.250	2.250
4	1638.000	0.500	0.250	1.250	2.250
5	1638.000	0.500	0.250	1.250	2.250
6	1638.000	0.500	0.250	1.250	2.250
7	1638.000	0.500	0.250	1.250	2.250
8	1638.000	0.500	0.250	1.250	2.250
9	1638.000	0.500	0.250	1.250	2.250
10	1638.000	0.500	0.250	1.250	2.250
11	1638.000	0.500	0.250	1.250	2.250

(dac# -offset)/slope=Voltage

ADC	ADU's		Data Set		
Channel	Slope	Offset	410	2048	3686
0	0.026	-30.32	17193	81161	145121
1	0.026	-22.68	16908	80914	144922
2	0.026	-27.20	17092	81129	145165
3	0.026	-26.86	17087	81153	145220
4	0.026	-29.62	17172	81147	145128
5	0.026	-27.93	17118	81141	145167
6	0.026	-25.35	17025	81088	145145
7	0.026	-21.31	16874	80961	145044
8	0.026	-28.62	17130	81110	145082
9	0.026	-26.74	17061	81040	145026
10	0.026	-32.76	17280	81219	145148
11	0.026	-23.70	16977	81088	145206

(dac# -offset)/slope=ADU

Notes and Observations

Checked for oscillations using a Agilent Oscilloscope on AC. OK

Stage 11. CDS Control Functions and Video Channel Performanc

TEST #1: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit is held static. The purpose of this test is to verify the correct operation of the ADC devices and measure the noise of the Offset voltage generators, ADC buffer amplifiers and ADC devices

Noise Test 1

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	81146	81161	81153.7	2.11626
CH 1	80902	80919	80911	2.2735
CH 2	81115	81131	81123	2.31818
CH 3	81141	81158	81149.2	2.37696
CH 4	81134	81152	81144.2	2.24768
CH 5	81127	81145	81136.3	2.31093
CH 6	81075	81092	81083.7	2.29479
CH 7	80948	80966	80958	2.35824
CH 8	81094	81111	81102.4	2.26915
CH 9	81031	81047	81039.1	2.33816
CH 10	81206	81224	81215.7	2.35107
CH 11	81082	81098	81090.5	2.32361

TEST #2: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the invert/non-invert and the DC Restore switches are held static.

Noise Test 2

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76561	76581	76571.3	2.77405
CH 1	76446	76467	76455.8	2.77478
CH 2	76678	76698	76688.4	2.77318
CH 3	76993	77015	77003.6	2.82661
CH 4	76496	76519	76507.2	2.74378
CH 5	76752	76771	76760.5	2.78128
CH 6	76738	76758	76748.9	2.76259
CH 7	76669	76689	76679.7	2.8272
CH 8	76572	76590	76581.1	2.5849
CH 9	76802	76825	76813.3	2.81203
CH 10	76714	76734	76723.9	2.72242
CH 11	76708	76728	76718	2.86023

TEST #3: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the DC Restore switch is held static.

Noise Test 3

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76562	76583	76573.6	2.98239
CH 1	76442	76463	76451.9	3.01274
CH 2	76673	76696	76683.9	3.00997
CH 3	76994	77015	77003.7	3.01507
CH 4	76489	76511	76499.4	2.86737
CH 5	76739	76761	76750.8	2.94401
CH 6	76735	76756	76745.4	3.01141
CH 7	76663	76684	76674	3.06628
CH 8	76562	76582	76572.8	3.00501
CH 9	76795	76819	76806.9	3.0869
CH 10	76718	76738	76727.7	3.00898
CH 11	76708	76729	76718.1	3.11049

TEST #4: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition.

Noise Test 4

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76553	76576	76565.5	3.0307
CH 1	76445	76467	76455.6	3.15232
CH 2	76674	76702	76687.6	3.18305
CH 3	76993	77014	77003.2	3.14569
CH 4	76523	76546	76533.4	3.1412
CH 5	76732	76755	76742.9	3.08999
CH 6	76738	76761	76750.4	3.18236
CH 7	76635	76658	76647.4	3.15715
CH 8	76601	76624	76613.3	3.05972
CH 9	76724	76746	76735.1	3.16281
CH 10	76734	76759	76745.6	3.22352
CH 11	76669	76692	76680.8	3.21692

TEST #5: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the circuitry set to high GAIN.

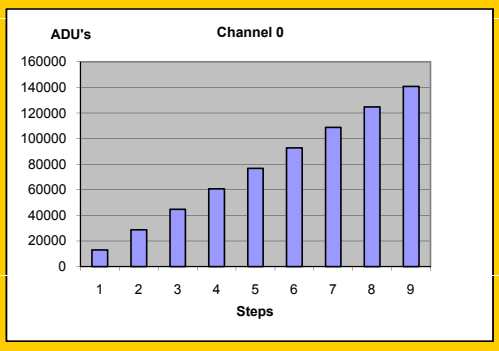
Noise Test 5

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76560	76585	76573.9	3.59946
CH 1	76452	76481	76467.5	3.57187
CH 2	76688	76716	76704.9	3.3892
CH 3	76995	77024	77009.5	3.73701
CH 4	76522	76552	76536.4	3.68872
CH 5	76729	76754	76741.1	3.59453
CH 6	76738	76765	76752.7	3.57464
CH 7	76636	76660	76647.8	3.64218
CH 8	76652	76677	76664.4	3.67151
CH 9	76722	76748	76734.8	3.60297
CH 10	76793	76821	76805.6	3.64063
CH 11	76666	76692	76679.8	3.68498

TEST #6A: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

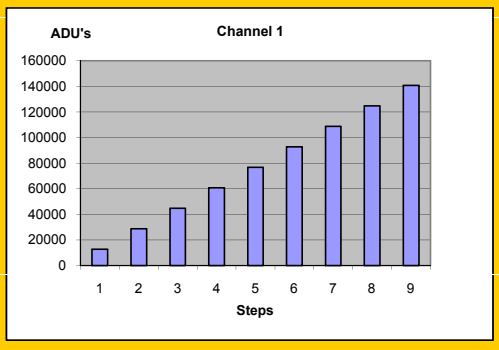
BrdTst6_006 / Channel 0					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12884	12905	12895.4	3.06068	10%
0x333	28856	28878	28867.7	3.15312	20%
0x4cc	44825	44848	44836.6	3.0835	30%
0x666	60837	60858	60847.8	3.08886	40%
0x800	76842	76867	76854.9	3.18766	50%
0x999	92816	92838	92827.4	3.0897	60%
0xb33	108828	108851	108839	2.94834	70%
0xccc	124800	124822	124812	3.11443	80%
0xe66	140812	140835	140823	3.08375	90%



TEST #6B: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

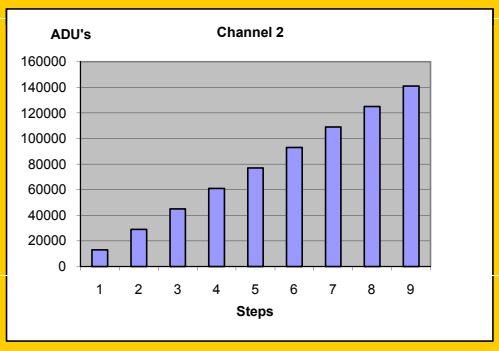
BrdTst6_006 / Channel 1					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12684	12707	12695.2	3.26217	10%
0x333	28667	28690	28677.1	3.08031	20%
0x4cc	44647	44669	44657.4	3.1935	30%
0x666	60668	60692	60678.9	3.12915	40%
0x800	76686	76709	76697.7	3.17981	50%
0x999	92669	92690	92678.6	3.0354	60%
0xb33	108688	108712	108700	3.12829	70%
0xccc	124673	124697	124684	3.14326	80%
0xe66	140695	140716	140705	2.99565	90%



TEST #6C: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

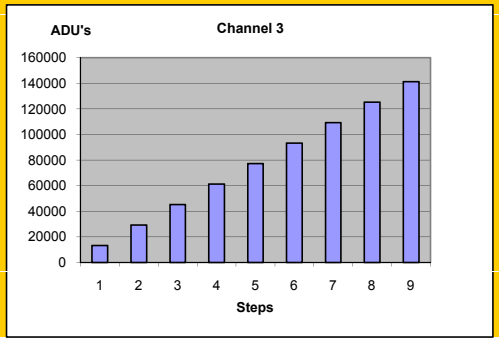
BrdTst6_006 / Channel 2					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12928	12950	12938.5	3.10217	10%
0x333	28919	28941	28929.4	2.97483	20%
0x4cc	44905	44930	44917.5	3.06685	30%
0x666	60938	60959	60947.5	3.13099	40%
0x800	76962	76986	76974.5	3.12209	50%
0x999	92953	92976	92964.7	2.86706	60%
0xb33	108984	109006	108995	3.05112	70%
0xccc	124973	124999	124985	3.13145	80%
0xe66	141003	141029	141015	3.03337	90%



TEST #6D: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

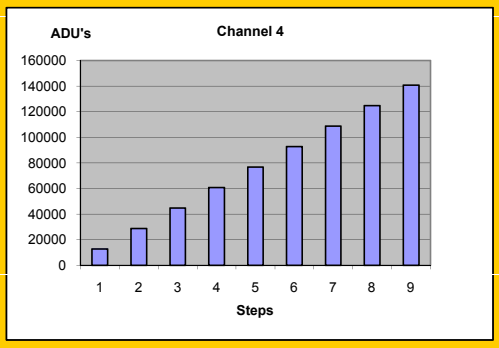
BrdTst6_006 / Channel 3					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13167	13189	13178.4	3.16953	10%
0x333	29165	29185	29175	3.06772	20%
0x4cc	45158	45182	45171.1	3.0283	30%
0x666	61195	61217	61206.5	3.16699	40%
0x800	77224	77248	77237.3	3.26032	50%
0x999	93219	93244	93231.6	3.27765	60%
0xb33	109258	109279	109269	3.13596	70%
0xccc	125257	125282	125268	3.0554	80%
0xe66	141293	141316	141304	3.20138	90%



TEST #6E: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

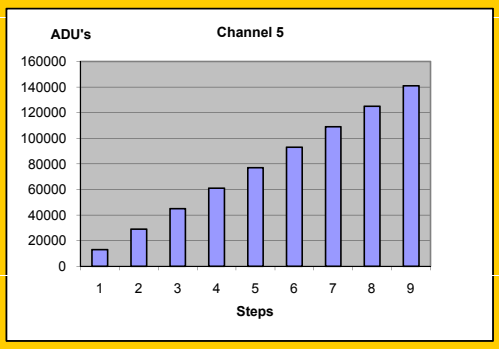
BrdTst6_006 / Channel 4					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12845	12866	12855.4	3.06829	10%
0x333	28821	28842	28831.8	3.19203	20%
0x4cc	44792	44814	44804.1	3.02559	30%
0x666	60809	60830	60818.7	2.97825	40%
0x800	76821	76843	76832.1	3.01072	50%
0x999	92798	92820	92809.5	3.14728	60%
0xb33	108812	108835	108824	3.10991	70%
0xccc	124785	124810	124799	3.14759	80%
0xe66	140803	140826	140815	3.09684	90%



TEST #6F: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

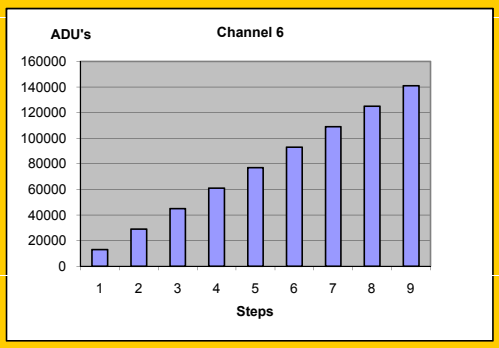
BrdTst6_006 / Channel 5					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12968	12990	12977.9	2.97442	10%
0x333	28951	28974	28962.5	2.98539	20%
0x4cc	44936	44959	44947.4	2.9423	30%
0x666	60960	60982	60971.1	3.1518	40%
0x800	76988	77012	76998.6	3.01951	50%
0x999	92975	92998	92986.7	3.14958	60%
0xb33	108999	109021	109011	3.21219	70%
0xccc	124987	125008	124998	3.08021	80%
0xe66	141012	141034	141023	3.1159	90%



TEST #6G: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

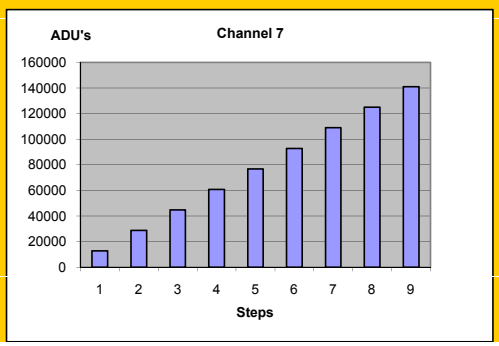
BrdTst6_006 / Channel 6					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12920	12944	12933.2	3.06225	10%
0x333	28918	28941	28929.9	3.1526	20%
0x4cc	44912	44935	44923.5	3.09499	30%
0x666	60948	60969	60958.8	3.03139	40%
0x800	76977	77000	76989.8	3.08732	50%
0x999	92974	92995	92985.2	3.07204	60%
0xb33	109009	109033	109022	3.11384	70%
0xccc	125005	125028	125017	3.17292	80%
0xe66	141044	141066	141054	3.12287	90%



TEST #6H: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

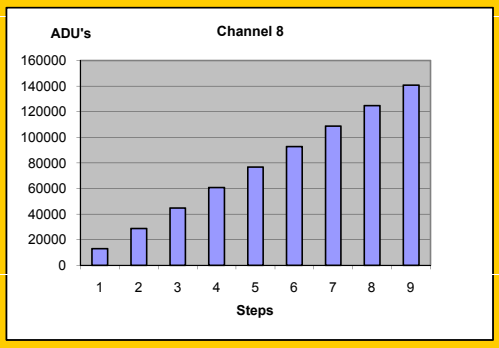
BrdTst6_006 / Channel 7					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12784	12808	12795.7	3.21726	10%
0x333	28784	28808	28796.9	3.17864	20%
0x4cc	44787	44810	44798.8	3.20344	30%
0x666	60828	60852	60838.6	3.17638	40%
0x800	76866	76886	76876	3.1962	50%
0x999	92868	92892	92880	3.21796	60%
0xb33	108905	108930	108919	3.15078	70%
0xccc	124912	124935	124924	3.22828	80%
0xe66	140953	140978	140967	3.22259	90%



TEST #6I: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

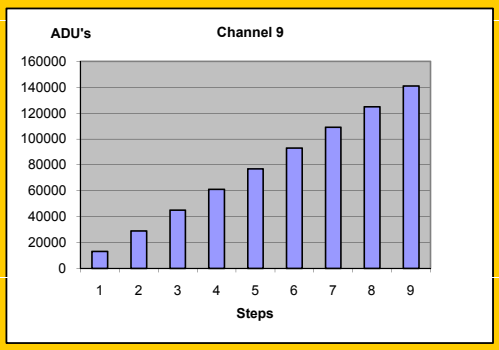
BrdTst6_006 / Channel 8					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12891	12915	12902.9	3.14996	10%
0x333	28867	28890	28877.8	3.06708	20%
0x4cc	44838	44860	44849.3	3.16298	30%
0x666	60852	60874	60863.7	3.13884	40%
0x800	76865	76888	76876.4	3.11208	50%
0x999	92842	92864	92853.3	3.15025	60%
0xb33	108856	108878	108867	3.01205	70%
0xccc	124828	124853	124841	3.1298	80%
0xe66	140844	140864	140855	3.02308	90%



TEST #6J: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

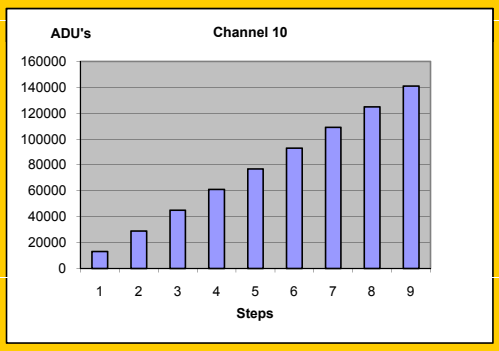
BrdTst6_006 / Channel 9					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13000	13022	13010.9	3.12199	10%
0x333	28976	28999	28986.9	3.24043	20%
0x4cc	44948	44973	44961.3	3.10738	30%
0x666	60964	60986	60976	3.12178	40%
0x800	76978	77001	76988.6	3.15915	50%
0x999	92955	92980	92968.2	3.11031	60%
0xb33	108972	108995	108982	3.11815	70%
0xccc	124947	124972	124959	3.21034	80%
0xe66	140966	140988	140976	3.16526	90%



TEST #6K: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

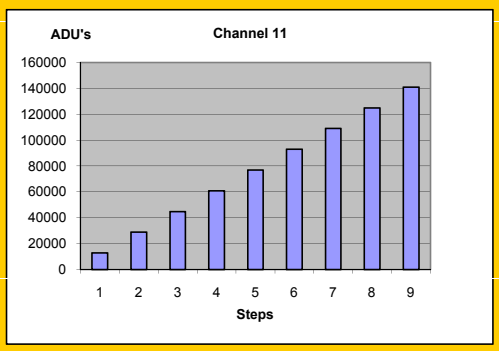
BrdTst6_006 / Channel 10					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13077	13099	13087.4	3.17385	10%
0x333	29042	29064	29053.8	3.19145	20%
0x4cc	45000	45028	45014.7	3.13552	30%
0x666	61010	61032	61019.5	3.20739	40%
0x800	77010	77033	77021.3	3.15725	50%
0x999	92976	93000	92987.8	3.19135	60%
0xb33	108978	109004	108992	3.15729	70%
0xccc	124942	124968	124955	3.16076	80%
0xe66	140951	140974	140962	3.20067	90%



TEST #6L: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

BrdTst6_006 / Channel 11					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12819	12842	12830.2	3.11834	10%
0x333	28831	28853	28842.2	3.28272	20%
0x4cc	44837	44861	44847.9	3.15918	30%
0x666	60884	60908	60897.8	3.07723	40%
0x800	76931	76952	76941.2	3.23188	50%
0x999	92943	92966	92953.9	3.27595	60%
0xb33	108994	109015	109004	3.30355	70%
0xccc	125000	125024	125013	3.08894	80%
0xe66	141053	141076	141064	3.19388	90%



Stage 13. Other Bit Tests. Table 11

Electronic Serial Number	0xDB8F8A		Board Serial Number	7
Firmware Version	0x193		Name Of Person Testing	S. Holm
Ident Register	0x502		Board passed Functional Tests	YES