DES 12 Channel Board - Functional Tests: CCD Acquisition Board Revision 1.0

Stage 1. Preparation of documentation and configuration settings - Table 1.

Board Part Number	#		Board Serial Number	1
Date Of Tests	November , 2009		Name Of Person Testing	S. Holm
Suggested Filename To Save	CCDACQ_12Ch_REPORT_BOARD#.xls		Sequence number: Test	

Stage 3. Power plane short test - Table 2.

Supply Name	Short test to ground: Impedance to ground	Test Point	
+1.2VD	65.00	TP43	~60 ohms
+1.8VD	1M	TPB12	> 1K ohm
+2.5VD	16k	TPB11	> 1K ohm
+3.3VD	23k	D13	> 1K ohm
+5VD	400k	D14	> 1K ohm
+5VA	1.1M	C267	> 1K ohm
-5VA	35k	C270	> 1K ohm
+15VA	1M	C288	> 1K ohm
-15VA	2M	C282	> 1K ohm
-28VA	500k	C307	> 1K ohm

Stage 4. Firmware programming tests - Table 3.

JTAG Order	Designator	Device	Load File	Check Sum or User Code
1	U122	XCF08PFS48C PROM	CcdAcqFpgaV41.mcs	0014ef670
2	U114	Spartan3 XC3S2000 FPGA	ccdacqfpgav41.bit	5102801

Stage 5. Power Consumption - Table 4.

Supply Name	Power Supply Consumption: Measured Voltage at test point	Measured Current on power supply	Test Point	
+1.2VD	1.20	N/A	TP43	
+1.8VD	1.80	N/A	TPB12	
+2.5VD	2.50	N/A	TPB11	
+3.3VD	3.30	0.116	D13	
+5VD	5.00	0.133	D14	
+5VA	5.00	0.615	C267	
-5VA	-5.00	0.444	C270	
+15VA	15.00	0.57	C288	
-15VA	-15.00	0.408	C282	
-28VA	-28.00	0.195	C307	
Vref 0+	10.03	N/A	R534	Vsub+ Reference(+10v)
Vref 0-	-2.50	N/A	R525	Vsub - Reference(-2.5v)
Vref Offset	2.50	N/A	R573	ADC Offset Reference(+2.5v)
Vclamp	1.80	N/A	VIA	ADC Clamp Voltage(+1.8v)
ADC Ref.	2.50	N/A	VIA	ADC Reference Voltage(+2.5v)
Vref 1+	2.50	N/A	R537	Vru and Vrl + Reference(+2.5v)
Vref 1-	-10.00	N/A	R535	Vru and Vrl - Reference(-10v)
Vref 2+	5.00	N/A	R563	Vog + Reference(+5v)
Vref 2-	-2.50	N/A	R555	Vog - Reference(-2.5v)
Vref 3+	2.50	N/A	R543	Vdd + Reference(+2.5v)
Vref 3-	-10.00	N/A	R571	Vdd - Reference(-10v)

Power Dissipation:
26.5 Watts

~27 watts +/- 5%

Stage 7. Basic Bus Transactions - **D**igital **Register** Tests - Table 5.

Register name	Put an X on any bit that has an error: 31-24	23-16	15-08	07-00	Function	Test name: Pattern	Walking 0's	Walking 1's
CDS Control			00000000	00000000	16 bit R/W			
Digital Output	00000000	00000000	00000000	00000000	32 bit R/W			
ADC Config.			0000	00000000	12 bit R/W			
Offset DAC			0000	00000000	12 bit R/W			
Bias DAC			0000	00000000	12 bit R/W			
Telemetry Config.				0000	4 bit R/W			
Auxilary Config.				00 00000000	10 bit R/W			
Redirect				0000	4 bit R/W			
Pixel Transfer				00000000	8 bit R/W			
Micro SEQ			00000000	00000000	16 bit R/W			
RAM Buffer			00000000	00000000	16 bit R/W			
LED Control				0000	4 bit R/W			
Control			00000000	00000000	16 bit R/W			
All Register Test	00000000	00000000	00000000	00000000	16 bit R/W	**YES**	**Passed**	**ALL**

Stage 8. Bias Voltage settings and output enables testing - Table 8

DAC Value	410	Bias Voltage Test Data 2048	3686	50% rms Noise	10-90% Rise Time			
Signal	volts	volts	volts	uV	millisec.	Fanout Brd	Slope	Offset
Vru 0	-13.14	-5.63	1.86	<10	10	BIAS 3	218.40	3279.05
Vru 1	-13.13	-5.63	1.86	<10	10	BIAS 4	218.55	3279.14
Vru 2	-13.14	-5.63	1.86	<10	10	BIAS 5	218.40	3279.05
Vru 3	-13.14	-5.64	1.86	<10	10	BIAS 6	218.40	3279.78
Vru 4	-13.15	-5.64	1.86	<10	10	BIAS 7	218.25	3279.68
Vru 5	-13.14	-5.64	1.86	<10	10	BIAS 8	218.40	3279.78
Vru 6	-13.12	-5.63	1.86	NA	NA	BIAS 9	218.69	3279.23
Vru 7	-13.13	-5.63	1.86	NA	NA	BIAS 10	218.55	3279.14
Vrl 0	-13.13	-5.63	1.86	<10	10	BIAS 11	218.55	3279.14
Vrl 1	-13.14	-5.63	1.86	<10	10	BIAS 12	218.40	3279.05
Vrl 2	-13.13	-5.63	1.86	<10	10	BIAS 13	218.55	3279.14
Vrl 3	-13.14	-5.64	1.86	<10	10	BIAS 14	218.40	3279.78
Vrl 4	-13.15	-5.64	1.86	<10	10	BIAS 15	218.25	3279.68
Vrl 5	-13.13	-5.64	1.86	<10	10	BIAS 16	218.55	3279.87
Vrl 6	-13.14	-5.64	1.86	NA	NA	BIAS 17	218.40	3279.78
Vrl 7	-13.16	-5.64	1.86	NA	NA	BIAS 18	218.11	3279.59
Vog 0	-1.75	1.25	4.25	<10	1	BIAS 19	546.00	1365.50
Vog 1	-1.75	1.25	4.25	<10	1	BIAS 20	546.00	1365.50
Vog 2	-1.75	1.25	4.25	<10	1	BIAS 21	546.00	1365.50
Vog 3	-1.75	1.25	4.25	<10	1	BIAS 22	546.00	1365.50
Vog 4	-1.75	1.25	4.25	<10	1	BIAS 23	546.00	1365.50
Vog 5	-1.75	1.25	4.25	<10	1	BIAS 24	546.00	1365.50
Vog 6	-1.75	1.25	4.25	NA	NA	BIAS 25	546.00	1365.50
Vog 7	-1.75	1.25	4.25	NA	NA	BIAS 26	546.00	1365.50
Vdd 0	-21.88	-9.39	3.11	<10	40	BIAS 27	131.09	3278.52
Vdd 1	-21.91	-9.40	3.12	<10	40	BIAS 28	130.88	3277.86
Vdd 2	-21.92	-9.40	3.12	<10	40	BIAS 29	130.83	3277.81
Vdd 3	-21.85	-9.37	3.12	<10	40	BIAS 30	131.20	3276.88
Vdd 4	-21.92	-9.40	3.11	<10	40	BIAS 21	130.88	3278.74
Vdd 5	-21.90	-9.39	3.12	<10	40	BIAS 32	130.94	3277.48
Vdd 6	-21.86	-9.37	3.11	NA	NA	BIAS 33	131.20	3277.76
Vdd 7	-21.87	-9.38	3.11	NA	NA	BIAS 34	131.14	3278.14

Vru	Slope		Offset
Mean	218.45	Mean	3279.36
Stdev	0.1248781	Stdev	0.307802738
Average	218.45464	Average	3279.355505
	Dac #	Average voltage	
	0	-15.0	
	4095	3.7	

Vrl	Slope		Offset
Mean	218.40	Mean	3279.50
Stdev	0.1455515	Stdev	0.314873256
Average	218.40005	Average	3279.502667
	Dac #	Average voltage	
	0	-15.0	
	4095	3.7	

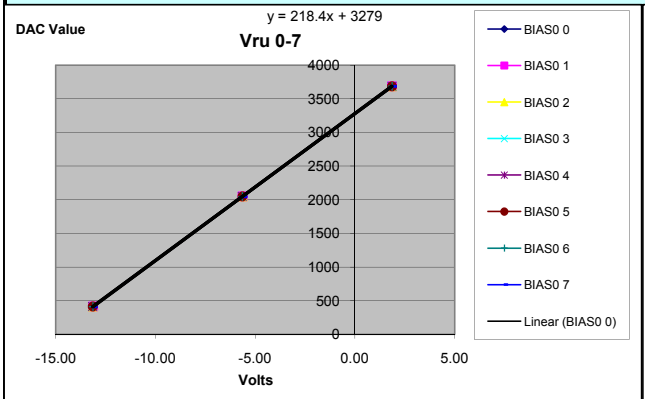
Vog	Slope		Offset
Mean	546.00	Mean	1365.50
Stdev	0	Stdev	0
Average	546	Average	1365.5
	Dac #	Average voltage	
	0	-2.5	
	4095	5.0	

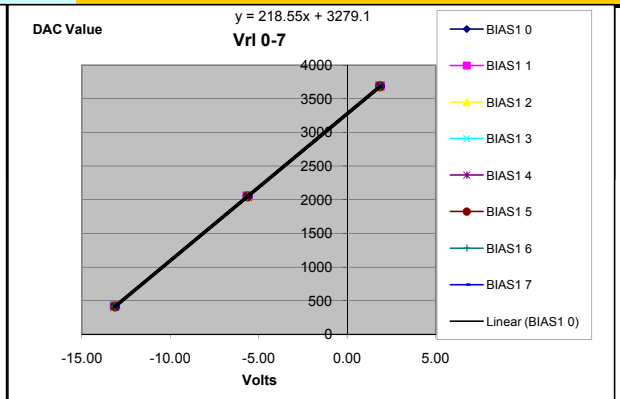
Vdd	Slope		Offset
Mean	131.02	Mean	3277.90
Stdev	0.1433584	Stdev	0.545600127
Average	131.0205	Average	3277.898695
	Dac #	Average voltage	
	0	-25.0	
	4095	6.2	

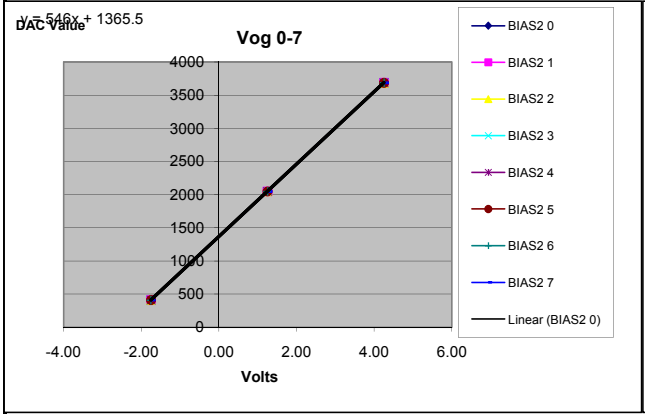
Notes and Observations

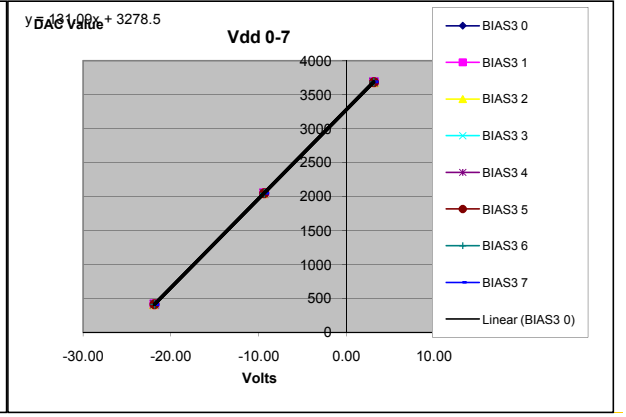
Checked for oscillations using a Agilent Oscilloscpe on AC. OK

average min & max voltages
(dac# -offset)/slope=voltage









Stage 8B. Telemetry System Tests - Table 7 (Bias Telemetry Tests)

DAC Value	410	3686	Bias Signals		Resolved Values for	
	Telemetry Return Values		Set Volts		Telemetry Channel	
Signal	10%	90%	10%	90%	Slope	Offset
Vru 0	-1730	423	-13.14	1.86	143.5333	156.03
Vru 1	-1729	423	-13.13	1.86	143.5624	155.97
Vru 2	-1729	424	-13.14	1.86	143.5333	157.03
Vru 3	-1731	424	-13.14	1.86	143.6667	156.78
Vru 4	-1731	424	-13.15	1.86	143.5710	156.96
Vru 5	-1728	423	-13.14	1.86	143.4000	156.28
Vru 6	-1730	423	-13.12	1.86	143.7250	155.67
Vru 7	-1731	424	-13.13	1.86	143.7625	156.60
Vrl 0	-1733	423	-13.13	1.86	143.8292	155.48
Vrl 1	-1736	423	-13.14	1.86	143.9333	155.28
Vrl 2	-1735	422	-13.13	1.86	143.8959	154.35
Vrl 3	-1735	423	-13.14	1.86	143.8667	155.41
Vrl 4	-1736	423	-13.15	1.86	143.8374	155.46
Vrl 5	-1739	423	-13.13	1.86	144.2295	154.73
Vrl 6	-1734	422	-13.14	1.86	143.7333	154.66
Vrl 7	-1734	423	-13.16	1.86	143.6085	155.89
Vog 0	-362	868	-1.75	4.25	205.0000	-3.25
Vog 1	-362	867	-1.75	4.25	204.8333	-3.54
Vog 2	-362	867	-1.75	4.25	204.8333	-3.54
Vog 3	-362	867	-1.75	4.25	204.8333	-3.54
Vog 4	-362	867	-1.75	4.25	204.8333	-3.54
Vog 5	-362	867	-1.75	4.25	204.8333	-3.54
Vog 6	-362	867	-1.75	4.25	204.8333	-3.54
Vog 7	-362	867	-1.75	4.25	204.8333	-3.54
Vdd 0	-1712	574	-21.88	3.11	91.4766	289.51
Vdd 1	-1719	575	-21.91	3.12	91.6500	289.05
Vdd 2	-1720	575	-21.92	3.12	91.6534	289.04
Vdd 3	-1713	574	-21.85	3.12	91.5899	288.24
Vdd 4	-1718	575	-21.92	3.11	91.6101	290.09
Vdd 5	-1719	575	-21.90	3.12	91.6867	288.94
Vdd 6	-1715	575	-21.86	3.11	91.7101	289.78
Vdd 7	-1715	575	-21.87	3.11	91.6733	289.90

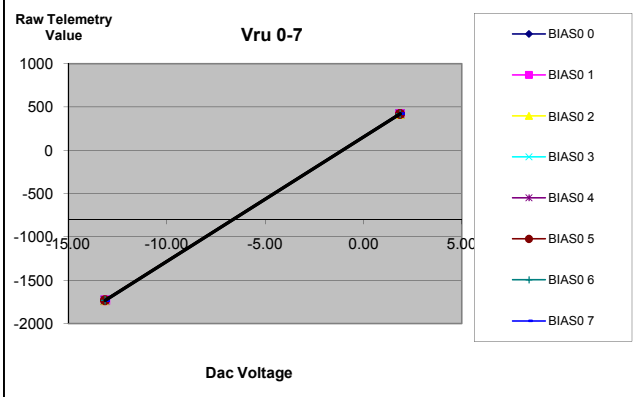
AVERAGE

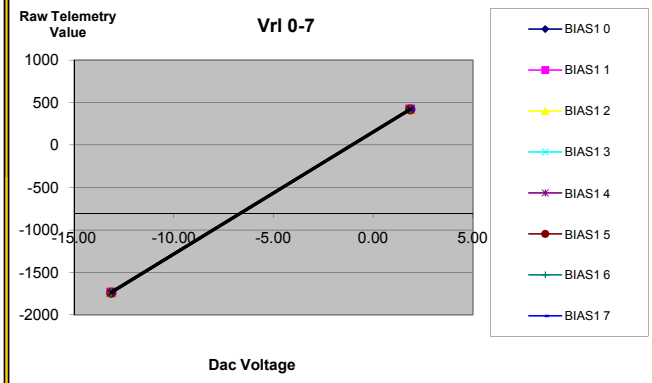
Vru	Slope		Offset
Mean	143.59	Mean	156.41
Stdev	0.1103151	Stdev	0.4683787

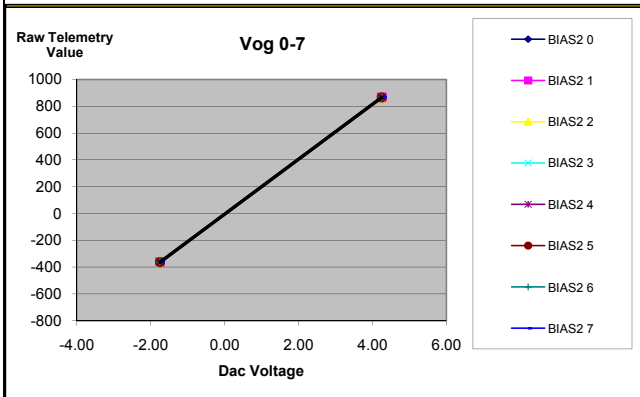
Vrl	Slope		Offset
Mean	143.87	Mean	155.16
Stdev	0.1671869	Stdev	0.4855295

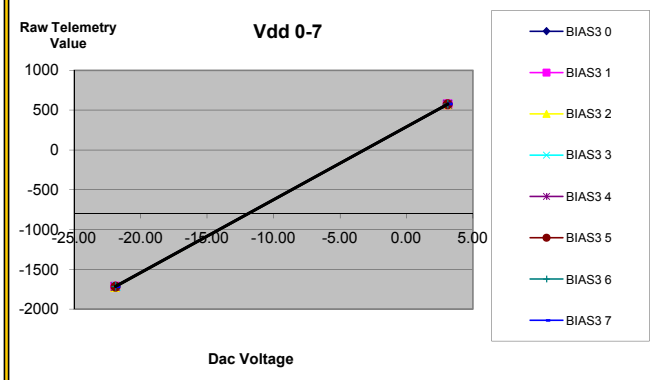
Vog	Slope		Offset
Mean	204.85	Mean	-3.51
Stdev	0.0551198	Stdev	0.0964597

Vdd	Slope		Offset
Mean	91.63	Mean	289.32
Stdev	0.0688919	Stdev	0.5744872









Stage 8C. Bias Voltage output enables testing - Table 8

Place a line through Bias Voltage name if enable/disable switch works

Vru 0	Vru 1	Vru 2	Vru 3	Vru 4	Vru 5
Vrl 0	Vrl 1	Vrl 2	Vrl 3	Vrl 4	Vrl 5
Vog 0	Vog 1	Vog 2	Vog 3	Vog 4	Vog 5
Vdd 0	Vdd 1	Vdd 2	Vdd 3	Vdd 4	Vdd 5

Stage 9. Vsub and Heater Control testing - Table 9

DAC	Vsub Measured Voltage	Test Data	
Value	10%	50%	90%
Signal	volts	volts	volts
Vsub - rate	-1.25	3.76	8.76

Vsub - Limit	-1.25	3.75	8.78
Vsub0	0.00	3.75	8.79
	Vsub Enable Bit - pass		

DAC	Telemetery Readback Test Data		
Value	10%	50%	90%
Signal	dec	dec	dec
Vbias 0	158.00	306.00	1101.00
Vbias 1	-21.00	695.00	1407.00
RTD1	219.00	NA	NA
RTD2	248.00	NA	NA
RTD3	275.00	NA	NA
RTD4	302.00	NA	NA
RTD5	325.00	NA	NA
RTD6	350.00	NA	NA
Reference 4096	836.00	NA	NA
eference buffere	836.00	NA	NA

Stage 10. Video Offset DAC Tests - Table 10.

	DAC Value 410				DAC Value 2048				DAC Value 3686			
ADC	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU
0	0.250	NA	NA	56472	1.250		NA	120577	2.250	NA	500ms	184677
1	0.250	NA	NA	55960	1.250		NA	120096	2.250	NA	500ms	184233
2	0.250	NA	NA	56262	1.250		NA	120311	2.250	NA	500ms	184350
3	0.250	NA	NA	56345	1.250		NA	120346	2.250	NA	500ms	184357
4	0.250	NA	NA	56105	1.250		NA	120178	2.250	NA	500ms	184250
5	0.250	NA	NA	56274	1.250		NA	120280	2.250	NA	500ms	184278
6	0.250	NA	NA	56243	1.250		NA	120281	2.250	NA	500ms	184331
7	0.250	NA	NA	56209	1.250		NA	120279	2.250	NA	500ms	184352
8	0.250	NA	NA	56069	1.250		NA	120145	2.250	NA	500ms	184232
9	0.250	NA	NA	56168	1.250		NA	120204	2.250	NA	500ms	184235
10	0.250	NA	NA	56318	1.250		NA	120344	2.250	NA	500ms	184387
11	0.250	NA	NA	56295	1.250		NA	120394	2.250	NA	500ms	184491

ADC	DC Volts		Data Set		
Channel	Slope	Offset	410	2048	3686
0	1638.000	0.500	0.250	1.250	2.250
1	1638.000	0.500	0.250	1.250	2.250
2	1638.000	0.500	0.250	1.250	2.250
3	1638.000	0.500	0.250	1.250	2.250
4	1638.000	0.500	0.250	1.250	2.250
5	1638.000	0.500	0.250	1.250	2.250
6	1638.000	0.500	0.250	1.250	2.250
7	1638.000	0.500	0.250	1.250	2.250
8	1638.000	0.500	0.250	1.250	2.250
9	1638.000	0.500	0.250	1.250	2.250
10	1638.000	0.500	0.250	1.250	2.250
11	1638.000	0.500	0.250	1.250	2.250

(dac# -offset)/slope=Voltage

ADC	ADU's		Data Set		
Channel	Slope	Offset	410	2048	3686
0	0.026	-1033.04	56472	120577	184677
1	0.026	-1019.17	55960	120096	184233
2	0.026	-1029.01	56262	120311	184350
3	0.026	-1031.90	56345	120346	184357
4	0.026	-1024.32	56105	120178	184250
5	0.026	-1030.25	56274	120280	184278
6	0.026	-1028.43	56243	120281	184331
7	0.026	-1026.98	56209	120279	184352
8	0.026	-1023.14	56069	120145	184232
9	0.026	-1026.82	56168	120204	184235
10	0.026	-1030.54	56318	120344	184387
11	0.026	-1028.61	56295	120394	184491

(dac# -offset)/slope=ADU

Notes and Observations

Checked for oscillations using a Agilent Oscilloscope on AC. OK

Stage 11. CDS Control Functions and Video Channel Performanc

TEST #1: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit is held static. The purpose of this test is to verify the correct operation of the ADC devices and measure the noise of the Offset voltage generators, ADC buffer amplifiers and ADC devices

Noise Test 1

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	104560	104581	104569	2.82931
CH 1	104074	104094	104083	2.9018
CH 2	104304	104325	104314	2.91869
CH 3	104360	104383	104372	2.88172
CH 4	104172	104190	104181	2.91743
CH 5	104285	104304	104296	2.85377
CH 6	104285	104306	104295	2.88275
CH 7	104273	104296	104283	2.93278
CH 8	104141	104161	104150	2.87348
CH 9	104207	104228	104216	2.94218
CH 10	104351	104371	104361	2.9906
CH 11	104380	104401	104390	2.97275

TEST #2: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the invert/non-invert and the DC Restore switches are held static.

Noise Test 2

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	99850	99872	99862.4	3.31603
CH 1	99800	99826	99811.2	3.14955
CH 2	99842	99864	99852.3	3.37313
CH 3	100269	100293	100282	3.44734
CH 4	99576	99600	99587.5	3.30707
CH 5	100068	100092	100080	3.23376
CH 6	99820	99845	99833.6	3.4392
CH 7	99938	99960	99948.8	3.38573
CH 8	99805	99828	99817.3	3.308
CH 9	100090	100113	100101	3.42636
CH 10	99814	99837	99825.1	3.30634
CH 11	100332	100355	100344	3.36077

TEST #3: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the DC Restore switch is held static.

Noise Test 3

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	99846	99870	99857.6	3.52267
CH 1	99788	99813	99802.7	3.45741
CH 2	99839	99863	99851.7	3.48022
CH 3	100270	100295	100283	3.7815
CH 4	99572	99596	99584.5	3.53689
CH 5	100066	100089	100077	3.40507
CH 6	99814	99838	99826.6	3.55004
CH 7	99939	99964	99951.5	3.49604
CH 8	99811	99836	99823.8	3.53253
CH 9	100089	100115	100103	3.58202
CH 10	99816	99842	99829.9	3.53771
CH 11	100332	100357	100344	3.46723

TEST #4: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition.

Noise Test 4

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	99843	99870	99854.9	3.68674
CH 1	99791	99820	99806.2	3.51556
CH 2	99840	99865	99853.7	3.59878
CH 3	100268	100298	100282	3.8038
CH 4	99605	99630	99616.9	3.67039
CH 5	100052	100078	100065	3.55065
CH 6	99819	99845	99832.6	3.74407
CH 7	99908	99933	99919.2	3.60295
CH 8	99851	99875	99862.7	3.47811
CH 9	100009	100034	100022	3.72767
CH 10	99830	99860	99847.9	3.73532
CH 11	100291	100318	100305	3.63778

TEST #5: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the circuitry set to high GAIN.

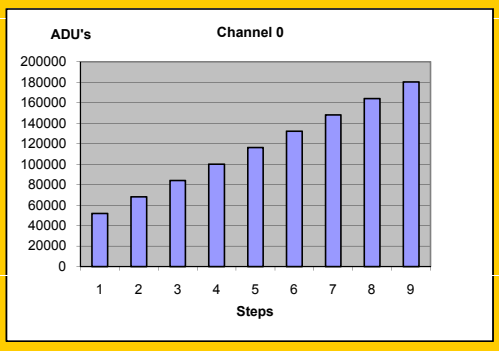
Noise Test 5

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	99841	99868	99855.4	3.69988
CH 1	99794	99818	99805.9	3.51945
CH 2	99840	99867	99853.3	3.60726
CH 3	100267	100296	100283	3.74745
CH 4	99605	99630	99618	3.57558
CH 5	100052	100080	100065	3.57736
CH 6	99820	99846	99831.9	3.77914
CH 7	99906	99933	99919.6	3.52317
CH 8	99848	99875	99862.6	3.50918
CH 9	100009	100034	100023	3.76145
CH 10	99831	99860	99847.4	3.77766
CH 11	100290	100318	100305	3.70056

TEST #6A: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

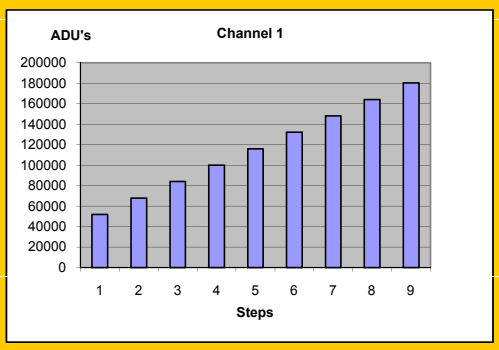
BrdTst6_006 / Channel 0					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	52026	52056	52039.9	3.75322	10%
0x333	68034	68060	68047.1	3.63173	20%
0x4cc	84040	84064	84050.9	3.5829	30%
0x666	100084	100108	100097	3.59848	40%
0x800	116128	116152	116139	3.62447	50%
0x999	132132	132160	132145	3.62584	60%
0xb33	148179	148208	148194	3.67046	70%
0xccc	164189	164214	164201	3.52692	80%
0xe66	180235	180261	180248	3.72029	90%



TEST #6B: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

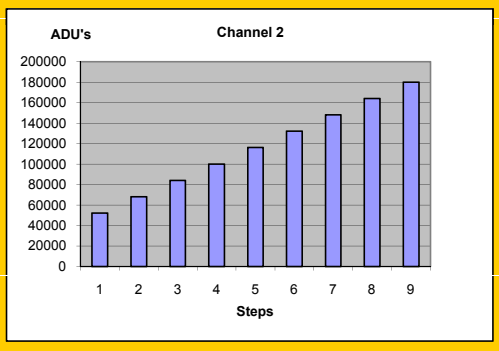
BrdTst6_006 / Channel 1					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	51896	51925	51910.7	3.68671	10%
0x333	67912	67940	67925.8	3.54786	20%
0x4cc	83923	83949	83936.8	3.49337	30%
0x666	99977	100004	99990.9	3.53723	40%
0x800	116026	116054	116039	3.59231	50%
0x999	132042	132068	132053	3.57177	60%
0xb33	148096	148121	148109	3.56297	70%
0xccc	164111	164135	164122	3.59075	80%
0xe66	180164	180189	180176	3.6229	90%



TEST #6C: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

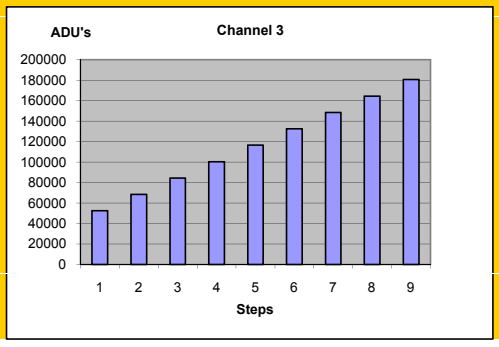
BrdTst6_006 / Channel 2					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	52053	52078	52066.8	3.50225	10%
0x333	68050	68073	68060.9	3.60993	20%
0x4cc	84038	84062	84050.2	3.60995	30%
0x666	100071	100099	100084	3.48194	40%
0x800	116098	116123	116110	3.53749	50%
0x999	132091	132117	132104	3.59228	60%
0xb33	148126	148153	148140	3.58897	70%
0xccc	164120	164145	164132	3.49752	80%
0xe66	180154	180178	180166	3.51576	90%



TEST #6D: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

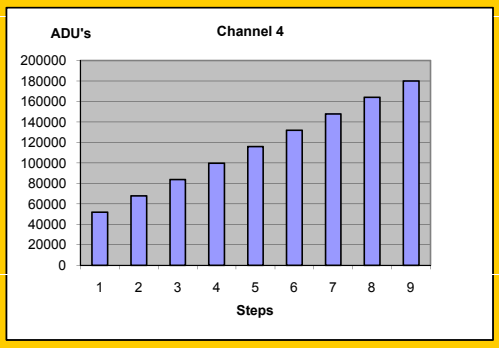
BrdTst6_006 / Channel 3					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	52468	52493	52480.4	3.88426	10%
0x333	68450	68480	68463.7	3.82606	20%
0x4cc	84434	84458	84446.2	3.79534	30%
0x666	100456	100480	100468	3.65518	40%
0x800	116473	116500	116486	3.69599	50%
0x999	132452	132481	132467	3.6962	60%
0xb33	148478	148503	148491	3.81445	70%
0xccc	164460	164489	164475	3.73111	80%
0xe66	180481	180513	180498	3.70894	90%



TEST #6E: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

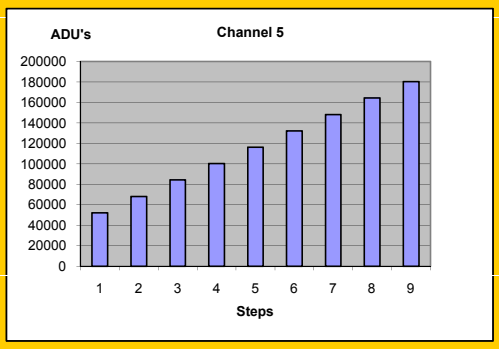
BrdTst6_006 / Channel 4					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	51800	51825	51811.7	3.75388	10%
0x333	67802	67827	67815.2	3.58307	20%
0x4cc	83796	83820	83808.9	3.53121	30%
0x666	99835	99862	99850.8	3.6667	40%
0x800	115873	115898	115886	3.59186	50%
0x999	131873	131897	131886	3.6074	60%
0xb33	147916	147942	147928	3.61357	70%
0xccc	163913	163939	163926	3.62142	80%
0xe66	179955	179983	179968	3.58088	90%



TEST #6F: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

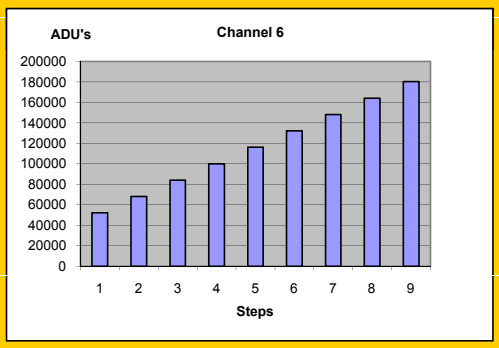
BrdTst6_006 / Channel 5					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	52265	52296	52278	3.62367	10%
0x333	68244	68274	68260.6	3.53025	20%
0x4cc	84226	84254	84239.3	3.70665	30%
0x666	100246	100273	100259	3.46843	40%
0x800	116262	116288	116275	3.58218	50%
0x999	132245	132272	132257	3.52102	60%
0xb33	148266	148295	148280	3.62159	70%
0xccc	164247	164272	164260	3.66953	80%
0xe66	180271	180294	180283	3.64739	90%



TEST #6G: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

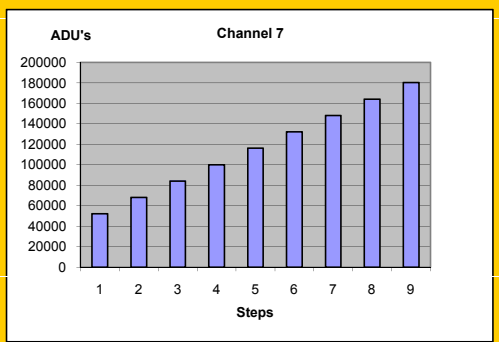
BrdTst6_006 / Channel 6					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	52064	52090	52076.7	3.69948	10%
0x333	68064	68088	68075.7	3.66443	20%
0x4cc	84059	84084	84072.7	3.74978	30%
0x666	100096	100123	100110	3.69492	40%
0x800	116131	116158	116144	3.76475	50%
0x999	132124	132152	132140	3.66882	60%
0xb33	148165	148192	148179	3.71077	70%
0xccc	164164	164193	164179	3.736	80%
0xe66	180206	180229	180218	3.62691	90%



TEST #6H: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

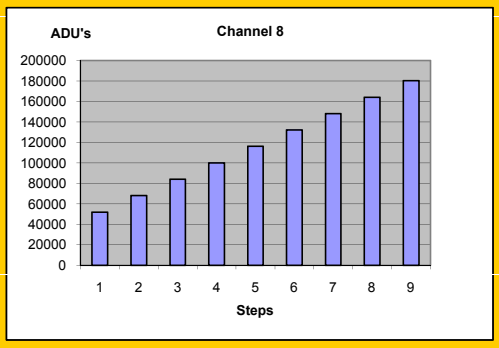
BrdTst6_006 / Channel 7					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	52064	52090	52076.7	3.69948	10%
0x333	68064	68088	68075.7	3.66443	20%
0x4cc	84059	84084	84072.7	3.74978	30%
0x666	100096	100123	100110	3.69492	40%
0x800	116131	116158	116144	3.76475	50%
0x999	132124	132152	132140	3.66882	60%
0xb33	148165	148192	148179	3.71077	70%
0xccc	164164	164193	164179	3.736	80%
0xe66	180206	180229	180218	3.62691	90%



TEST #6I: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

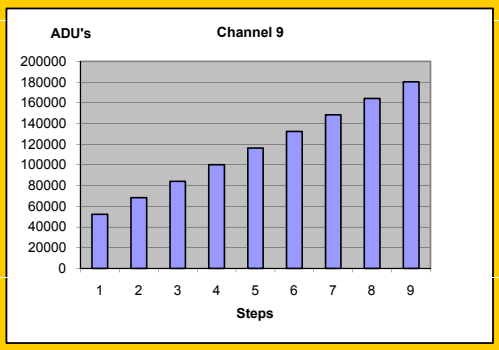
BrdTst6_006 / Channel 8					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	52020	52044	52032.7	3.56809	10%
0x333	68023	68049	68035.6	3.58147	20%
0x4cc	84024	84048	84035.8	3.60785	30%
0x666	100063	100089	100076	3.69302	40%
0x800	116101	116128	116115	3.47893	50%
0x999	132102	132131	132115	3.73321	60%
0xb33	148143	148175	148157	3.66157	70%
0xccc	164146	164173	164160	3.64523	80%
0xe66	180190	180216	180201	3.56854	90%



TEST #6J: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

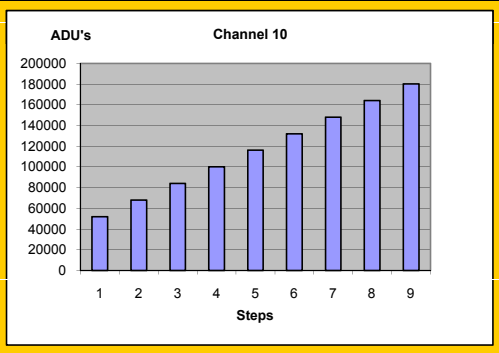
BrdTst6_006 / Channel 9					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	52208	52234	52221.7	3.71071	10%
0x333	68201	68224	68213.1	3.75557	20%
0x4cc	84188	84214	84200.8	3.65048	30%
0x666	100218	100245	100230	3.64977	40%
0x800	116239	116264	116252	3.65204	50%
0x999	132227	132256	132241	3.64193	60%
0xb33	148260	148285	148273	3.72652	70%
0xccc	164247	164276	164263	3.61133	80%
0xe66	180281	180311	180295	3.62663	90%



TEST #6K: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

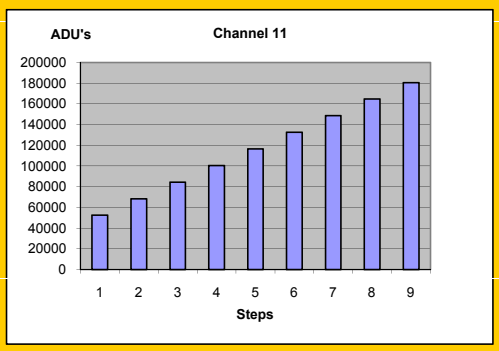
BrdTst6_006 / Channel 10					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	52048	52073	52060.3	3.71121	10%
0x333	68038	68064	68051.9	3.79272	20%
0x4cc	84028	84055	84040.8	3.74004	30%
0x666	100058	100084	100071	3.62136	40%
0x800	116086	116114	116098	3.564	50%
0x999	132074	132102	132089	3.62507	60%
0xb33	148107	148136	148121	3.69773	70%
0xccc	164098	164125	164112	3.61447	80%
0xe66	180130	180158	180144	3.76061	90%



TEST #6L: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

BrdTst6_006 / Channel 11					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	52454	52480	52467.1	3.70499	10%
0x333	68460	68485	68472.4	3.65389	20%
0x4cc	84465	84492	84478.6	3.63801	30%
0x666	100512	100538	100523	3.60266	40%
0x800	116551	116578	116566	3.62553	50%
0x999	132553	132583	132569	3.61688	60%
0xb33	148602	148628	148614	3.59504	70%
0xccc	164611	164638	164625	3.67533	80%
0xe66	180656	180683	180670	3.67755	90%



Stage 13. Other Bit Tests. Table 11

Electronic Serial Number	0xDB9130		Board Serial Number	1
Firmware Version	0x191		Name Of Person Testing	S. Holm
Ident Register	0x502		Board passed Functional Tests	YES