DES 12 Channel Board - Functional Tests: CCD Acquisition Board Revision 1.0

Stage 1. Preparation of documentation and configuration settings - Table 1.

Board Part Number	18	Board Serial Number	0xDB6FB8
Date Of Tests	June 2010	Name Of Person Testing	S. Holm
Suggested Filename To Save	CCDACQ_12Ch_REPORT_BOARD18.xl	Sequence number: Test	

Stage 3. Power plane short test - Table 2.

Supply Name	Short test to ground: Impedance to ground	Test Point	
+1.2VD	45.80	TP43	~50 ohms
+1.8VD	2M	TPB12	> 1K ohm
+2.5VD	18K	TPB11	> 1K ohm
+3.3VD	6.3k	D13	> 1K ohm
+5VD	19k	D14	> 1K ohm
+5VA	4M	C267	> 1K ohm
-5VA	311k	C270	> 1K ohm
+15VA	500k	C288	> 1K ohm
-15VA	500k	C282	> 1K ohm
-28VA	2.6M	C307	> 1K ohm

Stage 4. Firmware programming tests - Table 3.

JTAG Order	Designator	Device	Load File	Check Sum or User Code
1	U122	XCF08PFS48C PROM	CcdAcqFpgaV41.mcs	0014ef670
2	U114	Spartan3 XC3S2000 FPGA	ccdacqfpgav41.bit	5102801

Stage 5. Power Consumption - Table 4.

Supply Name	Power Supply Consumption: Measured Voltage at test point	Measured Current on power supply	Test Point	
+1.2VD	1.20	N/A	TP43	
+1.8VD	1.80	N/A	TPB12	
+2.5VD	2.51	N/A	TPB11	
+3.3VD	3.29	0.112	D13	
+5VD	5.21	0.155	D14	
+5VA	5.00	0.667	C267	
-5VA	-5.00	0.433	C270	
+15VA	15.00	0.556	C288	
-15VA	-15.09	0.408	C282	
-28VA	-28.00	0.219	C307	
Vref 0+	10.02	N/A	R534	Vsub+ Reference(+10v)
Vref 0-	-2.48	N/A	R525	Vsub - Reference(-2.5v)
Vref Offset	2.50	N/A	R573	ADC Offset Reference(+2.5v)
Vclamp	1.88	N/A	VIA	ADC Clamp Voltage(+1.8v)
ADC Ref.	2.50	N/A	VIA	ADC Reference Voltage(+2.5v)
Vref 1+	2.50	N/A	R537	Vru and Vrl + Reference(+2.5v)
Vref 1-	-9.97	N/A	R535	Vru and Vrl - Reference(-10v)
Vref 2+	5.01	N/A	R563	Vog + Reference(+5v)
Vref 2-	-2.48	N/A	R555	Vog - Reference(-2.5v)
Vref 3+	2.50	N/A	R543	Vdd + Reference(+2.5v)
Vref 3-	-9.97	N/A	R571	Vdd - Reference(-10v)

Power Dissipation:
27.3 Watts

~27 watts +/- 5%

Stage 7. Basic Bus Transactions - **D**igital **Register** Tests - Table 5.

Register name	Put an X on any bit that has an error: 31-24	23-16	15-08	07-00	Function	Test name: Pattern	Walking 0's	Walking 1's
CDS Control			00000000	00000000	16 bit R/W			
Digital Output	00000000	00000000	00000000	00000000	32 bit R/W			
ADC Config.			0000	00000000	12 bit R/W			
Offset DAC			0000	00000000	12 bit R/W			
Bias DAC			0000	00000000	12 bit R/W			
Telemetry Config.				0000	4 bit R/W			
Auxilary Config.			00	00000000	10 bit R/W			
Redirect				0000	4 bit R/W			
Pixel Transfer				00000000	8 bit R/W			
Micro SEQ			00000000	00000000	16 bit R/W			
RAM Buffer			00000000	00000000	16 bit R/W			
LED Control				0000	4 bit R/W			
Control			00000000	00000000	16 bit R/W			
All Register Test	00000000	00000000	00000000	00000000	16 bit R/W	**Passed**	**Passed**	**Passed**

Stage 8. Bias Voltage settings and output enables testing - Table 8

DAC Value	Bias Voltage Test Data 410	2048	3686	50% rms Noise	10-90% Rise Time			
Signal	volts	volts	volts	uV	millisec.	Fanout Brd	Slope	Offset
Vru 0	-13.09	-5.60	1.88	<10	2	BIAS 3	218.84	3274.22
Vru 1	-13.09	-5.60	1.88	<10	2	BIAS 4	218.84	3274.22
Vru 2	-13.07	-5.60	1.88	<10	2	BIAS 5	219.13	3274.40
Vru 3	-13.07	-5.60	1.88	<10	2	BIAS 6	219.13	3274.40
Vru 4	-13.06	-5.60	1.88	<10	2	BIAS 7	219.28	3274.49
Vru 5	-13.10	-5.60	1.88	<10	2	BIAS 8	218.69	3274.13
Vru 6	-13.09	-5.60	1.88	NA	NA	BIAS 9	218.84	3274.22
Vru 7	-13.09	-5.60	1.88	NA	NA	BIAS 10	218.84	3274.22
Vrl 0	-13.08	-5.60	1.88	<10	2	BIAS 11	218.98	3274.31
Vrl 1	-13.08	-5.60	1.88	<10	2	BIAS 12	218.98	3274.31
Vrl 2	-13.09	-5.60	1.88	<10	2	BIAS 13	218.84	3274.22
Vrl 3	-13.08	-5.60	1.88	<10	2	BIAS 14	218.98	3274.31
Vrl 4	-13.09	-5.60	1.88	<10	2	BIAS 15	218.84	3274.22
Vrl 5	-13.10	-5.60	1.88	<10	2	BIAS 16	218.69	3274.13
Vrl 6	-13.11	-5.60	1.88	NA	NA	BIAS 17	218.55	3274.04
Vrl 7	-13.06	-5.60	1.88	NA	NA	BIAS 18	219.28	3274.49
Vog 0	-1.73	1.26	4.26	<10	2	BIAS 19	546.91	1357.07
Vog 1	-1.73	1.26	4.26	<10	2	BIAS 20	546.91	1357.07
Vog 2	-1.73	1.26	4.26	<10	2	BIAS 21	546.91	1357.07
Vog 3	-1.73	1.26	4.26	<10	2	BIAS 22	546.91	1357.07
Vog 4	-1.73	1.26	4.26	<10	2	BIAS 23	546.91	1357.07
Vog 5	-1.73	1.26	4.26	<10	2	BIAS 24	546.91	1357.07
Vog 6	-1.73	1.26	4.26	NA	NA	BIAS 25	546.91	1357.07
Vog 7	-1.73	1.26	4.26	NA	NA	BIAS 26	546.91	1357.07
Vdd 0	-21.86	-9.37	3.13	<10	20	BIAS 27	131.09	3275.90
Vdd 1	-21.83	-9.36	3.12	<10	20	BIAS 28	131.30	3276.55
Vdd 2	-21.84	-9.36	3.13	<10	20	BIAS 29	131.20	3275.57
Vdd 3	-21.83	-9.35	3.13	<10	20	BIAS 30	131.25	3275.19
Vdd 4	-21.90	-9.38	3.14	<10	20	BIAS 21	130.83	3275.19
Vdd 5	-21.83	-9.35	3.14	<10	20	BIAS 32	131.20	3274.26
Vdd 6	-21.86	-9.36	3.13	NA	NA	BIAS 33	131.09	3275.46
Vdd 7	-21.84	-9.36	3.13	NA	NA	BIAS 34	131.20	3275.57

Vru	Slope		Offset
Mean	218.95	Mean	3274.29
Stdev	0.1901622	Stdev	0.116608638
Average	218.94748	Average	3274.287501
	Dac #	Average voltage	
	0	-14.0	
	4095	3.8	

Vrl	Slope		Offset
Mean	218.89	Mean	3274.25
Stdev	0.2061028	Stdev	0.126655345
Average	218.89262	Average	3274.253758
	Dac #	Average voltage	
	0	-15.0	
	4095	3.8	

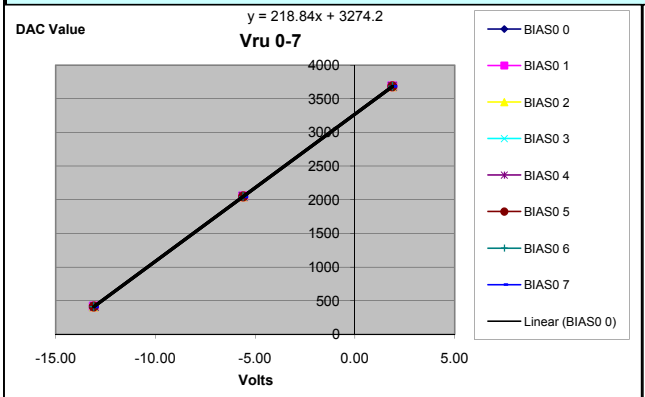
Vog	Slope		Offset
Mean	546.91	Mean	1357.07
Stdev	0	Stdev	2.27374E-13
Average	546.91101	Average	1357.069089
	Dac #	Average voltage	
	0	-2.5	
	4095	5.0	

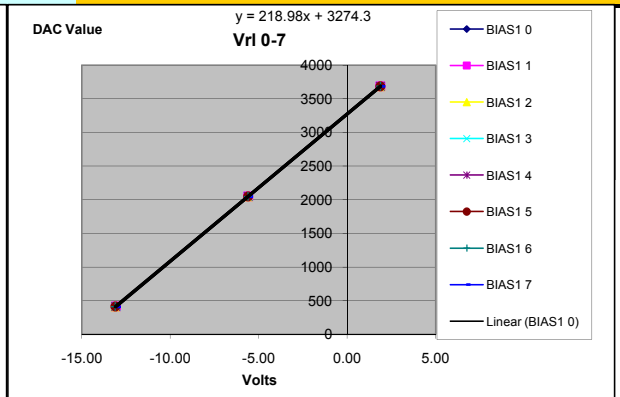
Vdd	Slope		Offset
Mean	131.15	Mean	3275.46
Stdev	0.1362162	Stdev	0.612882227
Average	131.14505	Average	3275.461867
	Dac #	Average voltage	
	0	-25.0	
	4095	6.3	

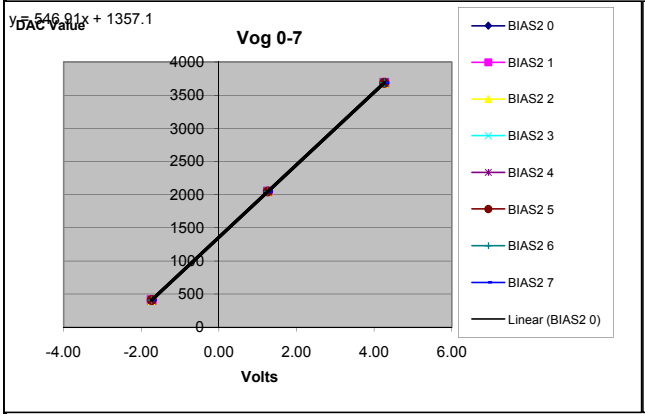
Notes and Observations

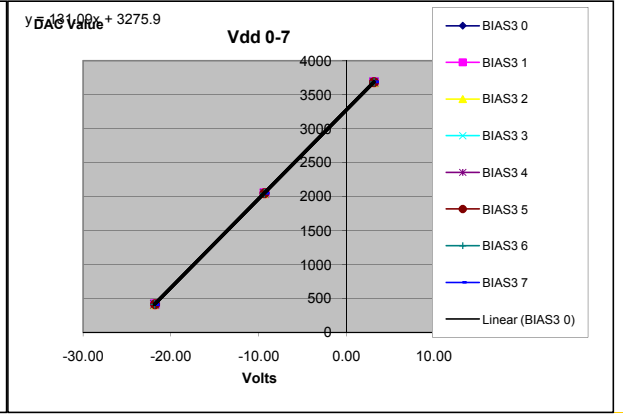
Checked for oscillations using a Agilent Oscilloscpe on AC.**OK**

average min & max voltages
(dac# -offset)/slope=voltage









Stage 8B. Telemetry System Tests - Table 7 (Bias Telemetry Tests)

DAC Value	410	3686	Bias Signals Set Volts		Resolved Values for Telemetry Channel	
	Telemetry Return Values					
Signal	10%	90%	10%	90%	Slope	Offset
Vru 0	-1735	424	-13.09	1.88	144.2218	152.86
Vru 1	-1737	424	-13.09	1.88	144.3554	152.61
Vru 2	-1736	424	-13.07	1.88	144.4816	152.37
Vru 3	-1737	423	-13.07	1.88	144.4816	151.37
Vru 4	-1737	424	-13.06	1.88	144.6452	152.07
Vru 5	-1741	425	-13.10	1.88	144.5928	153.17
Vru 6	-1743	424	-13.09	1.88	144.7562	151.86
Vru 7	-1734	423	-13.09	1.88	144.0882	152.11
Vrl 0	-1733	424	-13.08	1.88	144.1845	152.93
Vrl 1	-1733	425	-13.08	1.88	144.2513	153.81
Vrl 2	-1738	425	-13.09	1.88	144.4890	153.36
Vrl 3	-1734	424	-13.08	1.88	144.2513	152.81
Vrl 4	-1735	424	-13.09	1.88	144.2218	152.86
Vrl 5	-1738	425	-13.10	1.88	144.3925	153.54
Vrl 6	-1737	424	-13.11	1.88	144.1628	152.97
Vrl 7	-1739	424	-13.06	1.88	144.7791	151.82
Vog 0	-358	868	-1.73	4.26	204.6745	-3.91
Vog 1	-358	868	-1.73	4.26	204.6745	-3.91
Vog 2	-358	868	-1.73	4.26	204.6745	-3.91
Vog 3	-358	868	-1.73	4.26	204.6745	-3.91
Vog 4	-358	868	-1.73	4.26	204.6745	-3.91
Vog 5	-358	868	-1.73	4.26	204.6745	-3.91
Vog 6	-358	868	-1.73	4.26	204.6745	-3.91
Vog 7	-358	868	-1.73	4.26	204.6745	-3.91
Vdd 0	-1718	575	-21.86	3.13	91.7567	287.80
Vdd 1	-1715	575	-21.83	3.12	91.7836	288.64
Vdd 2	-1718	575	-21.84	3.13	91.8302	287.57
Vdd 3	-1713	575	-21.83	3.13	91.6667	288.08
Vdd 4	-1718	576	-21.90	3.14	91.6134	288.33
Vdd 5	-1721	575	-21.83	3.14	91.9503	286.28
Vdd 6	-1730	576	-21.86	3.13	92.2769	287.17
Vdd 7	-1718	576	-21.84	3.13	91.8702	288.45

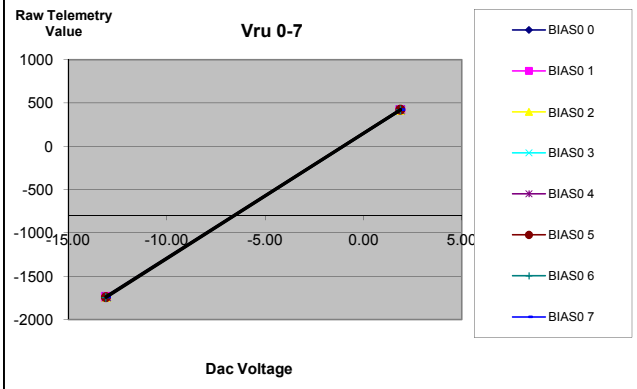
AVERAGE

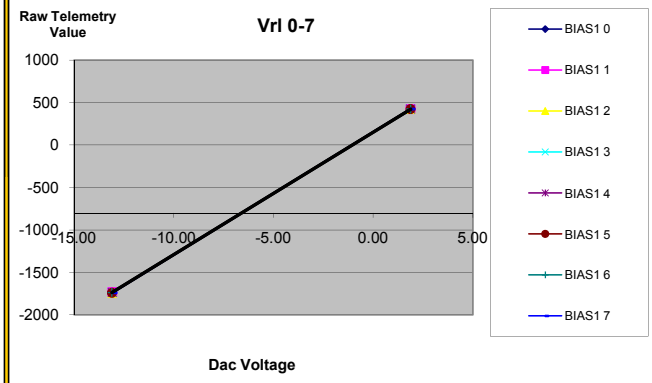
Vru	Slope		Offset
Mean	144.45	Mean	152.30
Stdev	0.2080099	Stdev	0.5372622

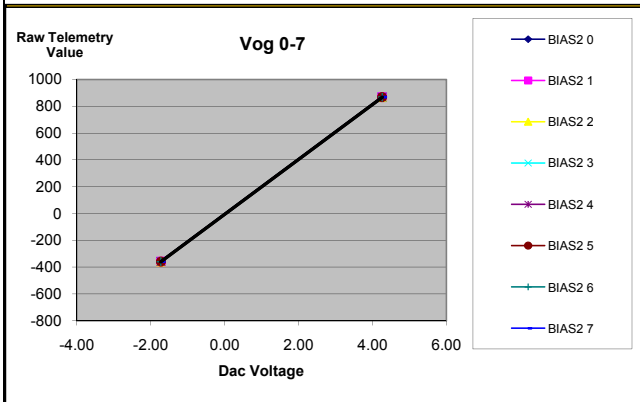
Vrl	Slope		Offset
Mean	144.34	Mean	153.01
Stdev	0.1946303	Stdev	0.5633841

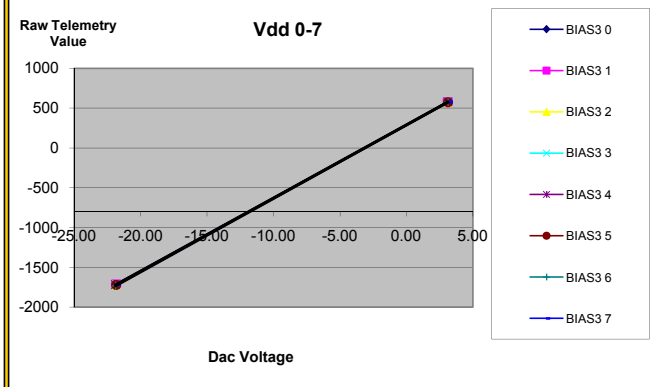
Vog	Slope		Offset
Mean	204.67	Mean	-3.91
Stdev	2.842E-14	Stdev	0

Vdd	Slope		Offset
Mean	91.84	Mean	287.79
Stdev	0.1921865	Stdev	0.7286522









Stage 8C. Bias Voltage output enables testing - Table 8

Place a line through Bias Voltage name if enable/disable switch works

Vru 0	Vru 1	Vru 2	Vru 3	Vru 4	Vru 5
Vrl 0	Vrl 1	Vrl 2	Vrl 3	Vrl 4	Vrl 5
Vog 0	Vog 1	Vog 2	Vog 3	Vog 4	Vog 5
Vdd 0	Vdd 1	Vdd 2	Vdd 3	Vdd 4	Vdd 5

Stage 9. Vsub and Heater Control testing - Table 9

DAC Value	Vsub Measured Voltage Test Data 10%	50%	90%
Signal	volts	volts	volts
Vsub - rate	-1.23	3.76	8.76
Vsub - Limit	-1.23	3.76	8.76
Vsub0	0.00	0.00	0.00
	Vsub Enable Bit - pass		

DAC Value	Telemetery Readback Test Data 10%	50%	90%
Signal	dec	dec	dec
Vbias 0	131	263	439
Vbias 1	-25	696	1417
RTD1	218	NA	NA
RTD2	250	NA	NA
RTD3	275	NA	NA
RTD4	301	NA	NA
RTD5	326	NA	NA
RTD6	352	NA	NA
Reference 4096	836	NA	NA
eference buffere	836	NA	NA

Stage 10. Video Offset DAC Tests - Table 10.

	DAC Value 410				DAC Value 2048				DAC Value 3686			
ADC	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU
0	0.250	NA	NA	17284	1.250		NA	81216	2.250	NA	500ms	145144
1	0.250	NA	NA	17200	1.250		NA	81214	2.250	NA	500ms	145236
2	0.250	NA	NA	17179	1.250		NA	81141	2.250	NA	500ms	145121
3	0.250	NA	NA	16977	1.250		NA	81011	2.250	NA	500ms	145042
4	0.250	NA	NA	16927	1.250		NA	81028	2.250	NA	500ms	145121
5	0.250	NA	NA	16845	1.250		NA	81001	2.250	NA	500ms	145150
6	0.250	NA	NA	17065	1.250		NA	81112	2.250	NA	500ms	145152
7	0.250	NA	NA	17062	1.250		NA	81087	2.250	NA	500ms	145108
8	0.250	NA	NA	17082	1.250		NA	81156	2.250	NA	500ms	145225
9	0.250	NA	NA	16918	1.250		NA	80984	2.250	NA	500ms	145057
10	0.250	NA	NA	17080	1.250		NA	81187	2.250	NA	500ms	145299
11	0.250	NA	NA	16928	1.250		NA	80978	2.250	NA	500ms	145020

ADC	DC Volts		Data Set		
Channel	Slope	Offset	410	2048	3686
0	1638.000	0.500	0.250	1.250	2.250
1	1638.000	0.500	0.250	1.250	2.250
2	1638.000	0.500	0.250	1.250	2.250
3	1638.000	0.500	0.250	1.250	2.250
4	1638.000	0.500	0.250	1.250	2.250
5	1638.000	0.500	0.250	1.250	2.250
6	1638.000	0.500	0.250	1.250	2.250
7	1638.000	0.500	0.250	1.250	2.250
8	1638.000	0.500	0.250	1.250	2.250
9	1638.000	0.500	0.250	1.250	2.250
10	1638.000	0.500	0.250	1.250	2.250
11	1638.000	0.500	0.250	1.250	2.250

(dac# -offset)/slope=Voltage

ADC	ADU's		Data Set		
Channel	Slope	Offset	410	2048	3686
0	0.026	-32.86	17284	81216	145144
1	0.026	-30.05	17200	81214	145236
2	0.026	-29.80	17179	81141	145121
3	0.026	-24.30	16977	81011	145042
4	0.026	-22.60	16927	81028	145121
5	0.026	-20.13	16845	81001	145150
6	0.026	-26.49	17065	81112	145152
7	0.026	-26.54	17062	81087	145108
8	0.026	-26.73	17082	81156	145225
9	0.026	-22.50	16918	80984	145057
10	0.026	-26.37	17080	81187	145299
11	0.026	-22.97	16928	80978	145020

(dac# -offset)/slope=ADU

Notes and Observations

Checked for oscillations using a Agilent Oscilloscope on AC. OK

Stage 11. CDS Control Functions and Video Channel Performanc

TEST #1: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit is held static. The purpose of this test is to verify the correct operation of the ADC devices and measure the noise of the Offset voltage generators, ADC buffer amplifiers and ADC devices

Noise Test 1

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	145136	145152	145143	2.20678
CH 1	145226	145243	145234	2.32672
CH 2	145107	145125	145116	2.31254
CH 3	145033	145050	145041	2.3634
CH 4	145116	145131	145123	2.0845
CH 5	145144	145160	145152	2.2571
CH 6	145146	145162	145154	2.17274
CH 7	145102	145119	145111	2.44248
CH 8	145215	145234	145223	2.27688
CH 9	145046	145064	145056	2.38496
CH 10	145289	145308	145297	2.38302
CH 11	145014	145030	145022	2.33609

TEST #2: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the invert/non-invert and the DC Restore switches are held static.

Noise Test 2

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76512	76531	76520.7	2.76063
CH 1	76939	76960	76950.2	2.86216
CH 2	76500	76521	76510.3	2.78942
CH 3	76684	76706	76694.9	2.81984
CH 4	76267	76286	76276.8	2.69495
CH 5	76631	76650	76641.2	2.81733
CH 6	77083	77104	77094.8	2.70104
CH 7	76951	76973	76962.1	2.70961
CH 8	76714	76734	76724.3	2.59515
CH 9	76782	76803	76792.6	2.85958
CH 10	76604	76626	76613.9	2.87174
CH 11	76600	76620	76610	2.84732

TEST #3: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the DC Restore switch is held static.

Noise Test 3

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76499	76519	76509.5	2.91224
CH 1	76937	76958	76947.3	2.98437
CH 2	76488	76507	76496.8	2.95627
CH 3	76680	76700	76689.9	3.02819
CH 4	76265	76286	76275.5	3.03079
CH 5	76621	76644	76634.1	2.9845
CH 6	77078	77099	77088.4	2.92527
CH 7	76962	76983	76972.9	3.10928
CH 8	76717	76738	76728.1	2.87661
CH 9	76782	76805	76794.6	3.05205
CH 10	76607	76630	76619.4	3.09146
CH 11	76598	76620	76608.4	3.05906

TEST #4: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition.

Noise Test 4

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76491	76513	76501.6	2.96568
CH 1	76941	76962	76951.3	3.19841
CH 2	76488	76511	76499.9	3.14632
CH 3	76679	76701	76690.1	3.20615
CH 4	76299	76320	76308.2	2.88664
CH 5	76610	76634	76623.3	3.1656
CH 6	77087	77108	77096.6	3.13029
CH 7	76918	76940	76929.7	3.09236
CH 8	76756	76780	76768.3	2.99164
CH 9	76702	76724	76712.5	3.13638
CH 10	76625	76646	76636.7	3.15533
CH 11	76559	76580	76568.5	3.19871

TEST #5: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the circuitry set to high GAIN.

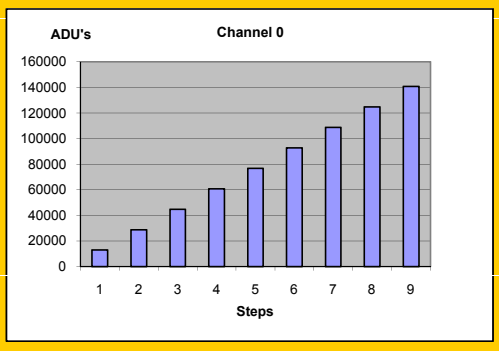
Noise Test 5

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76498	76524	76510.8	3.56595
CH 1	76948	76977	76962.2	3.60189
CH 2	76502	76529	76516.2	3.65676
CH 3	76684	76710	76696.6	3.65598
CH 4	76300	76324	76312.8	3.56224
CH 5	76609	76634	76621.1	3.6248
CH 6	77086	77112	77100	3.63525
CH 7	76916	76944	76929.3	3.56337
CH 8	76807	76832	76820.2	3.6858
CH 9	76698	76724	76712.4	3.71647
CH 10	76689	76714	76701.2	3.74736
CH 11	76558	76583	76569.1	3.6786

TEST #6A: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

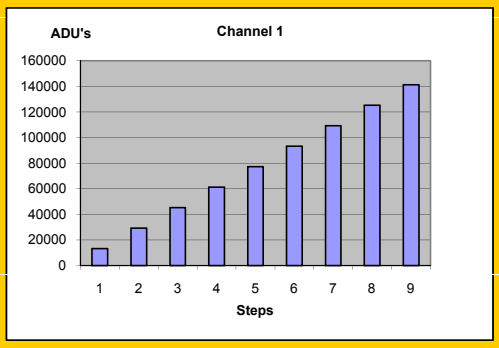
BrdTst6_006 / Channel 0					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12875	12897	12884.8	2.95252	10%
0x333	28835	28857	28845.8	3.09058	20%
0x4cc	44798	44823	44810.5	3.12256	30%
0x666	60799	60821	60810.7	3.12948	40%
0x800	76798	76819	76808.7	3.08284	50%
0x999	92761	92785	92772.1	3.08836	60%
0xb33	108761	108784	108774	3.21763	70%
0xccc	124729	124752	124741	3.10163	80%
0xe66	140732	140755	140743	3.04904	90%



TEST #6B: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

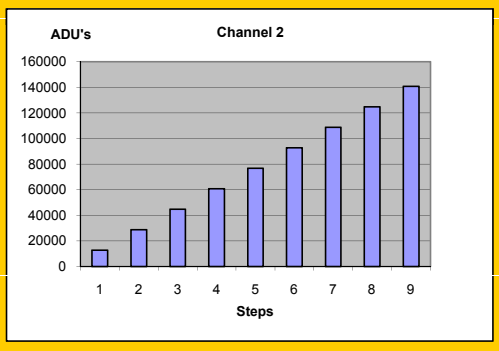
BrdTst6_006 / Channel 1					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13173	13194	13183.1	3.12386	10%
0x333	29152	29176	29164.8	3.1625	20%
0x4cc	45137	45160	45149	3.14843	30%
0x666	61157	61181	61168.9	3.08365	40%
0x800	77183	77205	77193.5	3.1378	50%
0x999	93169	93192	93180.6	3.18891	60%
0xb33	109189	109213	109201	3.11559	70%
0xccc	125179	125202	125190	3.05852	80%
0xe66	141198	141223	141210	3.12014	90%



TEST #6C: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

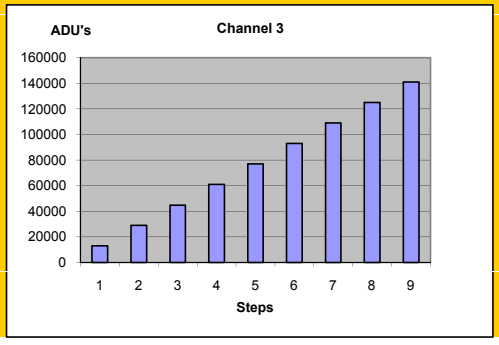
BrdTst6_006 / Channel 2					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12816	12841	12827.8	3.17671	10%
0x333	28786	28809	28797.9	3.09854	20%
0x4cc	44760	44784	44773.6	3.13312	30%
0x666	60769	60792	60781.4	3.10768	40%
0x800	76783	76806	76794.7	3.16558	50%
0x999	92757	92782	92769	3.03376	60%
0xb33	108767	108790	108779	3.23235	70%
0xccc	124745	124766	124755	3.17429	80%
0xe66	140755	140776	140765	3.16684	90%



TEST #6D: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

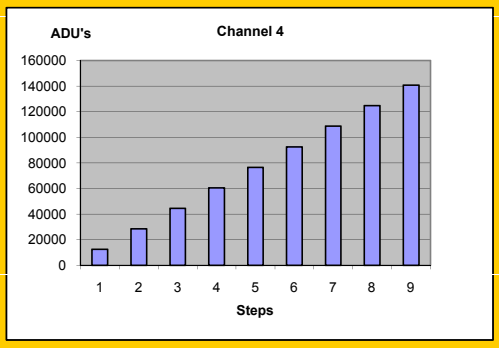
BrdTst6_006 / Channel 3					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12893	12918	12906.5	3.1525	10%
0x333	28878	28903	28889.5	3.21948	20%
0x4cc	44869	44892	44880.3	3.17866	30%
0x666	60890	60914	60902.6	3.10179	40%
0x800	76919	76943	76931.1	3.27791	50%
0x999	92910	92934	92922.8	3.15304	60%
0xb33	108934	108957	108946	3.04012	70%
0xccc	124928	124949	124939	3.13271	80%
0xe66	140952	140974	140962	3.06354	90%



TEST #6E: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

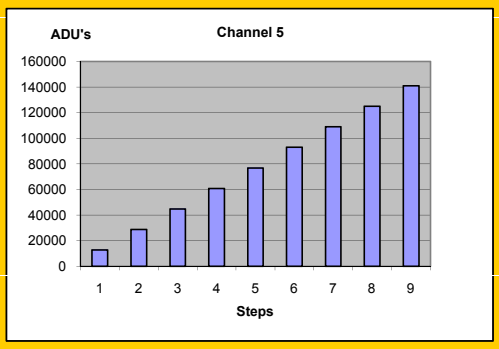
BrdTst6_006 / Channel 4					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12507	12532	12520.1	3.13126	10%
0x333	28515	28538	28526	3.05133	20%
0x4cc	44516	44540	44527.3	3.01689	30%
0x666	60558	60583	60572.4	3.05922	40%
0x800	76600	76625	76611.4	2.94343	50%
0x999	92605	92628	92615.9	3.13714	60%
0xb33	108649	108673	108661	3.10239	70%
0xccc	124653	124677	124664	3.1105	80%
0xe66	140698	140721	140709	3.10894	90%



TEST #6F: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

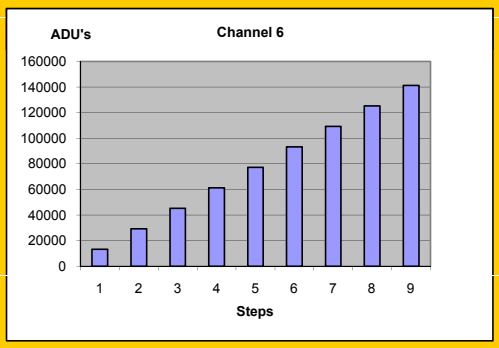
BrdTst6_006 / Channel 5					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12710	12738	12723.6	3.07096	10%
0x333	28732	28756	28744	3.13493	20%
0x4cc	44746	44768	44757.2	3.03257	30%
0x666	60802	60828	60816.6	3.0622	40%
0x800	76859	76880	76869.9	3.1693	50%
0x999	92878	92899	92888.3	3.10587	60%
0xb33	108937	108960	108948	3.14517	70%
0xccc	124950	124974	124962	3.26338	80%
0xe66	141011	141033	141023	3.1802	90%



TEST #6G: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

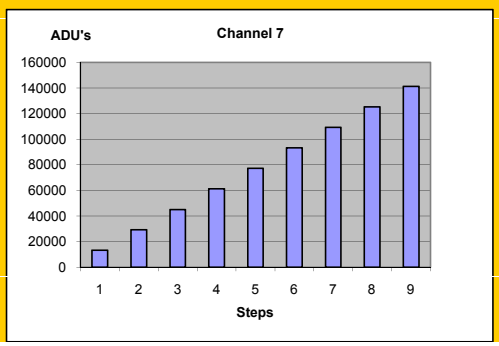
BrdTst6_006 / Channel 6					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13284	13307	13295.3	3.11653	10%
0x333	29276	29300	29289	3.20415	20%
0x4cc	45266	45288	45277	3.14644	30%
0x666	61299	61322	61310.3	3.09947	40%
0x800	77320	77344	77332.4	3.06592	50%
0x999	93312	93331	93321.6	3.15778	60%
0xb33	109345	109366	109354	3.1255	70%
0xccc	125332	125355	125344	3.12246	80%
0xe66	141364	141388	141377	3.04984	90%



TEST #6H: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

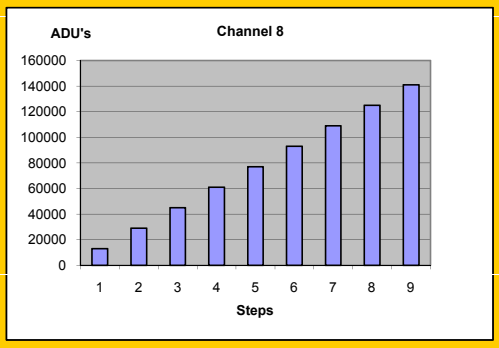
BrdTst6_006 / Channel 7					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13148	13172	13159.7	3.14523	10%
0x333	29135	29159	29146.5	3.19515	20%
0x4cc	45118	45143	45130	3.25954	30%
0x666	61146	61168	61157	3.08513	40%
0x800	77165	77190	77178.4	3.13854	50%
0x999	93153	93175	93164.9	3.17995	60%
0xb33	109181	109204	109193	3.20891	70%
0xccc	125166	125191	125178	3.29903	80%
0xe66	141195	141218	141206	3.11384	90%



TEST #6I: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

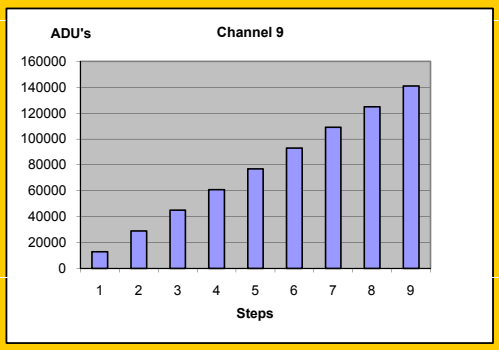
BrdTst6_006 / Channel 8					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12956	12978	12966.9	3.08915	10%
0x333	28951	28972	28962	2.98427	20%
0x4cc	44952	44974	44963.3	3.23085	30%
0x666	60987	61009	60997.6	3.02373	40%
0x800	77023	77044	77033.7	3.10813	50%
0x999	93024	93046	93034.5	3.07998	60%
0xb33	109057	109080	109069	3.11008	70%
0xccc	125060	125084	125073	3.02651	80%
0xe66	141097	141118	141108	3.17731	90%



TEST #6J: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

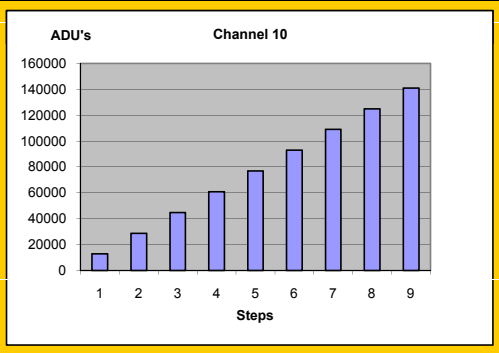
BrdTst6_006 / Channel 9					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12903	12927	12915.1	3.12	10%
0x333	28899	28922	28910.9	3.23894	20%
0x4cc	44899	44920	44910.4	3.1183	30%
0x666	60934	60956	60945.1	3.05161	40%
0x800	76970	76991	76980	3.17034	50%
0x999	92968	92991	92979.9	3.02722	60%
0xb33	109005	109028	109017	3.22845	70%
0xccc	125004	125027	125015	3.17525	80%
0xe66	141042	141064	141053	3.20435	90%



TEST #6K: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

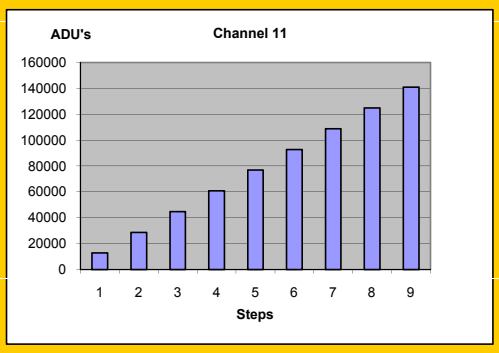
BrdTst6_006 / Channel 10					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12794	12818	12806.3	3.22573	10%
0x333	28799	28824	28812.2	3.23851	20%
0x4cc	44811	44834	44821.9	3.2136	30%
0x666	60854	60878	60866.7	3.23224	40%
0x800	76897	76925	76911.1	3.19869	50%
0x999	92911	92936	92921.4	3.12921	60%
0xb33	108955	108977	108966	3.11826	70%
0xccc	124965	124987	124977	3.11203	80%
0xe66	141012	141035	141023	3.16466	90%



TEST #6L: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

BrdTst6_006 / Channel 11					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12785	12807	12796.2	3.21888	10%
0x333	28773	28796	28783.7	3.20124	20%
0x4cc	44766	44791	44779.4	3.20886	30%
0x666	60795	60818	60806.1	3.10794	40%
0x800	76826	76849	76837.9	2.96538	50%
0x999	92820	92843	92830.7	3.16211	60%
0xb33	108846	108871	108859	3.14257	70%
0xccc	124844	124865	124855	3.24918	80%
0xe66	140873	140895	140884	3.16238	90%



Stage 13. Other Bit Tests. Table 11

Electronic Serial Number	0xDB6FB8		Board Serial Number	18
Firmware Version	0x193		Name Of Person Testing	S. Holm
Ident Register	0x502		Board passed Functional Tests	YES