DES 12 Channel Board - Functional Tests: CCD Acquisition Board Revision 1.0

Stage 1. Preparation of documentation and configuration settings - Table 1.

Board Part Number	21	Board Serial Number	21
Date Of Tests	May 2010	Name Of Person Testing	S. Holm
Suggested Filename To Save	CCDACQ_12Ch_REPORT_BOARD14.xl	Sequence number: Test	

Stage 3. Power plane short test - Table 2.

Supply Name	Short test to ground: Impedance to ground	Test Point	
+1.2VD	55.90	TP43	~50 ohms
+1.8VD	450k	TPB12	> 1K ohm
+2.5VD	18k	TPB11	> 1K ohm
+3.3VD	6k	D13	> 1K ohm
+5VD	18k	D14	> 1K ohm
+5VA	4M	C267	> 1K ohm
-5VA	300k	C270	> 1K ohm
+15VA	550K	C288	> 1K ohm
-15VA	550K	C282	> 1K ohm
-28VA	2.6M	C307	> 1K ohm

Stage 4. Firmware programming tests - Table 3.

JTAG Order	Designator	Device	Load File	Check Sum or User Code
1	U122	XCF08PFS48C PROM	CcdAcqFpgaV41.mcs	0014ef670
2	U114	Spartan3 XC3S2000 FPGA	ccdacqfpgav41.bit	5102801

Stage 5. Power Consumption - Table 4.

Supply Name	Power Supply Consumption: Measured Voltage at test point	Measured Current on power supply	Test Point	
+1.2VD	1.21	N/A	TP43	
+1.8VD	1.81	N/A	TPB12	
+2.5VD	2.50	N/A	TPB11	
+3.3VD	3.29	0.224	D13	
+5VD	5.21	0.153	D14	
+5VA	4.92	0.625	C267	
-5VA	-5.00	0.435	C270	
+15VA	15.09	0.56	C288	
-15VA	-15.08	0.406	C282	
-28VA	-27.94	0.212	C307	
Vref 0+	10.04	N/A	R534	Vsub+ Reference(+10v)
Vref 0-	-2.51	N/A	R525	Vsub - Reference(-2.5v)
Vref Offset	2.50	N/A	R573	ADC Offset Reference(+2.5v)
Vclamp	1.87	N/A	VIA	ADC Clamp Voltage(+1.8v)
ADC Ref.	2.50	N/A	VIA	ADC Reference Voltage(+2.5v)
Vref 1+	2.50	N/A	R537	Vru and Vrl + Reference(+2.5v)
Vref 1-	-10.12	N/A	R535	Vru and Vrl - Reference(-10v)
Vref 2+	5.01	N/A	R563	Vog + Reference(+5v)
Vref 2-	-2.51	N/A	R555	Vog - Reference(-2.5v)
Vref 3+	2.50	N/A	R543	Vdd + Reference(+2.5v)
Vref 3-	-10.05	N/A	R571	Vdd - Reference(-10v)

Power Dissipation:
27.3 Watts

~27 watts +/- 5%

Stage 7. Basic Bus Transactions - **D**igital **Register** Tests - Table 5.

Register name	Put an X on any bit that has an error: 31-24	23-16	15-08	07-00	Function	Test name: Pattern	Walking 0's	Walking 1's
CDS Control			00000000	00000000	16 bit R/W			
Digital Output	00000000	00000000	00000000	00000000	32 bit R/W			
ADC Config.			0000	00000000	12 bit R/W			
Offset DAC			0000	00000000	12 bit R/W			
Bias DAC			0000	00000000	12 bit R/W			
Telemetry Config.				0000	4 bit R/W			
Auxilary Config.				00 00000000	10 bit R/W			
Redirect				0000	4 bit R/W			
Pixel Transfer				00000000	8 bit R/W			
Micro SEQ			00000000	00000000	16 bit R/W			
RAM Buffer			00000000	00000000	16 bit R/W			
LED Control				0000	4 bit R/W			
Control			00000000	00000000	16 bit R/W			
All Register Test	00000000	00000000	00000000	00000000	16 bit R/W	**Passed**	**Passed**	**Passed**

Stage 8. Bias Voltage settings and output enables testing - Table 8

DAC Value	Bias Voltage Test Data 410	2048	3686	50% rms Noise	10-90% Rise Time	Fanout Brd	Slope	Offset
Signal	volts	volts	volts	uV	millisec.			
Vru 0	-13.30	-5.72	1.86	<10	2	BIAS 3	216.09	3284.06
Vru 1	-13.30	-5.72	1.86	<10	2	BIAS 4	216.09	3284.06
Vru 2	-13.30	-5.72	1.86	<10	2	BIAS 5	216.09	3284.06
Vru 3	-13.30	-5.72	1.86	<10	2	BIAS 6	216.09	3284.06
Vru 4	-13.30	-5.72	1.86	<10	2	BIAS 7	216.09	3284.06
Vru 5	-13.30	-5.72	1.86	<10	2	BIAS 8	216.09	3284.06
Vru 6	-13.30	-5.72	1.86	NA	NA	BIAS 9	216.09	3284.06
Vru 7	-13.30	-5.72	1.86	NA	NA	BIAS 10	216.09	3284.06
Vrl 0	-13.30	-5.72	1.86	<10	2	BIAS 11	216.09	3284.06
Vrl 1	-13.30	-5.72	1.86	<10	2	BIAS 12	216.09	3284.06
Vrl 2	-13.30	-5.72	1.86	<10	2	BIAS 13	216.09	3284.06
Vrl 3	-13.30	-5.72	1.86	<10	2	BIAS 14	216.09	3284.06
Vrl 4	-13.30	-5.72	1.86	<10	2	BIAS 15	216.09	3284.06
Vrl 5	-13.30	-5.72	1.86	<10	2	BIAS 16	216.09	3284.06
Vrl 6	-13.30	-5.72	1.86	NA	NA	BIAS 17	216.09	3284.06
Vrl 7	-13.30	-5.72	1.86	NA	NA	BIAS 18	216.09	3284.06
Vog 0	-1.76	1.25	4.26	<10	2	BIAS 19	544.19	1367.77
Vog 1	-1.76	1.25	4.26	<10	2	BIAS 20	544.19	1367.77
Vog 2	-1.76	1.25	4.26	<10	2	BIAS 21	544.19	1367.77
Vog 3	-1.76	1.25	4.26	<10	2	BIAS 22	544.19	1367.77
Vog 4	-1.76	1.25	4.26	<10	2	BIAS 23	544.19	1367.77
Vog 5	-1.76	1.25	4.26	<10	2	BIAS 24	544.19	1367.77
Vog 6	-1.76	1.25	4.26	NA	NA	BIAS 25	544.19	1367.77
Vog 7	-1.76	1.25	4.26	NA	NA	BIAS 26	544.19	1367.77
Vdd 0	-22.06	-9.47	3.11	<10	20	BIAS 27	130.15	3281.00
Vdd 1	-22.05	-9.47	3.11	<10	20	BIAS 28	130.21	3281.06
Vdd 2	-21.99	-9.47	3.11	<10	20	BIAS 29	130.52	3281.39
Vdd 3	-21.98	-9.47	3.11	<10	20	BIAS 30	130.57	3281.45
Vdd 4	-22.04	-9.47	3.11	<10	20	BIAS 21	130.26	3281.11
Vdd 5	-22.04	-9.47	3.11	<10	20	BIAS 32	130.26	3281.11
Vdd 6	-22.04	-9.47	3.11	NA	NA	BIAS 33	130.26	3281.11
Vdd 7	-22.09	-9.47	3.11	NA	NA	BIAS 34	130.00	3280.83

Vru	Slope		Offset
Mean	216.09	Mean	3284.06
Stdev	0	Stdev	4.54747E-13
Average	216.09499	Average	3284.063325
	Dac #	Average voltage	
	0	-15.0	
	4095	3.8	

Vrl	Slope		Offset
Mean	216.09	Mean	3284.06
Stdev	0	Stdev	4.54747E-13
Average	216.09499	Average	3284.063325
	Dac #	Average voltage	
	0	-15.2	
	4095	3.8	

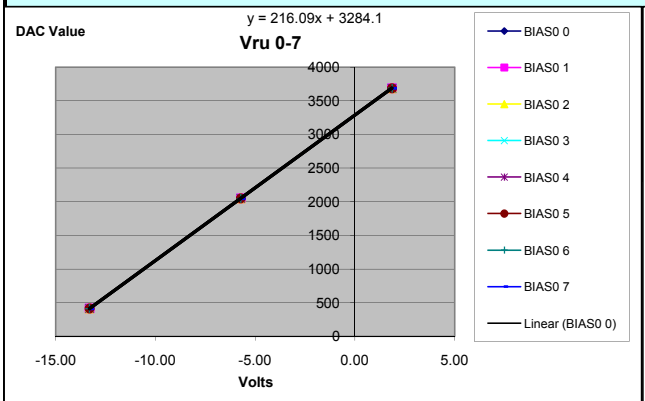
Vog	Slope		Offset
Mean	544.19	Mean	1367.77
Stdev	0	Stdev	2.27374E-13
Average	544.18605	Average	1367.767442
	Dac #	Average voltage	
	0	-2.5	
	4095	5.0	

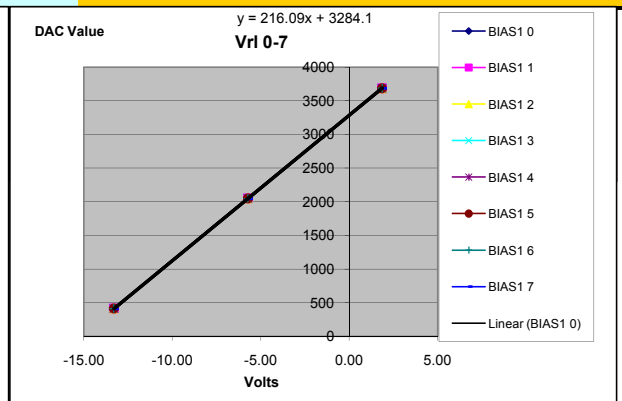
Vdd	Slope		Offset
Mean	130.28	Mean	3281.13
Stdev	0.1736395	Stdev	0.187348324
Average	130.27802	Average	3281.133759
	Dac #	Average voltage	
	0	-25.2	
	4095	6.3	

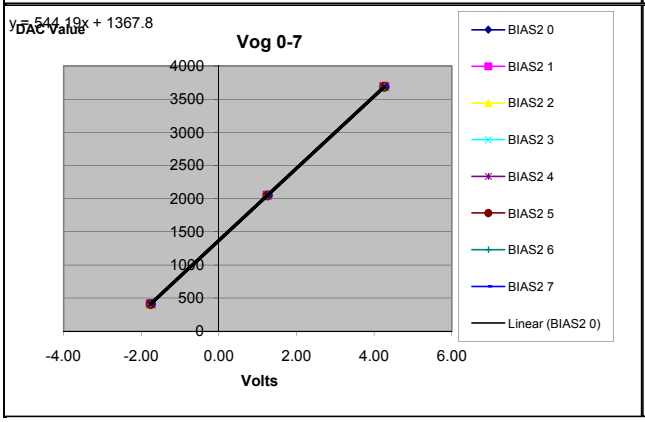
Notes and Observations

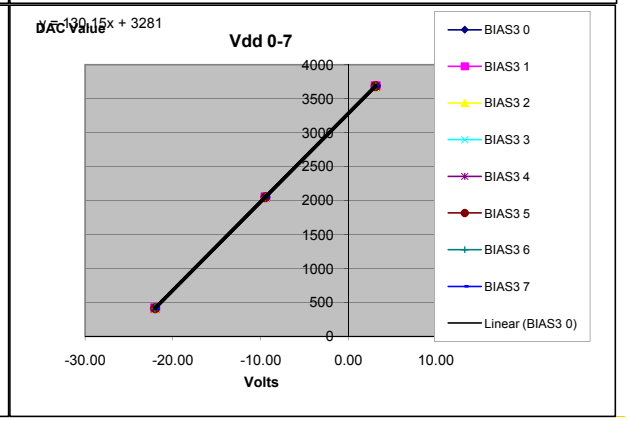
Checked for oscillations using a Agilent Oscilloscpe on AC.OK

average min & max voltages
(dac# -offset)/slope=voltage









Stage 8B. Telemetry System Tests - Table 7 (Bias Telemetry Tests)

DAC Value	410	3686	Bias Signals Set Volts		Resolved Values for Telemetry Channel	
	Telemetry Return Values					
Signal	10%	90%	10%	90%	Slope	Offset
Vru 0	-1764	421	-13.30	1.86	144.1293	152.92
Vru 1	-1759	421	-13.30	1.86	143.7995	153.53
Vru 2	-1760	421	-13.30	1.86	143.8654	153.41
Vru 3	-1762	421	-13.30	1.86	143.9974	153.16
Vru 4	-1762	421	-13.30	1.86	143.9974	153.16
Vru 5	-1761	421	-13.30	1.86	143.9314	153.29
Vru 6	-1760	421	-13.30	1.86	143.8654	153.41
Vru 7	-1762	420	-13.30	1.86	143.9314	152.29
Vrl 0	-1775	419	-13.30	1.86	144.7230	149.82
Vrl 1	-1778	420	-13.30	1.86	144.9868	150.32
Vrl 2	-1782	419	-13.30	1.86	145.1847	148.96
Vrl 3	-1784	420	-13.30	1.86	145.3826	149.59
Vrl 4	-1783	420	-13.30	1.86	145.3166	149.71
Vrl 5	-1783	420	-13.30	1.86	145.3166	149.71
Vrl 6	-1785	420	-13.30	1.86	145.4485	149.47
Vrl 7	-1783	420	-13.30	1.86	145.3166	149.71
Vog 0	-364	868	-1.76	4.26	204.6512	-3.81
Vog 1	-363	869	-1.76	4.26	204.6512	-2.81
Vog 2	-364	869	-1.76	4.26	204.8173	-3.52
Vog 3	-363	869	-1.76	4.26	204.6512	-2.81
Vog 4	-364	869	-1.76	4.26	204.8173	-3.52
Vog 5	-364	869	-1.76	4.26	204.8173	-3.52
Vog 6	-364	869	-1.76	4.26	204.8173	-3.52
Vog 7	-364	869	-1.76	4.26	204.8173	-3.52
Vdd 0	-1712	573	-22.06	3.11	90.7827	290.67
Vdd 1	-1712	573	-22.05	3.11	90.8188	290.55
Vdd 2	-1702	572	-21.99	3.11	90.5976	290.24
Vdd 3	-1700	572	-21.98	3.11	90.5540	290.38
Vdd 4	-1709	573	-22.04	3.11	90.7356	290.81
Vdd 5	-1700	573	-22.04	3.11	90.3777	291.93
Vdd 6	-1702	572	-22.04	3.11	90.4175	290.80
Vdd 7	-1706	574	-22.09	3.11	90.4762	292.62

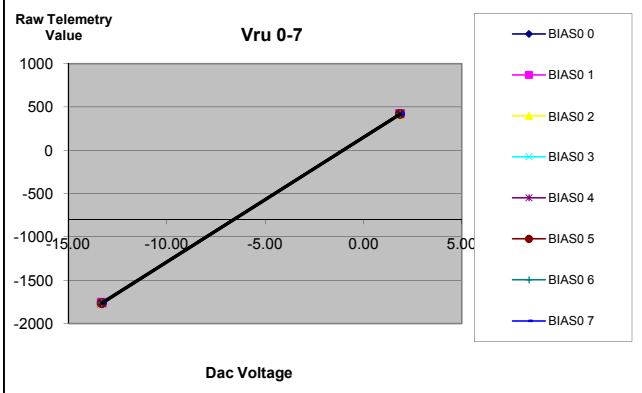
AVERAGE

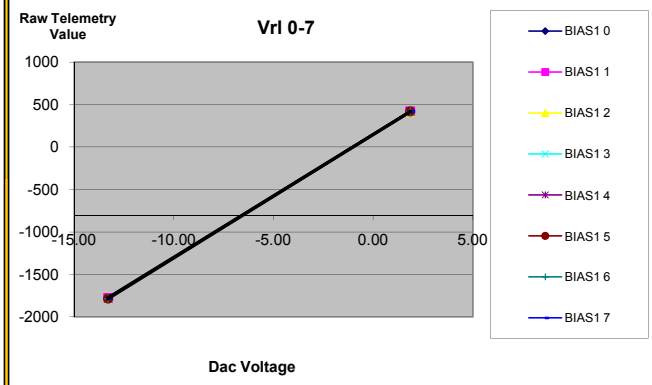
Vru	Slope		Offset
Mean	143.94	Mean	153.15
Stdev	0.0958027	Stdev	0.3705316

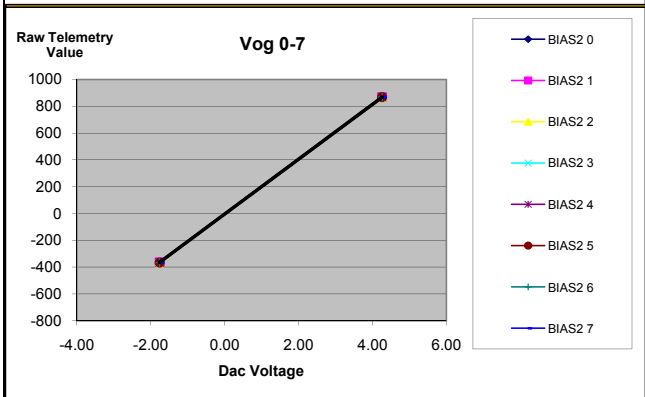
Vrl	Slope		Offset
Mean	145.21	Mean	149.66
Stdev	0.2259596	Stdev	0.3555629

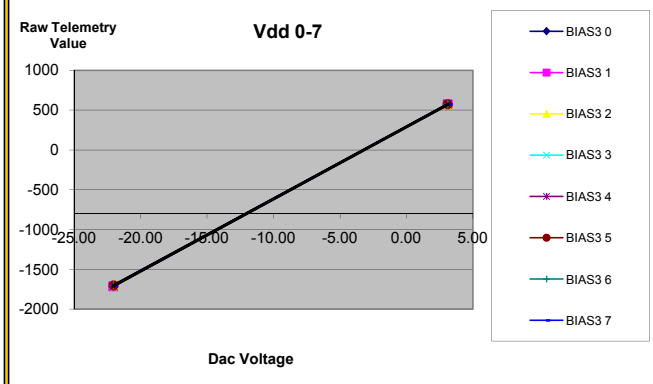
Vog	Slope		Offset
Mean	204.75	Mean	-3.38
Stdev	0.0804191	Stdev	0.3408383

Vdd	Slope		Offset
Mean	90.60	Mean	291.00
Stdev	0.1579445	Stdev	0.7767197









Stage 8C. Bias Voltage output enables testing - Table 8

Place a line through Bias Voltage name if enable/disable switch works

Vru 0	Vru 1	Vru 2	Vru 3	Vru 4	Vru 5
Vrl 0	Vrl 1	Vrl 2	Vrl 3	Vrl 4	Vrl 5
Vog 0	Vog 1	Vog 2	Vog 3	Vog 4	Vog 5
Vdd 0	Vdd 1	Vdd 2	Vdd 3	Vdd 4	Vdd 5

Stage 9. Vsub and Heater Control testing - Table 9

DAC Value	Vsub Measured Voltage Test Data 10%	50%	90%
Signal	volts	volts	volts
Vsub - rate	-1.26	3.76	8.78
Vsub - Limit	-1.27	3.75	8.79
Vsub0	0.00	3.75	8.75
	Vsub Enable Bit - pass		

DAC Value	Telemetery Readback Test Data 10%	50%	90%
Signal	dec	dec	dec
Vbias 0	155	271	446
Vbias 1	-28	696	1419
RTD1	219	NA	NA
RTD2	247	NA	NA
RTD3	275	NA	NA
RTD4	301	NA	NA
RTD5	324	NA	NA
RTD6	350	NA	NA
Reference 4096	836	NA	NA
eference buffere	836	NA	NA

Stage 10. Video Offset DAC Tests - Table 10.

	DAC Value 410				DAC Value 2048				DAC Value 3686			
ADC	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU
0	0.250	NA	NA	17002	1.250		NA	81090	2.250	NA	500ms	145170
1	0.250	NA	NA	16971	1.250		NA	80988	2.250	NA	500ms	145013
2	0.250	NA	NA	17062	1.250		NA	81055	2.250	NA	500ms	145042
3	0.250	NA	NA	17057	1.250		NA	81074	2.250	NA	500ms	145087
4	0.250	NA	NA	17089	1.250		NA	81148	2.250	NA	500ms	145202
5	0.250	NA	NA	17124	1.250		NA	81122	2.250	NA	500ms	145136
6	0.250	NA	NA	16997	1.250		NA	81011	2.250	NA	500ms	145024
7	0.250	NA	NA	17021	1.250		NA	81080	2.250	NA	500ms	145146
8	0.250	NA	NA	17062	1.250		NA	81083	2.250	NA	500ms	145101
9	0.250	NA	NA	17074	1.250		NA	81107	2.250	NA	500ms	145135
10	0.250	NA	NA	16888	1.250		NA	81004	2.250	NA	500ms	145118
11	0.250	NA	NA	16933	1.250		NA	81068	2.250	NA	500ms	145204

ADC	DC Volts		Data Set		
Channel	Slope	Offset	410	2048	3686
0	1638.000	0.500	0.250	1.250	2.250
1	1638.000	0.500	0.250	1.250	2.250
2	1638.000	0.500	0.250	1.250	2.250
3	1638.000	0.500	0.250	1.250	2.250
4	1638.000	0.500	0.250	1.250	2.250
5	1638.000	0.500	0.250	1.250	2.250
6	1638.000	0.500	0.250	1.250	2.250
7	1638.000	0.500	0.250	1.250	2.250
8	1638.000	0.500	0.250	1.250	2.250
9	1638.000	0.500	0.250	1.250	2.250
10	1638.000	0.500	0.250	1.250	2.250
11	1638.000	0.500	0.250	1.250	2.250

(dac# -offset)/slope=Voltage

ADC	ADU's		Data Set		
Channel	Slope	Offset	410	2048	3686
0	0.026	-24.61	17002	81090	145170
1	0.026	-24.17	16971	80988	145013
2	0.026	-26.77	17062	81055	145042
3	0.026	-26.47	17057	81074	145087
4	0.026	-27.01	17089	81148	145202
5	0.026	-28.16	17124	81122	145136
6	0.026	-24.93	16997	81011	145024
7	0.026	-25.18	17021	81080	145146
8	0.026	-26.56	17062	81083	145101
9	0.026	-26.80	17074	81107	145135
10	0.026	-21.46	16888	81004	145118
11	0.026	-22.46	16933	81068	145204

(dac# -offset)/slope=ADU

Notes and Observations

Checked for oscillations using a Agilent Oscilloscope on AC. OK

Stage 11. CDS Control Functions and Video Channel Performanc

TEST #1: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit is held static. The purpose of this test is to verify the correct operation of the ADC devices and measure the noise of the Offset voltage generators, ADC buffer amplifiers and ADC devices

Noise Test 1

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	81082	81098	81090.2	2.31131
CH 1	80984	80999	80990.8	2.34108
CH 2	81048	81067	81056.3	2.32547
CH 3	81067	81084	81075.8	2.37692
CH 4	81143	81160	81150.7	2.26277
CH 5	81118	81138	81129.6	2.39706
CH 6	81006	81023	81015.2	2.36134
CH 7	81076	81096	81084.5	2.4511
CH 8	81076	81093	81084.2	2.28446
CH 9	81100	81117	81107.8	2.28074
CH 10	80997	81015	81006.2	2.35852
CH 11	81060	81079	81070.5	2.39798

TEST #2: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the invert/non-invert and the DC Restore switches are held static.

Noise Test 2

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76657	76676	76665.8	2.76715
CH 1	76657	76678	76668.1	2.92566
CH 2	76504	76525	76514.4	2.89271
CH 3	76818	76839	76827.6	2.8344
CH 4	76403	76423	76413.1	2.7965
CH 5	77018	77038	77026.8	2.85822
CH 6	76946	76968	76956.2	2.90342
CH 7	76825	76844	76835.3	2.60004
CH 8	76618	76639	76629.7	2.77086
CH 9	76858	76881	76869.7	2.85587
CH 10	76354	76374	76364.8	2.87778
CH 11	76809	76830	76820.2	2.72023

TEST #3: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the DC Restore switch is held static.

Noise Test 3

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76659	76681	76671	2.95528
CH 1	76661	76682	76671.8	3.09036
CH 2	76504	76525	76514.1	3.12395
CH 3	76811	76835	76822.9	3.0594
CH 4	76396	76418	76407.7	3.05779
CH 5	77011	77037	77024.9	3.08287
CH 6	76945	76966	76955.8	3.11143
CH 7	76826	76849	76837.8	3.00206
CH 8	76609	76631	76620.5	3.03934
CH 9	76860	76881	76870.6	3.07841
CH 10	76344	76367	76354.5	3.15976
CH 11	76803	76828	76816.5	2.97822

TEST #4: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition.

Noise Test 4

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76654	76675	76663	3.09748
CH 1	76664	76688	76675.2	3.08416
CH 2	76507	76532	76519	3.25398
CH 3	76812	76834	76822.7	3.10757
CH 4	76434	76456	76445.5	3.16899
CH 5	77002	77025	77013.2	3.07936
CH 6	76952	76974	76962.9	3.09182
CH 7	76799	76823	76809.4	3.18226
CH 8	76649	76672	76661.2	3.03346
CH 9	76779	76802	76790.8	3.15371
CH 10	76360	76383	76372	3.05773
CH 11	76768	76792	76780.1	3.26978

TEST #5: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the circuitry set to high GAIN.

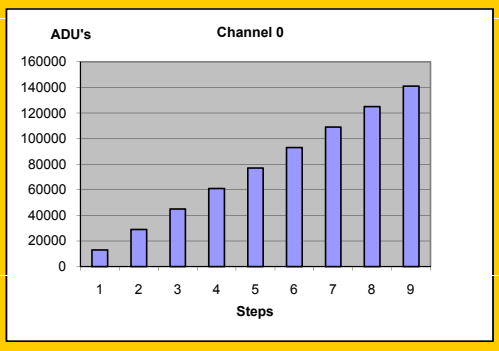
Noise Test 5

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76656	76686	76671.9	3.62955
CH 1	76672	76701	76685.7	3.85997
CH 2	76521	76549	76535.4	3.67959
CH 3	76814	76841	76828.1	3.70087
CH 4	76437	76461	76449.6	3.54551
CH 5	76997	77024	77011.3	3.63191
CH 6	76950	76978	76964.6	3.65318
CH 7	76797	76826	76811.4	3.70956
CH 8	76697	76721	76708.8	3.52305
CH 9	76777	76808	76790.8	3.76417
CH 10	76418	76444	76430	3.70657
CH 11	76766	76793	76779.9	3.73537

TEST #6A: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

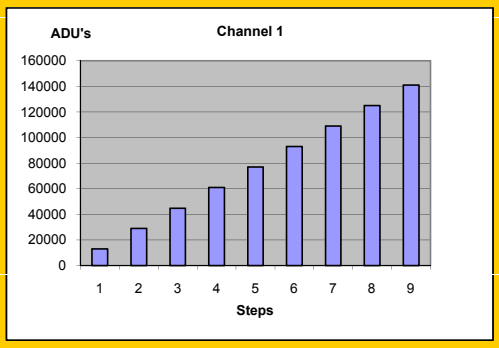
BrdTst6_006 / Channel 0					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12879	12900	12889.6	3.17205	10%
0x333	28883	28906	28893.9	3.12651	20%
0x4cc	44879	44905	44891.1	3.1915	30%
0x666	60922	60945	60933.9	3.01532	40%
0x800	76961	76984	76973.3	3.13609	50%
0x999	92963	92987	92974.8	3.05955	60%
0xb33	109006	109029	109018	3.14727	70%
0xccc	125007	125030	125019	3.17621	80%
0xe66	141050	141074	141063	3.07485	90%



TEST #6B: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

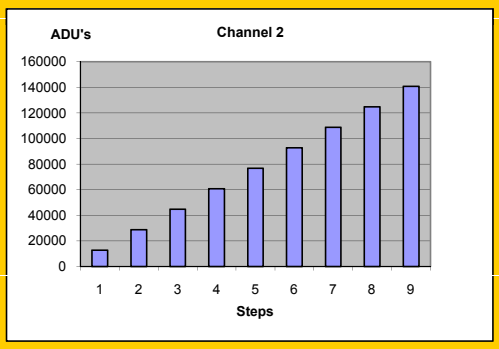
BrdTst6_006 / Channel 1					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12895	12916	12905.4	3.20377	10%
0x333	28879	28903	28891.7	3.2107	20%
0x4cc	44860	44883	44871.1	3.12922	30%
0x666	60886	60909	60897.2	3.11853	40%
0x800	76910	76933	76921.7	3.22631	50%
0x999	92898	92921	92908.7	3.21805	60%
0xb33	108921	108945	108934	3.22598	70%
0xccc	124903	124928	124916	3.19464	80%
0xe66	140930	140954	140942	3.23001	90%



TEST #6C: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

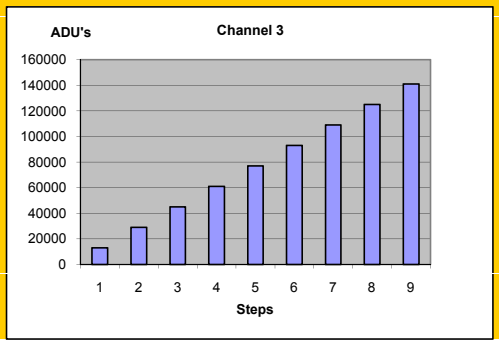
BrdTst6_006 / Channel 2					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12807	12832	12820.4	3.10637	10%
0x333	28786	28809	28798.6	3.14245	20%
0x4cc	44764	44788	44776	3.14808	30%
0x666	60782	60806	60793.6	3.10536	40%
0x800	76797	76819	76807.6	3.12941	50%
0x999	92773	92795	92785.4	3.11834	60%
0xb33	108793	108816	108805	3.3009	70%
0xccc	124771	124795	124784	3.19944	80%
0xe66	140792	140814	140802	3.07628	90%



TEST #6D: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

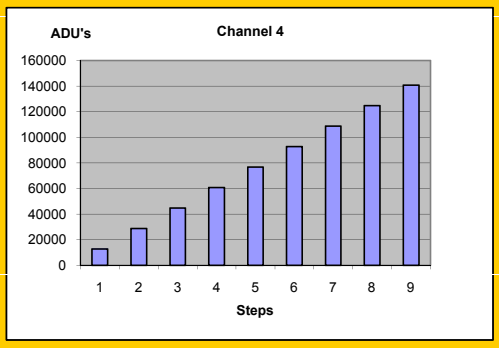
BrdTst6_006 / Channel 3					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13034	13059	13046.7	3.21994	10%
0x333	29020	29043	29030.8	3.13793	20%
0x4cc	45002	45025	45012.6	3.09729	30%
0x666	61026	61049	61037.6	3.15224	40%
0x800	77046	77068	77056.4	3.16398	50%
0x999	93027	93052	93038.6	3.20573	60%
0xb33	109053	109075	109063	3.18577	70%
0xccc	125036	125058	125046	3.06329	80%
0xe66	141061	141083	141072	3.28022	90%



TEST #6E: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

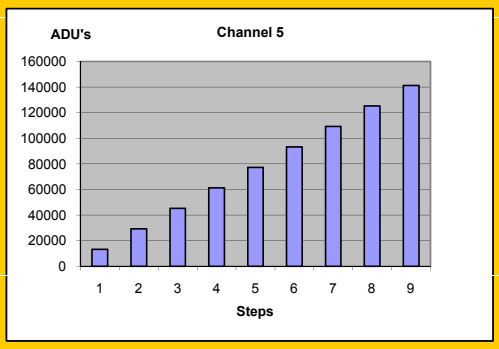
BrdTst6_006 / Channel 4					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12686	12709	12697.4	3.17751	10%
0x333	28680	28701	28691.1	3.04489	20%
0x4cc	44675	44697	44685.6	3.16125	30%
0x666	60706	60729	60718.2	3.17121	40%
0x800	76736	76760	76748	3.13706	50%
0x999	92730	92753	92740.8	3.19492	60%
0xb33	108761	108786	108775	3.08943	70%
0xccc	124761	124782	124772	3.02814	80%
0xe66	140795	140818	140805	3.11089	90%



TEST #6F: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

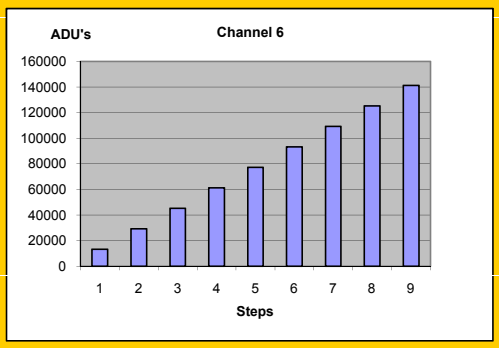
BrdTst6_006 / Channel 5					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13252	13272	13261.4	3.19219	10%
0x333	29234	29254	29244.2	3.23485	20%
0x4cc	45210	45235	45222	3.26903	30%
0x666	61231	61256	61243.4	3.25315	40%
0x800	77254	77278	77266.1	3.03254	50%
0x999	93240	93261	93249.7	3.14351	60%
0xb33	109260	109286	109273	3.19907	70%
0xccc	125240	125264	125252	3.15306	80%
0xe66	141263	141285	141275	3.25825	90%



TEST #6G: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

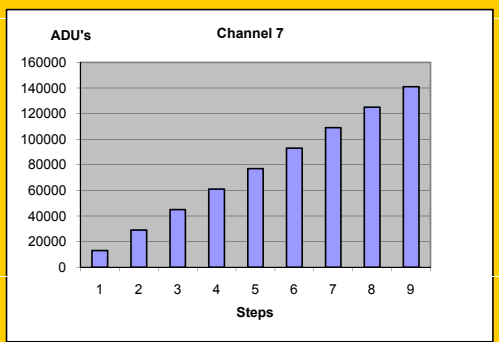
BrdTst6_006 / Channel 6					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13177	13200	13188.3	3.15774	10%
0x333	29158	29183	29171.2	3.19056	20%
0x4cc	45142	45163	45152.9	3.02563	30%
0x666	61164	61187	61175.1	3.10564	40%
0x800	77181	77204	77193.5	3.12841	50%
0x999	93166	93190	93178.4	3.16405	60%
0xb33	109189	109212	109201	3.19283	70%
0xccc	125175	125198	125186	3.27726	80%
0xe66	141196	141221	141208	3.2184	90%



TEST #6H: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

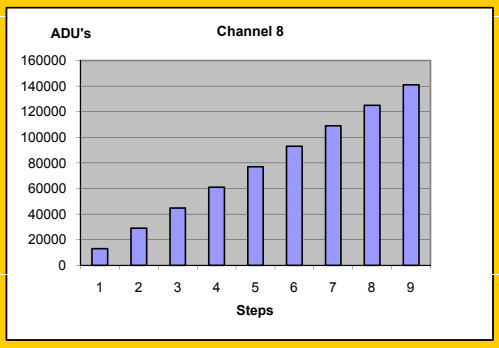
BrdTst6_006 / Channel 7					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12971	12994	12982.5	3.18658	10%
0x333	28966	28988	28977.3	3.11762	20%
0x4cc	44961	44983	44972.2	3.21534	30%
0x666	60994	61017	61005.7	3.18591	40%
0x800	77027	77050	77038.9	3.19936	50%
0x999	93024	93045	93034.7	3.23146	60%
0xb33	109060	109082	109071	3.1547	70%
0xccc	125054	125079	125066	3.26694	80%
0xe66	141090	141115	141103	3.27979	90%



TEST #6I: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

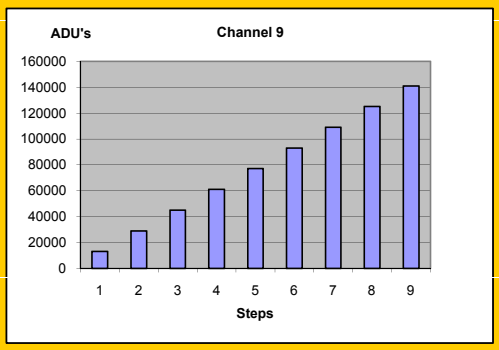
BrdTst6_006 / Channel 8					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12899	12921	12910.4	3.11789	10%
0x333	28884	28907	28895.7	3.16051	20%
0x4cc	44867	44889	44877.1	3.14145	30%
0x666	60890	60913	60901.3	2.97313	40%
0x800	76915	76937	76925.6	3.0629	50%
0x999	92899	92921	92910.8	3.19809	60%
0xb33	108924	108946	108935	3.11275	70%
0xccc	124906	124930	124919	3.11689	80%
0xe66	140933	140955	140945	3.11148	90%



TEST #6J: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

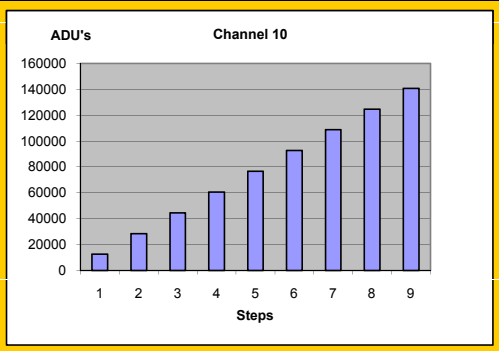
BrdTst6_006 / Channel 9					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13018	13040	13029	3.20244	10%
0x333	29006	29028	29016.8	3.17781	20%
0x4cc	44992	45016	45003.7	3.18497	30%
0x666	61020	61040	61030.4	3.12182	40%
0x800	77040	77063	77051.2	3.23324	50%
0x999	93028	93052	93039.3	3.23695	60%
0xb33	109058	109080	109070	3.14751	70%
0xccc	125046	125069	125058	3.2006	80%
0xe66	141077	141098	141087	3.18159	90%



TEST #6K: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

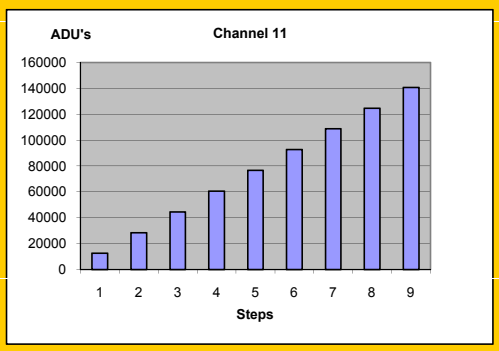
BrdTst6_006 / Channel 10					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12521	12543	12531	3.0987	10%
0x333	28529	28550	28539.9	3.21218	20%
0x4cc	44537	44560	44549	3.14326	30%
0x666	60587	60609	60598	3.05307	40%
0x800	76633	76654	76643.8	2.97154	50%
0x999	92641	92666	92652.7	3.18094	60%
0xb33	108689	108714	108702	3.16609	70%
0xccc	124703	124724	124714	3.19314	80%
0xe66	140753	140775	140764	3.24365	90%



TEST #6L: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

BrdTst6_006 / Channel 11					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12521	12543	12531	3.0987	10%
0x333	28529	28550	28539.9	3.21218	20%
0x4cc	44537	44560	44549	3.14326	30%
0x666	60587	60609	60598	3.05307	40%
0x800	76633	76654	76643.8	2.97154	50%
0x999	92641	92666	92652.7	3.18094	60%
0xb33	108689	108714	108702	3.16609	70%
0xccc	124703	124724	124714	3.19314	80%
0xe66	140753	140775	140764	3.24365	90%



Stage 13. Other Bit Tests. Table 11

Electronic Serial Number	0xDB6FC1		Board Serial Number	21
Firmware Version	0x193		Name Of Person Testing	S. Holm
Ident Register	0x502		Board passed Functional Tests	YES