DES 12 Channel Board - Functional Tests: CCD Acquisition Board Revision 1.0

Stage 1. Preparation of documentation and configuration settings - Table 1.

Board Part Number	4		Board Serial Number	0xDB8EE6
Date Of Tests	August 2010		Name Of Person Testing	S. Holm
Suggested Filename To Save	CCDACQ_12Ch_REPORT_BOARD12.xl		Sequence number: Test	

Stage 3. Power plane short test - Table 2.

Supply Name	Short test to ground: Impedance to ground	Test Point	
+1.2VD	81.00	TP43	~50 ohms
+1.8VD	2.4M	TPB12	> 1K ohm
+2.5VD	15K	TPB11	> 1K ohm
+3.3VD	24k	D13	> 1K ohm
+5VD	500k	D14	> 1K ohm
+5VA	2M	C267	> 1K ohm
-5VA	700K	C270	> 1K ohm
+15VA	400K	C288	> 1K ohm
-15VA	400K	C282	> 1K ohm
-28VA	700K	C307	> 1K ohm

Stage 4. Firmware programming tests - Table 3.

JTAG Order	Designator	Device	Load File	Check Sum or User Code
1	U122	XCF08PFS48C PROM	CcdAcqFpgaV41.mcs	0014ef670
2	U114	Spartan3 XC3S2000 FPGA	ccdacqfpgav41.bit	5102801

Stage 5. Power Consumption - Table 4.

Supply Name	Power Supply Consumption: Measured Voltage at test point	Measured Current on power supply	Test Point	
+1.2VD	1.20	N/A	TP43	
+1.8VD	1.80	N/A	TPB12	
+2.5VD	2.51	N/A	TPB11	
+3.3VD	3.29	0.188	D13	
+5VD	5.20	0.15	D14	
+5VA	4.92	0.556	C267	
-5VA	-5.00	0.434	C270	
+15VA	14.96	0.56	C288	
-15VA	-15.00	0.41	C282	
-28VA	-27.90	0.197	C307	
Vref 0+	10.04	N/A	R534	Vsub+ Reference(+10v)
Vref 0-	-2.49	N/A	R525	Vsub - Reference(-2.5v)
Vref Offset	2.50	N/A	R573	ADC Offset Reference(+2.5v)
Vclamp	1.88	N/A	VIA	ADC Clamp Voltage(+1.8v)
ADC Ref.	2.50	N/A	VIA	ADC Reference Voltage(+2.5v)
Vref 1+	2.50	N/A	R537	Vru and Vrl + Reference(+2.5v)
Vref 1-	-9.99	N/A	R535	Vru and Vrl - Reference(-10v)
Vref 2+	5.00	N/A	R563	Vog + Reference(+5v)
Vref 2-	-2.49	N/A	R555	Vog - Reference(-2.5v)
Vref 3+	2.50	N/A	R543	Vdd + Reference(+2.5v)
Vref 3-	-10.01	N/A	R571	Vdd - Reference(-10v)

Power Dissipation:
26.3 Watts

~27 watts +/- 5%

Stage 7. Basic Bus Transactions - **D**igital **Register** Tests - Table 5.

Register name	Put an X on any bit that has an error: 31-24	23-16	15-08	07-00	Function	Test name: Pattern	Walking 0's	Walking 1's
CDS Control			00000000	00000000	16 bit R/W			
Digital Output	00000000	00000000	00000000	00000000	32 bit R/W			
ADC Config.			0000	00000000	12 bit R/W			
Offset DAC			0000	00000000	12 bit R/W			
Bias DAC			0000	00000000	12 bit R/W			
Telemetry Config.				0000	4 bit R/W			
Auxilary Config.			00	00000000	10 bit R/W			
Redirect				0000	4 bit R/W			
Pixel Transfer				00000000	8 bit R/W			
Micro SEQ			00000000	00000000	16 bit R/W			
RAM Buffer			00000000	00000000	16 bit R/W			
LED Control				0000	4 bit R/W			
Control			00000000	00000000	16 bit R/W			
All Register Test	00000000	00000000	00000000	00000000	16 bit R/W	**Passed**	**Passed**	**Passed**

Stage 8. Bias Voltage settings and output enables testing - Table 8

DAC Value	Bias Voltage Test Data 410	2048	3686	50% rms Noise	10-90% Rise Time	Fanout Brd	Slope	Offset
Signal	volts	volts	volts	uV	millisec.			
Vru 0	-13.10	-5.61	1.87	<10	1	BIAS 3	218.84	3276.41
Vru 1	-13.10	-5.61	1.87	<10	1	BIAS 4	218.84	3276.41
Vru 2	-13.11	-5.61	1.87	<10	1	BIAS 5	218.69	3276.32
Vru 3	-13.08	-5.61	1.87	<10	1	BIAS 6	219.13	3276.59
Vru 4	-13.08	-5.61	1.87	<10	1	BIAS 7	219.13	3276.59
Vru 5	-13.12	-5.61	1.87	<10	1	BIAS 8	218.55	3276.23
Vru 6	-13.10	-5.61	1.87	NA	NA	BIAS 9	218.84	3276.41
Vru 7	-13.10	-5.61	1.87	NA	NA	BIAS 10	218.84	3276.41
Vrl 0	-13.10	-5.61	1.87	<10	1	BIAS 11	218.84	3276.41
Vrl 1	-13.10	-5.61	1.87	<10	1	BIAS 12	218.84	3276.41
Vrl 2	-13.10	-5.61	1.87	<10	1	BIAS 13	218.84	3276.41
Vrl 3	-13.09	-5.61	1.87	<10	1	BIAS 14	218.98	3276.50
Vrl 4	-13.12	-5.61	1.87	<10	1	BIAS 15	218.55	3276.23
Vrl 5	-13.11	-5.61	1.87	<10	1	BIAS 16	218.69	3276.32
Vrl 6	-13.11	-5.61	1.87	NA	NA	BIAS 17	218.69	3276.32
Vrl 7	-13.10	-5.61	1.87	NA	NA	BIAS 18	218.84	3276.41
Vog 0	-1.74	1.25	4.25	<10	1	BIAS 19	546.91	1362.54
Vog 1	-1.74	1.25	4.25	<10	1	BIAS 20	546.91	1362.54
Vog 2	-1.74	1.25	4.25	<10	1	BIAS 21	546.91	1362.54
Vog 3	-1.74	1.25	4.25	<10	1	BIAS 22	546.91	1362.54
Vog 4	-1.74	1.25	4.25	<10	1	BIAS 23	546.91	1362.54
Vog 5	-1.74	1.25	4.25	<10	1	BIAS 24	546.91	1362.54
Vog 6	-1.74	1.25	4.25	NA	NA	BIAS 25	546.91	1362.54
Vog 7	-1.74	1.25	4.25	NA	NA	BIAS 26	546.91	1362.54
Vdd 0	-21.96	-9.42	3.12	<10	20	BIAS 27	130.62	3278.46
Vdd 1	-21.97	-9.43	3.12	<10	20	BIAS 28	130.57	3278.84
Vdd 2	-21.98	-9.43	3.12	<10	20	BIAS 29	130.52	3278.78
Vdd 3	-21.90	-9.40	3.12	<10	20	BIAS 30	130.94	3277.92
Vdd 4	-21.94	-9.41	3.12	<10	20	BIAS 21	130.73	3278.13
Vdd 5	-21.98	-9.41	3.12	<10	20	BIAS 32	130.52	3277.91
Vdd 6	-21.94	-9.43	3.12	NA	NA	BIAS 33	130.73	3279.00
Vdd 7	-21.97	-9.43	3.12	NA	NA	BIAS 34	130.57	3278.84

Vru	Slope		Offset
Mean	218.86	Mean	3276.42
Stdev	0.185568	Stdev	0.115995903
Average	218.85603	Average	3276.419873
	Dac #	Average voltage	
	0	-14.0	
	4095	3.7	

Vrl	Slope		Offset
Mean	218.78	Mean	3276.37
Stdev	0.1252686	Stdev	0.078512494
Average	218.78286	Average	3276.374222
	Dac #	Average voltage	
	0	-15.0	
	4095	3.7	

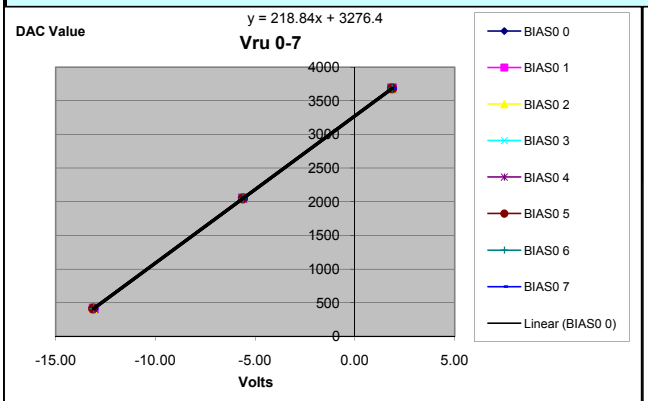
Vog	Slope		Offset
Mean	546.91	Mean	1362.54
Stdev	0	Stdev	0
Average	546.91101	Average	1362.538199
	Dac #	Average voltage	
	0	-2.5	
	4095	5.0	

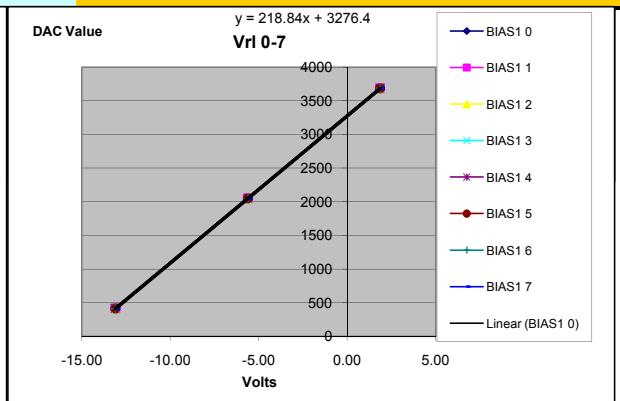
Vdd	Slope		Offset
Mean	130.65	Mean	3278.49
Stdev	0.1329738	Stdev	0.415749158
Average	130.64816	Average	3278.486468
	Dac #	Average voltage	
	0	-25.1	
	4095	6.3	

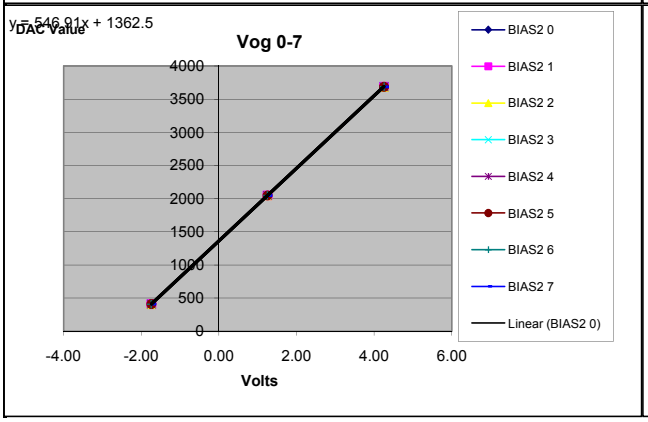
Notes and Observations

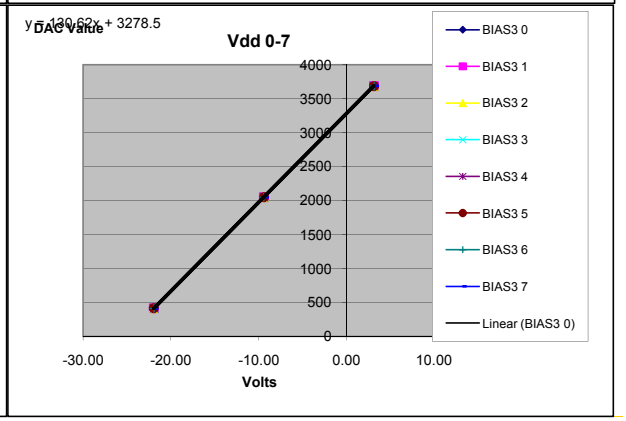
Checked for oscillations using a Agilent Oscilloscpe on AC.**OK**

average min & max voltages
(dac# -offset)/slope=voltage









Stage 8B. Telemetry System Tests - Table 7 (Bias Telemetry Tests)

DAC Value: 410 / 3686

Signal	Telemetry Return Values 10%	90%	Bias Signals Set Volts 10%	90%	Resolved Values for Telemetry Channel Slope	Offset
Vru 0	-1736	423	-13.10	1.87	144.2218	153.31
Vru 1	-1737	423	-13.10	1.87	144.2886	153.18
Vru 2	-1738	423	-13.11	1.87	144.2590	153.24
Vru 3	-1734	423	-13.08	1.87	144.2809	153.19
Vru 4	-1740	424	-13.08	1.87	144.7492	153.32
Vru 5	-1738	423	-13.12	1.87	144.1628	153.42
Vru 6	-1740	423	-13.10	1.87	144.4890	152.81
Vru 7	-1736	423	-13.10	1.87	144.2218	153.31
Vrl 0	-1724	424	-13.10	1.87	143.4870	155.68
Vrl 1	-1726	424	-13.10	1.87	143.6206	155.43
Vrl 2	-1726	424	-13.10	1.87	143.6206	155.43
Vrl 3	-1725	424	-13.09	1.87	143.6497	155.38
Vrl 4	-1723	424	-13.12	1.87	143.2288	156.16
Vrl 5	-1727	424	-13.11	1.87	143.5915	155.48
Vrl 6	-1726	425	-13.11	1.87	143.5915	156.48
Vrl 7	-1728	424	-13.10	1.87	143.7542	155.18
Vog 0	-361	867	-1.74	4.25	205.0083	-4.29
Vog 1	-361	867	-1.74	4.25	205.0083	-4.29
Vog 2	-361	867	-1.74	4.25	205.0083	-4.29
Vog 3	-361	867	-1.74	4.25	205.0083	-4.29
Vog 4	-361	867	-1.74	4.25	205.0083	-4.29
Vog 5	-361	867	-1.74	4.25	205.0083	-4.29
Vog 6	-361	867	-1.74	4.25	205.0083	-4.29
Vog 7	-361	867	-1.74	4.25	205.0083	-4.29
Vdd 0	-1699	574	-21.96	3.12	90.6300	291.23
Vdd 1	-1700	574	-21.97	3.12	90.6337	291.22
Vdd 2	-1700	574	-21.98	3.12	90.5976	291.34
Vdd 3	-1689	573	-21.90	3.12	90.4077	290.93
Vdd 4	-1693	574	-21.94	3.12	90.4629	291.76
Vdd 5	-1698	574	-21.98	3.12	90.5179	291.58
Vdd 6	-1697	573	-21.94	3.12	90.5826	290.38
Vdd 7	-1694	574	-21.97	3.12	90.3946	291.97

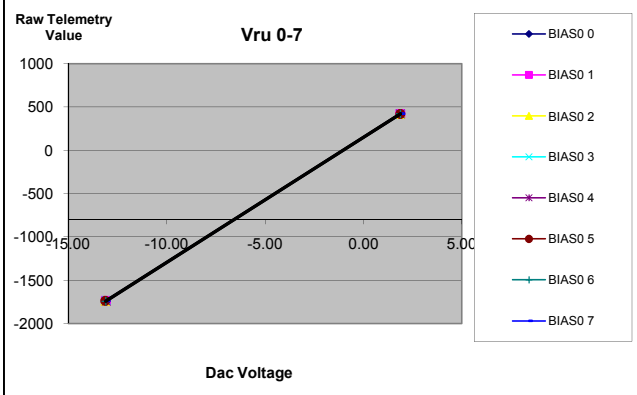
AVERAGE

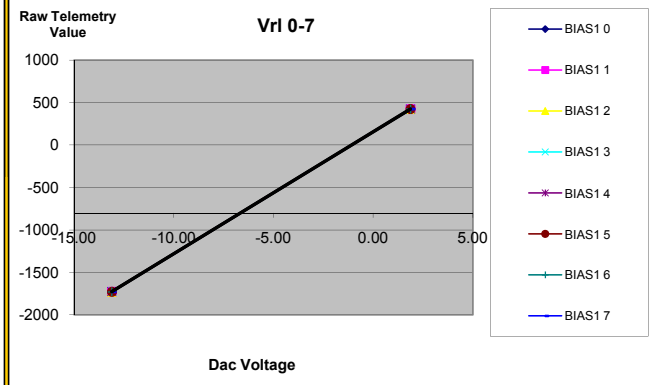
Vru	Slope		Offset
Mean	144.33	Mean	153.22
Stdev	0.1807579	Stdev	0.1720458

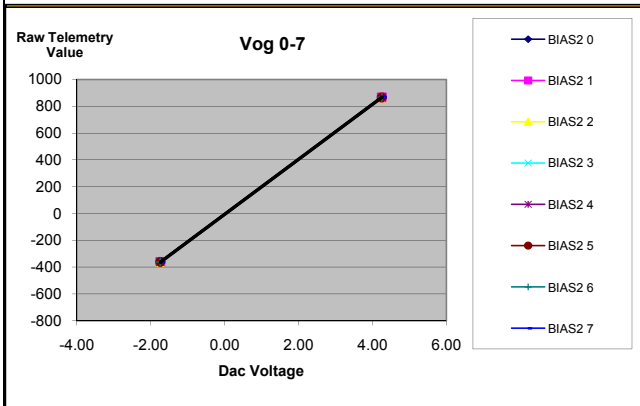
Vrl	Slope		Offset
Mean	143.57	Mean	155.65
Stdev	0.145593	Stdev	0.415356

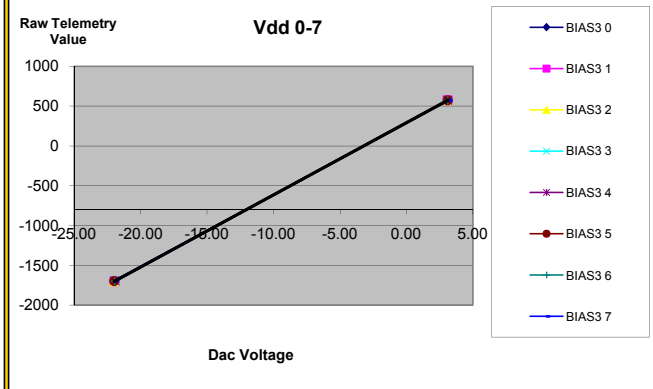
Vog	Slope		Offset
Mean	205.01	Mean	-4.29
Stdev	2.842E-14	Stdev	0

Vdd	Slope		Offset
Mean	90.53	Mean	291.30
Stdev	0.0908455	Stdev	0.4647472









Stage 8C. Bias Voltage output enables testing - Table 8

Place a line through Bias Voltage name if enable/disable switch works

Vru 0	Vru 1	Vru 2	Vru 3	Vru 4	Vru 5
Vrl 0	Vrl 1	Vrl 2	Vrl 3	Vrl 4	Vrl 5
Vog 0	Vog 1	Vog 2	Vog 3	Vog 4	Vog 5
Vdd 0	Vdd 1	Vdd 2	Vdd 3	Vdd 4	Vdd 5

Stage 9. Vsub and Heater Control testing - Table 9

DAC Value	Vsub Measured Voltage Test Data 10%	50%	90%
Signal	volts	volts	volts
Vsub - rate	-1.24	3.77	8.79
Vsub - Limit	-1.24	3.77	8.79
Vsub0	0.00	0.00	0.00
	Vsub Enable Bit - pass		

DAC Value	Telemetery Readback Test Data 10%	50%	90%
Signal	dec	dec	dec
Vbias 0	154	274	468
Vbias 1	-27	698	1422
RTD1	220	NA	NA
RTD2	248	NA	NA
RTD3	274	NA	NA
RTD4	301	NA	NA
RTD5	325	NA	NA
RTD6	350	NA	NA
Reference 4096	837	NA	NA
eference buffere	837	NA	NA

Stage 10. Video Offset DAC Tests - Table 10.

	DAC Value 410				DAC Value 2048				DAC Value 3686			
ADC	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU
0	0.250	NA	NA	16956	1.250		NA	80983	2.250	NA	500ms	145012
1	0.250	NA	NA	17149	1.250		NA	81153	2.250	NA	500ms	145164
2	0.250	NA	NA	17133	1.250		NA	81165	2.250	NA	500ms	145196
3	0.250	NA	NA	17201	1.250		NA	81184	2.250	NA	500ms	145166
4	0.250	NA	NA	16831	1.250		NA	81013	2.250	NA	500ms	145212
5	0.250	NA	NA	17076	1.250		NA	81114	2.250	NA	500ms	145159
6	0.250	NA	NA	16987	1.250		NA	81058	2.250	NA	500ms	145127
7	0.250	NA	NA	17132	1.250		NA	81176	2.250	NA	500ms	145215
8	0.250	NA	NA	17178	1.250		NA	81199	2.250	NA	500ms	145219
9	0.250	NA	NA	17000	1.250		NA	81054	2.250	NA	500ms	145118
10	0.250	NA	NA	17182	1.250		NA	81153	2.250	NA	500ms	145121
11	0.250	NA	NA	17016	1.250		NA	81118	2.250	NA	500ms	145223

ADC	DC Volts		Data Set		
Channel	Slope	Offset	410	2048	3686
0	1638.000	0.500	0.250	1.250	2.250
1	1638.000	0.500	0.250	1.250	2.250
2	1638.000	0.500	0.250	1.250	2.250
3	1638.000	0.500	0.250	1.250	2.250
4	1638.000	0.500	0.250	1.250	2.250
5	1638.000	0.500	0.250	1.250	2.250
6	1638.000	0.500	0.250	1.250	2.250
7	1638.000	0.500	0.250	1.250	2.250
8	1638.000	0.500	0.250	1.250	2.250
9	1638.000	0.500	0.250	1.250	2.250
10	1638.000	0.500	0.250	1.250	2.250
11	1638.000	0.500	0.250	1.250	2.250

(dac# -offset)/slope=Voltage

ADC	ADU's		Data Set		
Channel	Slope	Offset	410	2048	3686
0	0.026	-23.77	16956	80983	145012
1	0.026	-28.83	17149	81153	145164
2	0.026	-28.29	17133	81165	145196
3	0.026	-30.36	17201	81184	145166
4	0.026	-19.42	16831	81013	145212
5	0.026	-26.73	17076	81114	145159
6	0.026	-24.29	16987	81058	145127
7	0.026	-28.21	17132	81176	145215
8	0.026	-29.51	17178	81199	145219
9	0.026	-24.65	17000	81054	145118
10	0.026	-29.97	17182	81153	145121
11	0.026	-24.79	17016	81118	145223

(dac# -offset)/slope=ADU

Notes and Observations

Checked for oscillations using a Agilent Oscilloscope on AC. OK

Stage 11. CDS Control Functions and Video Channel Performanc

TEST #1: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit is held static. The purpose of this test is to verify the correct operation of the ADC devices and measure the noise of the Offset voltage generators, ADC buffer amplifiers and ADC devices

Noise Test 1

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	80975	80993	80983.7	2.28353
CH 1	81146	81162	81154.5	2.20405
CH 2	81156	81172	81165.2	2.26055
CH 3	81176	81193	81184.5	2.19583
CH 4	81011	81026	81018.8	2.28422
CH 5	81110	81126	81117.2	2.29606
CH 6	81049	81066	81058	2.24708
CH 7	81167	81182	81174.2	2.33661
CH 8	81191	81206	81197.8	2.28835
CH 9	81048	81065	81057.1	2.16292
CH 10	81146	81163	81154.9	2.30799
CH 11	81110	81126	81118	2.31763

TEST #2: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the invert/non-invert and the DC Restore switches are held static.

Noise Test 2

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76196	76218	76206.8	2.70269
CH 1	77146	77167	77157.3	2.79763
CH 2	76303	76324	76314.1	2.92694
CH 3	76916	76938	76926	2.72543
CH 4	76306	76326	76315.7	2.77192
CH 5	76830	76850	76839.6	2.75935
CH 6	76601	76626	76615.2	2.95401
CH 7	77070	77090	77080.6	2.75338
CH 8	76677	76699	76688.8	2.81875
CH 9	77103	77125	77112.3	2.74425
CH 10	76638	76657	76647	2.78166
CH 11	76850	76868	76859.5	2.82977

TEST #3: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the DC Restore switch is held static.

Noise Test 3

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76192	76214	76203.2	3.0178
CH 1	77158	77181	77169.9	2.95714
CH 2	76294	76318	76305.1	3.21427
CH 3	76897	76920	76908.1	3.00718
CH 4	76299	76322	76309.9	2.99763
CH 5	76819	76843	76831.9	2.89984
CH 6	76600	76624	76611.8	3.1788
CH 7	77055	77077	77065.8	3.05629
CH 8	76674	76697	76684.8	3.08506
CH 9	77092	77113	77102.6	2.99953
CH 10	76642	76663	76652.7	3.11518
CH 11	76836	76858	76847.1	3.04826

TEST #4: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition.

Noise Test 4

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76181	76204	76192.3	3.10622
CH 1	77163	77184	77172.8	2.97591
CH 2	76298	76320	76308.5	3.30947
CH 3	76897	76919	76908.8	3.11808
CH 4	76340	76361	76351.4	2.99233
CH 5	76809	76833	76821	3.0919
CH 6	76607	76631	76617.6	3.24161
CH 7	77025	77050	77037.2	3.18413
CH 8	76718	76742	76729.8	3.18931
CH 9	77014	77036	77024.9	3.10353
CH 10	76659	76683	76671.6	3.15611
CH 11	76800	76822	76810.6	3.12962

TEST #5: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the circuitry set to high GAIN.

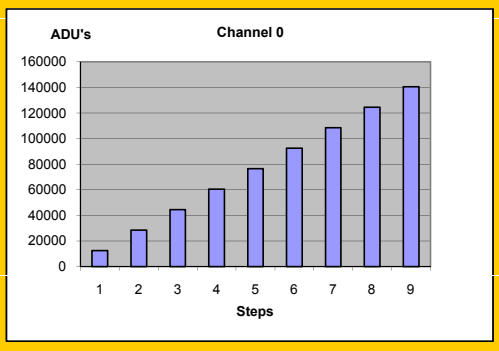
Noise Test 5

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76187	76213	76200.7	3.64363
CH 1	77173	77201	77185.3	3.58457
CH 2	76313	76342	76327.6	3.89016
CH 3	76903	76928	76914.7	3.5919
CH 4	76342	76368	76355.4	3.42395
CH 5	76802	76833	76819.2	3.55961
CH 6	76607	76635	76620.5	3.85952
CH 7	77025	77051	77038.6	3.64991
CH 8	76777	76804	76790.2	3.8412
CH 9	77009	77038	77024.2	3.64738
CH 10	76725	76751	76738.2	3.60982
CH 11	76797	76823	76810.1	3.64647

TEST #6A: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

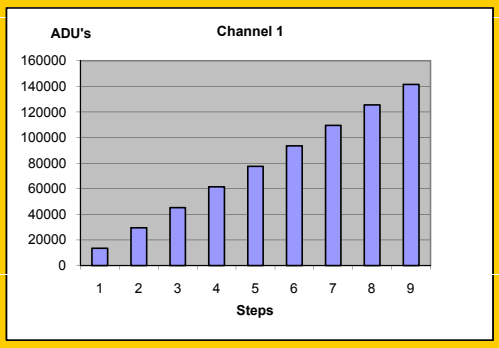
BrdTst6_006 / Channel 0					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12449	12473	12461.4	3.10695	10%
0x333	28434	28457	28444.9	3.1473	20%
0x4cc	44424	44448	44436.4	3.28463	30%
0x666	60448	60471	60459.4	3.11583	40%
0x800	76473	76498	76484.6	2.9727	50%
0x999	92464	92485	92474.6	3.07057	60%
0xb33	108487	108508	108498	2.94732	70%
0xccc	124481	124504	124492	3.08254	80%
0xe66	140505	140530	140518	3.17919	90%



TEST #6B: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

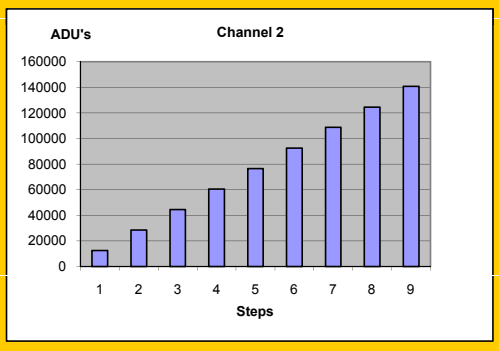
BrdTst6_006 / Channel 1					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13392	13415	13404.7	3.14558	10%
0x333	29376	29397	29386.4	3.14302	20%
0x4cc	45355	45381	45367.7	3.11709	30%
0x666	61375	61398	61387.6	3.16728	40%
0x800	77398	77421	77410.1	3.1234	50%
0x999	93381	93403	93390.9	3.15747	60%
0xb33	109401	109422	109411	2.99249	70%
0xccc	125385	125407	125395	3.10274	80%
0xe66	141407	141428	141416	3.03906	90%



TEST #6C: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

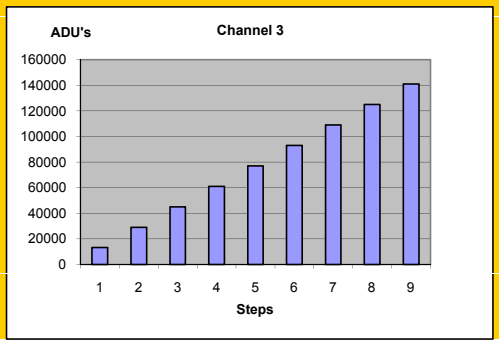
BrdTst6_006 / Channel 2					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12582	12608	12596	3.17967	10%
0x333	28569	28593	28580.6	3.49653	20%
0x4cc	44560	44586	44574	3.3412	30%
0x666	60586	60611	60597.9	3.35617	40%
0x800	76614	76637	76626	3.19384	50%
0x999	92606	92630	92618.4	3.3573	60%
0xb33	108630	108657	108642	3.38872	70%
0xccc	124624	124650	124638	3.30571	80%
0xe66	140649	140677	140662	3.27979	90%



TEST #6D: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

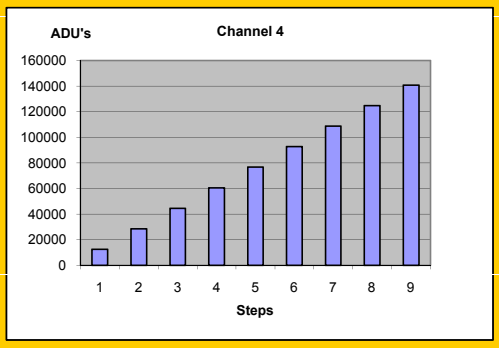
BrdTst6_006 / Channel 3					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13140	13162	13150.5	3.09197	10%
0x333	29112	29136	29123.9	3.15044	20%
0x4cc	45091	45112	45102	3.07738	30%
0x666	61103	61126	61114.4	3.08355	40%
0x800	77114	77139	77127.9	3.06263	50%
0x999	93092	93118	93105.3	3.06303	60%
0xb33	109108	109130	109119	3.12203	70%
0xccc	125087	125108	125099	3.06601	80%
0xe66	141102	141123	141113	3.1166	90%



TEST #6E: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

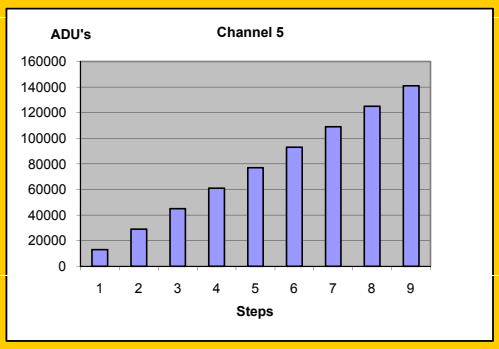
BrdTst6_006 / Channel 4					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12442	12464	12454.3	3.11505	10%
0x333	28471	28493	28482	2.95167	20%
0x4cc	44498	44522	44510.8	3.1755	30%
0x666	60566	60589	60577.9	3.12712	40%
0x800	76631	76654	76643.2	3.24294	50%
0x999	92659	92682	92670.8	3.14015	60%
0xb33	108726	108751	108738	2.99986	70%
0xccc	124760	124780	124770	2.96958	80%
0xe66	140828	140850	140838	3.06154	90%



TEST #6F: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

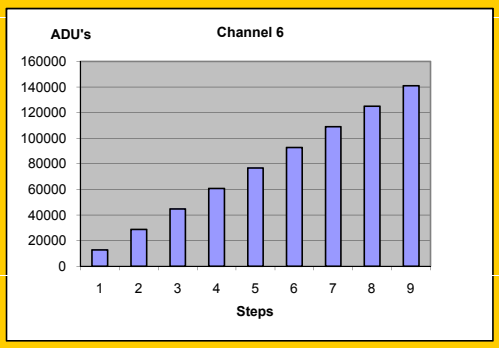
BrdTst6_006 / Channel 5					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13035	13062	13046.7	3.12114	10%
0x333	29024	29045	29034.7	3.26415	20%
0x4cc	45015	45038	45026.5	3.03451	30%
0x666	61041	61063	61052.8	3.26588	40%
0x800	77066	77089	77078.4	3.11563	50%
0x999	93060	93082	93070.7	3.19228	60%
0xb33	109086	109110	109097	3.14134	70%
0xccc	125081	125104	125092	3.04954	80%
0xe66	141108	141130	141119	3.14574	90%



TEST #6G: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

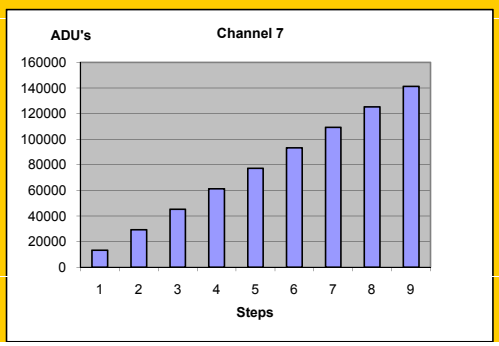
BrdTst6_006 / Channel 6					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12789	12815	12800.5	3.23582	10%
0x333	28783	28808	28795.5	3.34392	20%
0x4cc	44785	44806	44795.1	3.277	30%
0x666	60820	60841	60830.5	3.25554	40%
0x800	76853	76876	76864.5	3.22246	50%
0x999	92852	92876	92863.2	3.28636	60%
0xb33	108885	108910	108898	3.22315	70%
0xccc	124890	124913	124900	3.36756	80%
0xe66	140923	140947	140935	3.38396	90%



TEST #6H: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

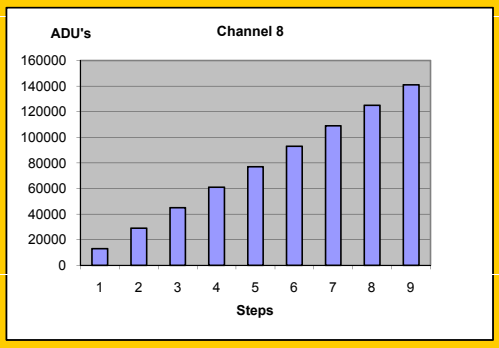
BrdTst6_006 / Channel 7					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13196	13220	13206.8	3.10667	10%
0x333	29187	29210	29197.7	3.15069	20%
0x4cc	45176	45198	45187.2	3.03435	30%
0x666	61207	61229	61216.9	3.0864	40%
0x800	77236	77258	77246.5	3.14479	50%
0x999	93226	93249	93238.1	3.05033	60%
0xb33	109253	109277	109266	3.00762	70%
0xccc	125248	125269	125259	3.18431	80%
0xe66	141278	141300	141289	3.18129	90%



TEST #6I: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

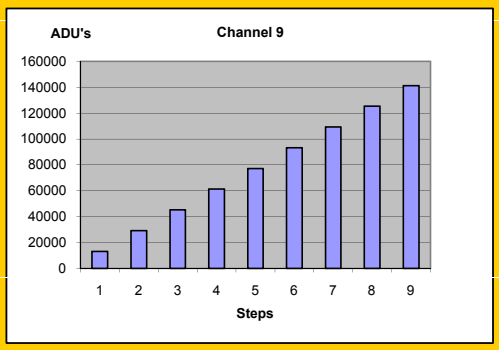
BrdTst6_006 / Channel 8					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12977	12998	12987	3.2355	10%
0x333	28961	28984	28972.3	3.22821	20%
0x4cc	44943	44966	44954.6	3.18226	30%
0x666	60967	60992	60980.6	3.22256	40%
0x800	76992	77019	77007	3.19233	50%
0x999	92983	93005	92992.5	3.25809	60%
0xb33	109006	109030	109018	3.20629	70%
0xccc	124992	125016	125003	3.24776	80%
0xe66	141017	141040	141029	3.16861	90%



TEST #6J: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

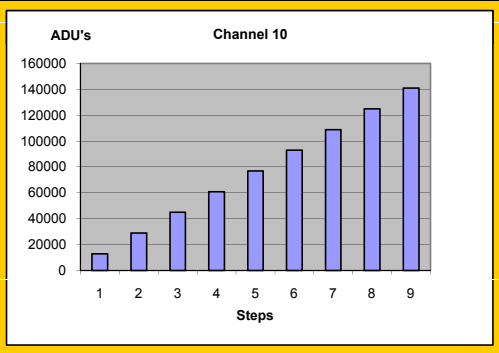
BrdTst6_006 / Channel 9					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13192	13217	13204.3	3.17845	10%
0x333	29189	29209	29199.2	3.10911	20%
0x4cc	45178	45201	45190.2	3.05719	30%
0x666	61215	61236	61225.3	3.11092	40%
0x800	77246	77268	77257.5	3.12645	50%
0x999	93242	93266	93253.6	3.21642	60%
0xb33	109276	109298	109287	3.10715	70%
0xccc	125270	125294	125281	3.00494	80%
0xe66	141307	141327	141317	2.9918	90%



TEST #6K: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

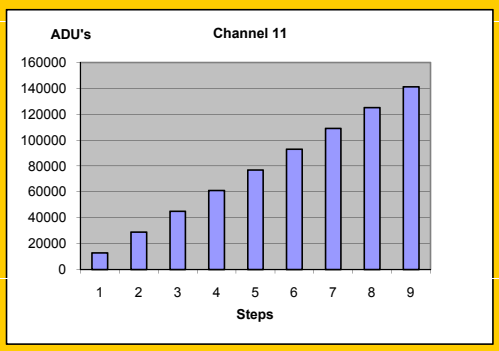
BrdTst6_006 / Channel 10					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12968	12991	12978.6	3.23645	10%
0x333	28934	28961	28949.5	3.25232	20%
0x4cc	44911	44937	44924.5	3.19243	30%
0x666	60925	60947	60935.6	3.13931	40%
0x800	76934	76956	76945.6	3.23291	50%
0x999	92906	92929	92918.8	3.2113	60%
0xb33	108917	108940	108929	3.12494	70%
0xccc	124894	124918	124907	3.23786	80%
0xe66	140906	140930	140919	3.23093	90%



TEST #6L: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

BrdTst6_006 / Channel 11					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12932	12956	12945.7	3.12574	10%
0x333	28938	28963	28952.3	3.12294	20%
0x4cc	44946	44968	44957.3	3.08996	30%
0x666	60993	61017	61004.2	3.17234	40%
0x800	77032	77056	77044.3	3.18757	50%
0x999	93038	93060	93049.6	3.18222	60%
0xb33	109084	109105	109095	3.05105	70%
0xccc	125093	125114	125103	3.14948	80%
0xe66	141139	141162	141150	3.14697	90%



Stage 13. Other Bit Tests. Table 11

Electronic Serial Number	0xDB8EE6		Board Serial Number	4
Firmware Version	0x193		Name Of Person Testing	S. Holm
Ident Register	0x502		Board passed Functional Tests	YES