DES 12 Channel Board - Functional Tests: CCD Acquisition Board Revision 1.0

Stage 1. Preparation of documentation and configuration settings - Table 1.

Board Part Number	5		Board Serial Number	0xDB8EEC
Date Of Tests	August 2010		Name Of Person Testing	S. Holm
Suggested Filename To Save	CCDACQ_12Ch_REPORT_BOARD12.xl		Sequence number: Test	

Stage 3. Power plane short test - Table 2.

Supply Name	Short test to ground: Impedance to ground	Test Point	
+1.2VD	44.00	TP43	~50 ohms
+1.8VD	2M	TPB12	> 1K ohm
+2.5VD	20k	TPB11	> 1K ohm
+3.3VD	7k	D13	> 1K ohm
+5VD	200k	D14	> 1K ohm
+5VA	4M	C267	> 1K ohm
-5VA	300K	C270	> 1K ohm
+15VA	400K	C288	> 1K ohm
-15VA	400K	C282	> 1K ohm
-28VA	2.5M	C307	> 1K ohm

Stage 4. Firmware programming tests - Table 3.

JTAG Order	Designator	Device	Load File	Check Sum or User Code
1	U122	XCF08PFS48C PROM	CcdAcqFpgaV41.mcs	0014ef670
2	U114	Spartan3 XC3S2000 FPGA	ccdacqfpgav41.bit	5102801

Stage 5. Power Consumption - Table 4.

Supply Name	Power Supply Consumption: Measured Voltage at test point	Measured Current on power supply	Test Point	
+1.2VD	1.19	N/A	TP43	
+1.8VD	2.49	N/A	TPB12	
+2.5VD	2.49	N/A	TPB11	
+3.3VD	3.29	0.23	D13	
+5VD	5.21	0.15	D14	
+5VA	4.92	0.55	C267	
-5VA	-5.00	0.43	C270	
+15VA	14.96	0.56	C288	
-15VA	-15.07	0.41	C282	
-28VA	-27.92	0.19	C307	
Vref 0+	10.04	N/A	R534	Vsub+ Reference(+10v)
Vref 0-	-2.50	N/A	R525	Vsub - Reference(-2.5v)
Vref Offset	2.50	N/A	R573	ADC Offset Reference(+2.5v)
Vclamp	1.87	N/A	VIA	ADC Clamp Voltage(+1.8v)
ADC Ref.	2.50	N/A	VIA	ADC Reference Voltage(+2.5v)
Vref 1+	2.50	N/A	R537	Vru and Vrl + Reference(+2.5v)
Vref 1-	-10.05	N/A	R535	Vru and Vrl - Reference(-10v)
Vref 2+	5.01	N/A	R563	Vog + Reference(+5v)
Vref 2-	-2.50	N/A	R555	Vog - Reference(-2.5v)
Vref 3+	2.50	N/A	R543	Vdd + Reference(+2.5v)
Vref 3-	-10.04	N/A	R571	Vdd - Reference(-10v)

Power Dissipation:
26.3 Watts

~27 watts +/- 5%

Stage 7. Basic Bus Transactions - **D**igital **Register** Tests - Table 5.

Register name	Put an X on any bit that has an error: 31-24 23-16 15-08 07-00	Function	Test name: Pattern	Walking 0's	Walking 1's
CDS Control	00000000 00000000	16 bit R/W			
Digital Output	00000000 00000000 00000000 00000000	32 bit R/W			
ADC Config.	0000 00000000	12 bit R/W			
Offset DAC	0000 00000000	12 bit R/W			
Bias DAC	0000 00000000	12 bit R/W			
Telemetry Config.	0000	4 bit R/W			
Auxilary Config.	00 00000000	10 bit R/W			
Redirect	0000	4 bit R/W			
Pixel Transfer	00000000	8 bit R/W			
Micro SEQ	00000000 00000000	16 bit R/W			
RAM Buffer	00000000 00000000	16 bit R/W			
LED Control	0000	4 bit R/W			
Control	00000000 00000000	16 bit R/W			
All Register Test	00000000 00000000 00000000 00000000	16 bit R/W	**Passed**	**Passed**	**Passed**

Stage 8. Bias Voltage settings and output enables testing - Table 8

DAC Value	Bias Voltage Test Data 410	2048	3686	50% rms Noise	10-90% Rise Time	Fanout Brd	Slope	Offset
Signal	volts	volts	volts	uV	millisec.			
Vru 0	-13.19	-5.65	1.86	<10	1	BIAS 3	217.67	3280.04
Vru 1	-13.20	-5.66	1.86	<10	1	BIAS 4	217.53	3280.67
Vru 2	-13.18	-5.66	1.86	<10	1	BIAS 5	217.82	3280.86
Vru 3	-13.18	-5.66	1.86	<10	1	BIAS 6	217.82	3280.86
Vru 4	-13.20	-5.66	1.86	<10	1	BIAS 7	217.53	3280.67
Vru 5	-13.18	-5.66	1.86	<10	1	BIAS 8	217.82	3280.86
Vru 6	-13.16	-5.66	1.86	NA	NA	BIAS 9	218.11	3281.04
Vru 7	-13.18	-5.66	1.86	NA	NA	BIAS 10	217.82	3280.86
Vrl 0	-13.21	-5.67	1.86	<10	1	BIAS 11	217.39	3281.30
Vrl 1	-13.19	-5.67	1.86	<10	1	BIAS 12	217.67	3281.49
Vrl 2	-13.20	-5.67	1.86	<10	1	BIAS 13	217.53	3281.39
Vrl 3	-13.19	-5.67	1.86	<10	1	BIAS 14	217.67	3281.49
Vrl 4	-13.19	-5.67	1.86	<10	1	BIAS 15	217.67	3281.49
Vrl 5	-13.19	-5.67	1.86	<10	1	BIAS 16	217.67	3281.49
Vrl 6	-13.18	-5.67	1.86	NA	NA	BIAS 17	217.82	3281.58
Vrl 7	-13.18	-5.67	1.86	NA	NA	BIAS 18	217.82	3281.58
Vog 0	-1.75	1.25	4.25	<10	1	BIAS 19	546.00	1365.50
Vog 1	-1.75	1.25	4.25	<10	1	BIAS 20	546.00	1365.50
Vog 2	-1.75	1.25	4.25	<10	1	BIAS 21	546.00	1365.50
Vog 3	-1.75	1.25	4.25	<10	1	BIAS 22	546.00	1365.50
Vog 4	-1.75	1.25	4.25	<10	1	BIAS 23	546.00	1365.50
Vog 5	-1.75	1.25	4.25	<10	1	BIAS 24	546.00	1365.50
Vog 6	-1.75	1.25	4.25	NA	NA	BIAS 25	546.00	1365.50
Vog 7	-1.75	1.25	4.25	NA	NA	BIAS 26	546.00	1365.50
Vdd 0	-22.02	-9.46	3.11	<10	20	BIAS 27	130.36	3280.79
Vdd 1	-22.07	-9.46	3.11	<10	20	BIAS 28	130.10	3280.51
Vdd 2	-22.04	-9.46	3.11	<10	20	BIAS 29	130.26	3280.68
Vdd 3	-21.98	-9.46	3.11	<10	20	BIAS 30	130.57	3281.01
Vdd 4	-21.95	-9.46	3.11	<10	20	BIAS 21	130.73	3281.18
Vdd 5	-22.00	-9.46	3.11	<10	20	BIAS 32	130.47	3280.90
Vdd 6	-22.01	-9.46	3.11	NA	NA	BIAS 33	130.41	3280.85
Vdd 7	-22.02	-9.46	3.11	NA	NA	BIAS 34	130.36	3280.79

Vru	Slope		Offset
Mean	217.76	Mean	3280.73
Stdev	0.1764387	Stdev	0.285428525
Average	217.76491	Average	3280.73019
	Dac #	Average voltage	
	0	-15.0	
	4095	3.7	

Vrl	Slope		Offset
Mean	217.66	Mean	3281.48
Stdev	0.1339672	Stdev	0.086913159
Average	217.65637	Average	3281.47638
	Dac #	Average voltage	
	0	-15.1	
	4095	3.7	

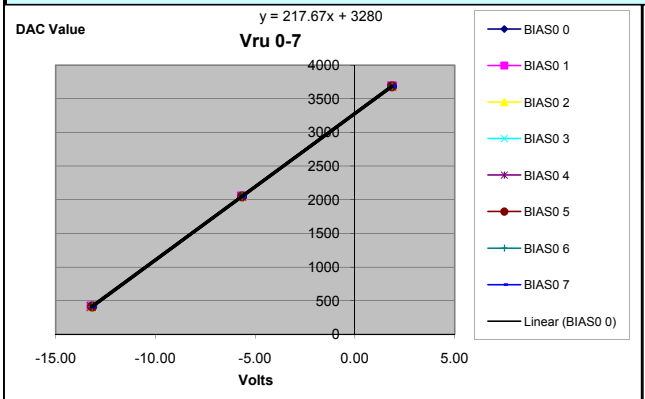
Vog	Slope		Offset
Mean	546.00	Mean	1365.50
Stdev	0	Stdev	0
Average	546	Average	1365.5
	Dac #	Average voltage	
	0	-2.5	
	4095	5.0	

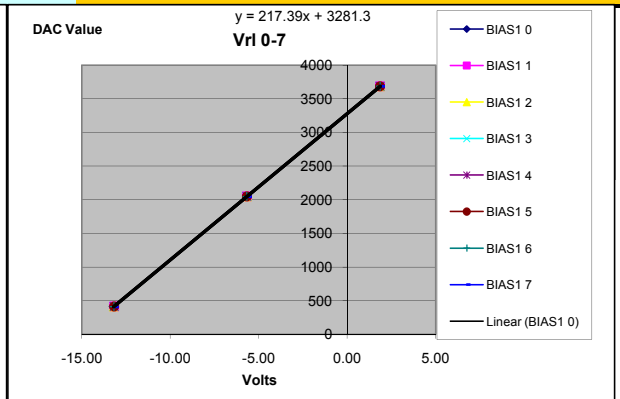
Vdd	Slope		Offset
Mean	130.41	Mean	3280.84
Stdev	0.1768038	Stdev	0.190134988
Average	130.40766	Average	3280.839397
	Dac #	Average voltage	
	0	-25.2	
	4095	6.3	

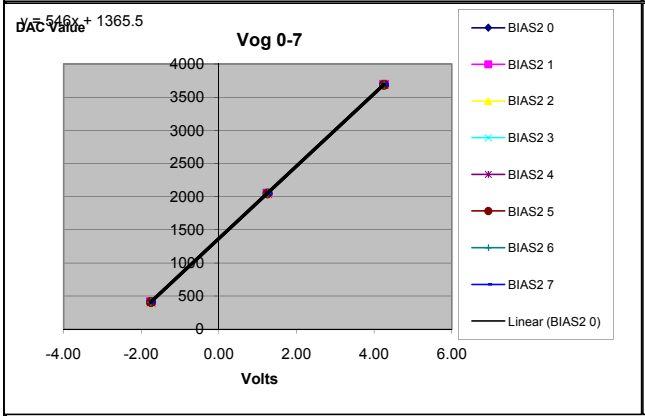
Notes and Observations

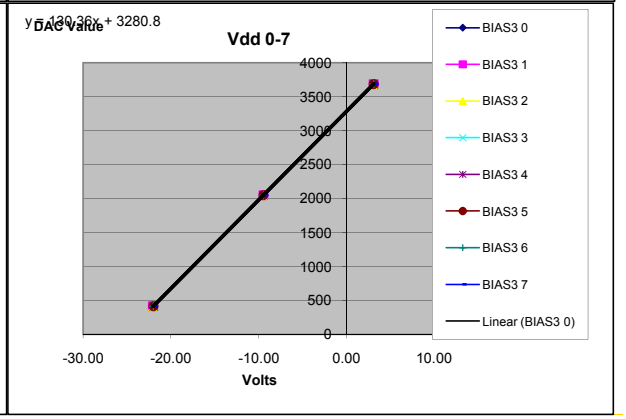
Checked for oscillations using a Agilent Oscilloscpe on AC.**OK**

average min & max voltages
(dac# -offset)/slope=voltage









Stage 8B. Telemetry System Tests - Table 7 (Bias Telemetry Tests)

DAC Value: 410 / 3686

Signal	Telemetry Return Values 10%	90%	Bias Signals Set Volts 10%	90%	Resolved Values for Telemetry Channel Slope	Offset
Vru 0	-1733	422	-13.19	1.86	143.1894	155.67
Vru 1	-1733	422	-13.20	1.86	143.0943	155.84
Vru 2	-1731	422	-13.18	1.86	143.1516	155.74
Vru 3	-1735	423	-13.18	1.86	143.4840	156.12
Vru 4	-1735	422	-13.20	1.86	143.2271	155.60
Vru 5	-1732	422	-13.18	1.86	143.2181	155.61
Vru 6	-1734	422	-13.16	1.86	143.5419	155.01
Vru 7	-1734	422	-13.18	1.86	143.3511	155.37
Vrl 0	-1743	422	-13.21	1.86	143.6629	154.79
Vrl 1	-1739	422	-13.19	1.86	143.5880	154.93
Vrl 2	-1741	422	-13.20	1.86	143.6255	154.86
Vrl 3	-1738	422	-13.19	1.86	143.5216	155.05
Vrl 4	-1740	422	-13.19	1.86	143.6545	154.80
Vrl 5	-1740	422	-13.19	1.86	143.6545	154.80
Vrl 6	-1739	422	-13.18	1.86	143.6835	154.75
Vrl 7	-1740	422	-13.18	1.86	143.7500	154.63
Vog 0	-362	867	-1.75	4.25	204.8333	-3.54
Vog 1	-362	868	-1.75	4.25	205.0000	-3.25
Vog 2	-362	868	-1.75	4.25	205.0000	-3.25
Vog 3	-362	867	-1.75	4.25	204.8333	-3.54
Vog 4	-362	868	-1.75	4.25	205.0000	-3.25
Vog 5	-362	868	-1.75	4.25	205.0000	-3.25
Vog 6	-362	868	-1.75	4.25	205.0000	-3.25
Vog 7	-362	867	-1.75	4.25	204.8333	-3.54
Vdd 0	-1697	571	-22.02	3.11	90.2507	290.32
Vdd 1	-1702	574	-22.07	3.11	90.3892	292.89
Vdd 2	-1697	574	-22.04	3.11	90.2982	293.17
Vdd 3	-1692	573	-21.98	3.11	90.2750	292.24
Vdd 4	-1687	573	-21.95	3.11	90.1836	292.53
Vdd 5	-1694	574	-22.00	3.11	90.3226	293.10
Vdd 6	-1695	573	-22.01	3.11	90.2866	292.21
Vdd 7	-1696	574	-22.02	3.11	90.3303	293.07

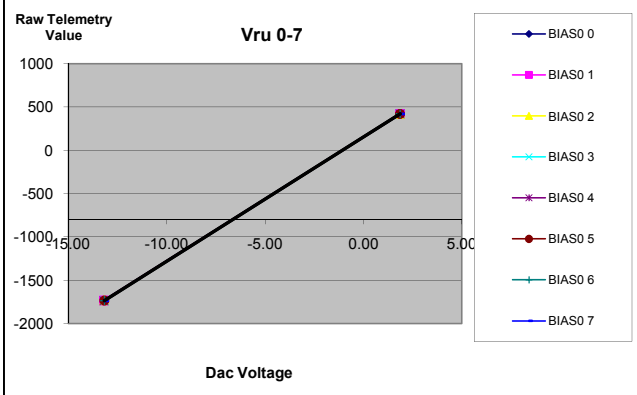
AVERAGE

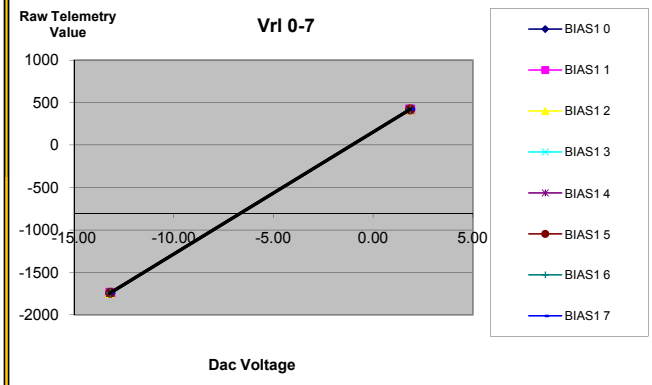
Vru	Slope		Offset
Mean	143.28	Mean	155.62
Stdev	0.1504505	Stdev	0.3063014

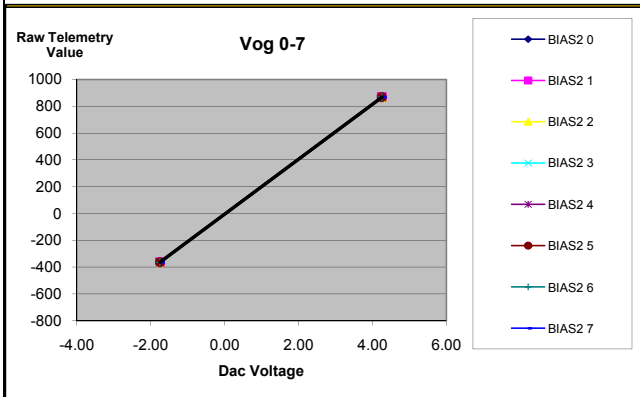
Vrl	Slope		Offset
Mean	143.64	Mean	154.82
Stdev	0.0630623	Stdev	0.1172959

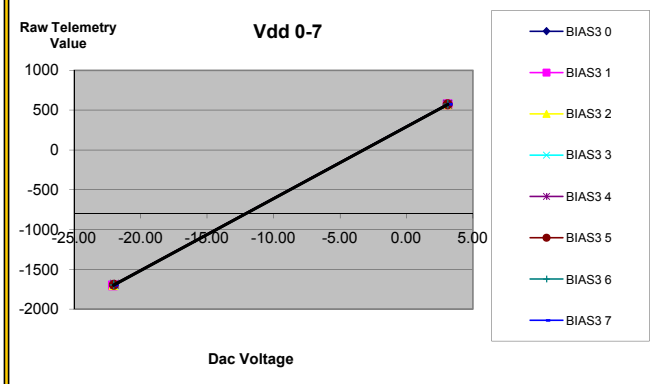
Vog	Slope		Offset
Mean	204.94	Mean	-3.36
Stdev	0.0806872	Stdev	0.1412025

Vdd	Slope		Offset
Mean	90.29	Mean	292.44
Stdev	0.0566454	Stdev	0.8777232









Stage 8C. Bias Voltage output enables testing - Table 8

Place a line through Bias Voltage name if enable/disable switch works

Vru 0	Vru 1	Vru 2	Vru 3	Vru 4	Vru 5
Vrl 0	Vrl 1	Vrl 2	Vrl 3	Vrl 4	Vrl 5
Vog 0	Vog 1	Vog 2	Vog 3	Vog 4	Vog 5
Vdd 0	Vdd 1	Vdd 2	Vdd 3	Vdd 4	Vdd 5

Stage 9. Vsub and Heater Control testing - Table 9

DAC Value	Vsub Measured Voltage Test Data 10%	50%	90%
Signal	volts	volts	volts
Vsub - rate	-1.25	3.78	8.80
Vsub - Limit	-1.25	3.78	8.80
Vsub0	0.00	0.00	0.00
	Vsub Enable Bit - pass		

DAC Value	Telemetery Readback Test Data 10%	50%	90%
Signal	dec	dec	dec
Vbias 0	155	277	472
Vbias 1	-24	697	1417
RTD1	220	NA	NA
RTD2	249	NA	NA
RTD3	274	NA	NA
RTD4	302	NA	NA
RTD5	326	NA	NA
RTD6	352	NA	NA
Reference 4096	837	NA	NA
eference buffere	837	NA	NA

Stage 10. Video Offset DAC Tests - Table 10.

	DAC Value 410				DAC Value 2048				DAC Value 3686			
ADC	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU
0	0.250	NA	NA	16962	1.250		NA	81028	2.250	NA	500ms	145092
1	0.250	NA	NA	17052	1.250		NA	81060	2.250	NA	500ms	145087
2	0.250	NA	NA	17050	1.250		NA	81086	2.250	NA	500ms	145118
3	0.250	NA	NA	16957	1.250		NA	81083	2.250	NA	500ms	145211
4	0.250	NA	NA	17185	1.250		NA	81200	2.250	NA	500ms	145214
5	0.250	NA	NA	17093	1.250		NA	81197	2.250	NA	500ms	145302
6	0.250	NA	NA	16940	1.250		NA	81067	2.250	NA	500ms	145204
7	0.250	NA	NA	17192	1.250		NA	81226	2.250	NA	500ms	145258
8	0.250	NA	NA	17128	1.250		NA	81188	2.250	NA	500ms	145250
9	0.250	NA	NA	17058	1.250		NA	81103	2.250	NA	500ms	145141
10	0.250	NA	NA	17257	1.250		NA	81299	2.250	NA	500ms	145343
11	0.250	NA	NA	17049	1.250		NA	81106	2.250	NA	500ms	145162

ADC	DC Volts		Data Set		
Channel	Slope	Offset	410	2048	3686
0	1638.000	0.500	0.250	1.250	2.250
1	1638.000	0.500	0.250	1.250	2.250
2	1638.000	0.500	0.250	1.250	2.250
3	1638.000	0.500	0.250	1.250	2.250
4	1638.000	0.500	0.250	1.250	2.250
5	1638.000	0.500	0.250	1.250	2.250
6	1638.000	0.500	0.250	1.250	2.250
7	1638.000	0.500	0.250	1.250	2.250
8	1638.000	0.500	0.250	1.250	2.250
9	1638.000	0.500	0.250	1.250	2.250
10	1638.000	0.500	0.250	1.250	2.250
11	1638.000	0.500	0.250	1.250	2.250

(dac# -offset)/slope=Voltage

ADC	ADU's		Data Set		
Channel	Slope	Offset	410	2048	3686
0	0.026	-23.69	16962	81028	145092
1	0.026	-26.22	17052	81060	145087
2	0.026	-26.16	17050	81086	145118
3	0.026	-23.13	16957	81083	145211
4	0.026	-29.73	17185	81200	145214
5	0.026	-26.76	17093	81197	145302
6	0.026	-22.62	16940	81067	145204
7	0.026	-29.79	17192	81226	145258
8	0.026	-27.94	17128	81188	145250
9	0.026	-26.33	17058	81103	145141
10	0.026	-31.37	17257	81299	145343
11	0.026	-25.97	17049	81106	145162

(dac# -offset)/slope=ADU

Notes and Observations

Checked for oscillations using a Agilent Oscilloscope on AC. OK

Stage 11. CDS Control Functions and Video Channel Performanc

TEST #1: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit is held static. The purpose of this test is to verify the correct operation of the ADC devices and measure the noise of the Offset voltage generators, ADC buffer amplifiers and ADC devices

Noise Test 1

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	81020	8.10E+04	81028.8	2.24581
CH 1	81057	8.11E+04	81064.9	2.31831
CH 2	81076	8.11E+04	81085	2.25961
CH 3	81077	8.11E+04	81085	2.3002
CH 4	81193	8.12E+04	81200.9	2.19383
CH 5	81188	8.12E+04	81197.4	2.37782
CH 6	81061	8.11E+04	81070.6	2.37328
CH 7	81217	8.12E+04	81224.9	2.40803
CH 8	81180	8.12E+04	81188.9	2.20967
CH 9	81094	81110	81102.1	2.38617
CH 10	81288	81306	81297.9	2.2787
CH 11	81098	81115	81106.4	2.36177

TEST #2: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the invert/non-invert and the DC Restore switches are held static.

Noise Test 2

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76396	7.64E+04	76405.5	2.67849
CH 1	76892	7.69E+04	76902.8	2.74002
CH 2	76260	7.63E+04	76272.2	2.84544
CH 3	77002	7.70E+04	77011.4	2.94176
CH 4	76393	7.64E+04	76404.5	2.78134
CH 5	77013	7.70E+04	77024.1	2.79904
CH 6	76927	7.69E+04	76937.5	2.85041
CH 7	77103	7.71E+04	77113.3	2.86144
CH 8	76752	7.68E+04	76762.6	2.81186
CH 9	76802	76823	76811.8	3.03604
CH 10	76880	76900	76890.4	2.9028
CH 11	76792	76813	76802.6	3.04197

TEST #3: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the DC Restore switch is held static.

Noise Test 3

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76399	7.64E+04	76410.1	2.98995
CH 1	76889	7.69E+04	76900.3	2.89493
CH 2	76259	7.63E+04	76270.4	3.08345
CH 3	76983	7.70E+04	76993.1	3.0169
CH 4	76394	7.64E+04	76405.8	3.09565
CH 5	77006	7.70E+04	77019.5	3.14271
CH 6	76919	7.69E+04	76929.5	3.04056
CH 7	77108	7.71E+04	77118.6	3.08463
CH 8	76751	7.68E+04	76763.2	3.00577
CH 9	76800	76822	76811	3.25708
CH 10	76878	76899	76888.2	3.10441
CH 11	76792	76816	76803.5	3.24883

TEST #4: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition.

Noise Test 4

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76385	7.64E+04	76397.9	3.16947
CH 1	76893	7.69E+04	76903.4	3.0585
CH 2	76262	7.63E+04	76273.7	3.27899
CH 3	76982	7.70E+04	76994.3	3.12833
CH 4	76425	7.64E+04	76436.4	3.30278
CH 5	76997	7.70E+04	77008.3	3.12507
CH 6	76925	7.69E+04	76937.2	3.24726
CH 7	77067	7.71E+04	77077.5	3.09455
CH 8	76791	7.68E+04	76801.9	3.03759
CH 9	76713	76738	76726.3	3.3055
CH 10	76894	76917	76905.5	3.20435
CH 11	76750	76774	76762	3.28063

TEST #5: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the circuitry set to high GAIN.

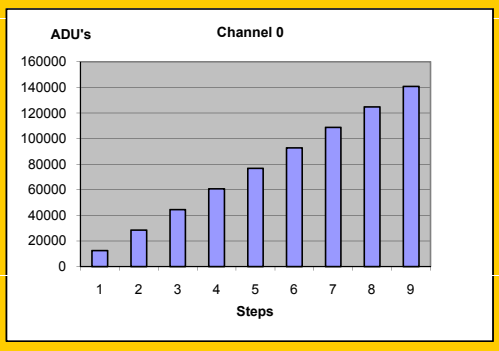
Noise Test 5

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76402	7.64E+04	76415	3.70137
CH 1	76900	7.69E+04	76915.7	3.71199
CH 2	76270	7.63E+04	76285.3	3.93024
CH 3	76987	7.70E+04	76999.7	3.7127
CH 4	76428	7.65E+04	76441.8	3.95637
CH 5	76994	7.70E+04	77007.3	3.75118
CH 6	76926	7.70E+04	76940.1	3.6722
CH 7	77065	7.71E+04	77079.3	3.68794
CH 8	76840	7.69E+04	76853.5	3.64476
CH 9	76713	76740	76725.7	3.84335
CH 10	76957	76982	76969.8	3.67324
CH 11	76747	76775	76761.3	3.90691

TEST #6A: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

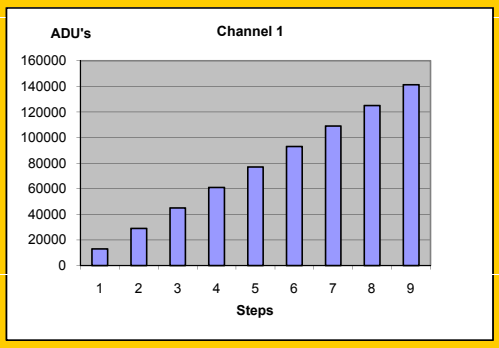
BrdTst6_006 / Channel 0					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12610	12633	12620.6	3.19702	10%
0x333	28605	28630	28617.1	3.20767	20%
0x4cc	44603	44625	44614.6	3.32145	30%
0x666	60639	60662	60649.7	3.17146	40%
0x800	76672	76695	76682.9	3.19619	50%
0x999	92668	92690	92678.1	3.10345	60%
0xb33	108702	108728	108715	3.20926	70%
0xccc	124703	124724	124712	3.16087	80%
0xe66	140738	140761	140750	3.24931	90%



TEST #6B: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

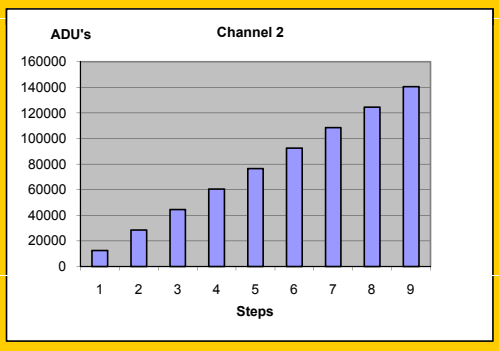
BrdTst6_006 / Channel 1					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13103	13125	13114.1	3.17686	10%
0x333	29089	29112	29099.7	3.18594	20%
0x4cc	45072	45096	45083	3.19163	30%
0x666	61094	61119	61106.6	3.25448	40%
0x800	77116	77138	77127.2	3.03088	50%
0x999	93099	93121	93110.1	3.07514	60%
0xb33	109124	109149	109134	3.13727	70%
0xccc	125107	125132	125120	3.1394	80%
0xe66	141133	141157	141144	3.21956	90%



TEST #6C: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

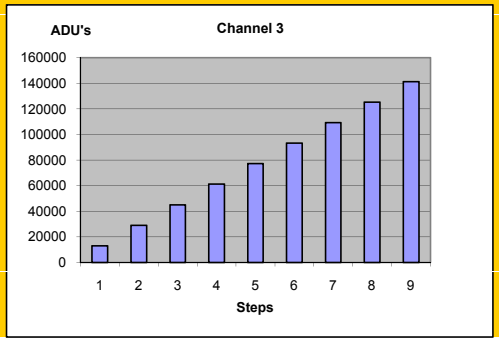
BrdTst6_006 / Channel 2					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12546	12567	12555.9	3.2543	10%
0x333	28532	28556	28544.5	3.07586	20%
0x4cc	44519	44546	44534.2	3.11762	30%
0x666	60550	60573	60562.3	3.12743	40%
0x800	76573	76597	76585.5	3.18834	50%
0x999	92560	92584	92572.1	3.21433	60%
0xb33	108588	108611	108600	3.27293	70%
0xccc	124581	124603	124592	3.15153	80%
0xe66	140607	140629	140619	3.27832	90%



TEST #6D: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

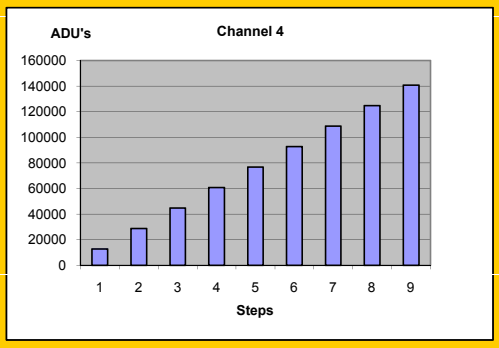
BrdTst6_006 / Channel 3					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13080	13101	13090.2	2.93019	10%
0x333	29091	29113	29101.9	3.10605	20%
0x4cc	45101	45125	45113.4	3.09923	30%
0x666	61154	61176	61165.4	3.13781	40%
0x800	77202	77223	77212.7	3.14193	50%
0x999	93212	93235	93223.3	3.06045	60%
0xb33	109264	109286	109276	3.13766	70%
0xccc	125279	125301	125289	3.0999	80%
0xe66	141332	141353	141342	3.09573	90%



TEST #6E: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

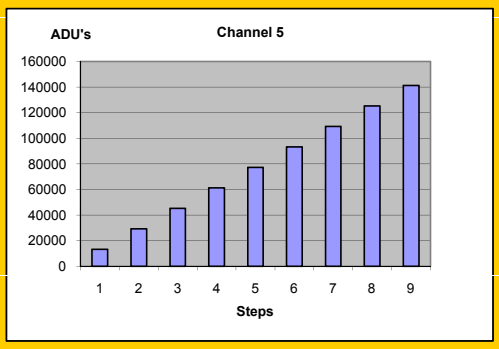
BrdTst6_006 / Channel 4					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12722	12744	12733.4	3.3236	10%
0x333	28709	28732	28719.8	3.26504	20%
0x4cc	44689	44714	44701.6	3.4338	30%
0x666	60713	60740	60726.4	3.41426	40%
0x800	76736	76759	76746.8	3.37247	50%
0x999	92720	92742	92731.1	3.35422	60%
0xb33	108744	108768	108756	3.30885	70%
0xccc	124728	124755	124741	3.43658	80%
0xe66	140755	140780	140768	3.40353	90%



TEST #6F: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

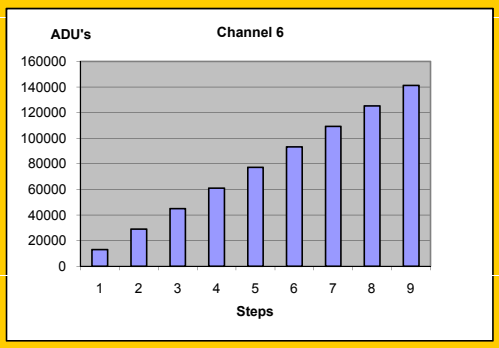
BrdTst6_006 / Channel 5					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13138	13160	13148.5	3.24307	10%
0x333	29143	29166	29155.2	3.25038	20%
0x4cc	45146	45171	45158.2	3.22332	30%
0x666	61191	61214	61202.6	3.30647	40%
0x800	77234	77260	77246.7	3.2689	50%
0x999	93241	93268	93255.8	3.13862	60%
0xb33	109291	109311	109301	3.08111	70%
0xccc	125295	125316	125306	3.18831	80%
0xe66	141340	141364	141353	3.16632	90%



TEST #6G: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

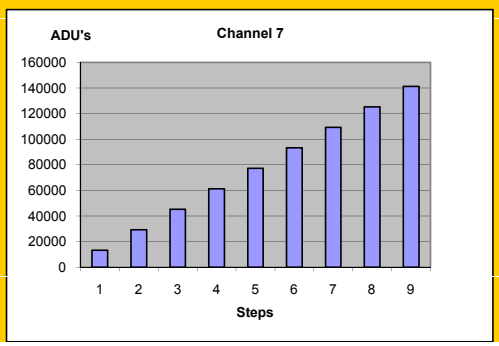
BrdTst6_006 / Channel 6					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13017	13041	13028.7	3.18176	10%
0x333	29032	29052	29042.3	3.05663	20%
0x4cc	45039	45062	45050.8	3.15638	30%
0x666	61093	61115	61103.8	3.06858	40%
0x800	77145	77166	77156.1	2.98791	50%
0x999	93160	93184	93170.9	3.16924	60%
0xb33	109213	109234	109224	3.18313	70%
0xccc	125224	125246	125235	3.31548	80%
0xe66	141277	141301	141288	3.12007	90%



TEST #6H: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

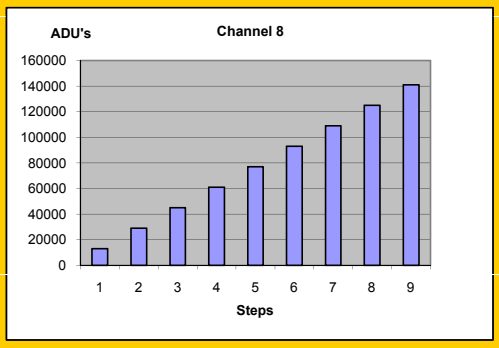
BrdTst6_006 / Channel 7					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13260	13281	13270.1	3.14034	10%
0x333	29248	29270	29259	3.21842	20%
0x4cc	45232	45254	45242.6	3.2095	30%
0x666	61260	61281	61270.5	3.14829	40%
0x800	77284	77308	77294.7	3.17365	50%
0x999	93272	93296	93284.2	3.24967	60%
0xb33	109301	109326	109313	3.27488	70%
0xccc	125290	125310	125299	3.20195	80%
0xe66	141317	141342	141330	3.22162	90%



TEST #6I: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

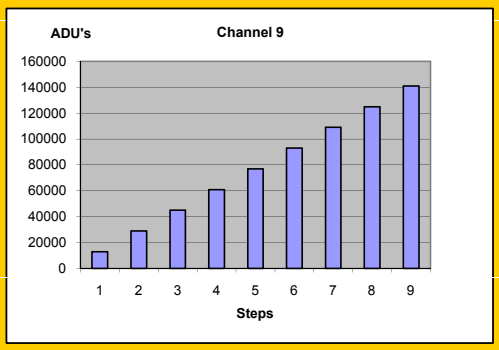
BrdTst6_006 / Channel 8					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12966	12992	12978.5	3.18099	10%
0x333	28964	28986	28974.4	3.14289	20%
0x4cc	44962	44985	44971.8	3.17188	30%
0x666	60996	61019	61007.4	3.08329	40%
0x800	77027	77050	77039.9	3.11023	50%
0x999	93027	93047	93037	3.10719	60%
0xb33	109061	109085	109073	3.1155	70%
0xccc	125063	125085	125073	3.13064	80%
0xe66	141096	141120	141107	3.00386	90%



TEST #6J: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

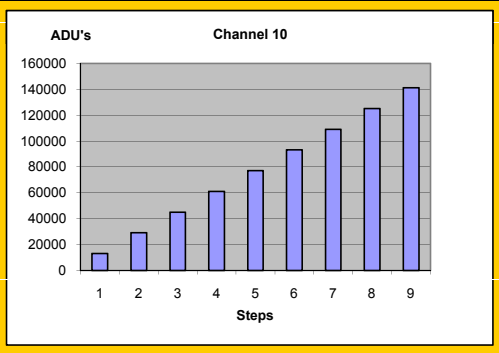
BrdTst6_006 / Channel 9					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12942	12966	12954.8	3.4582	10%
0x333	28935	28958	28946.4	3.4126	20%
0x4cc	44922	44947	44934.7	3.34916	30%
0x666	60948	60974	60962.5	3.33803	40%
0x800	76980	77003	76990.8	3.28777	50%
0x999	92973	92997	92984	3.3763	60%
0xb33	108999	109027	109013	3.43105	70%
0xccc	124994	125017	125005	3.35826	80%
0xe66	141024	141050	141038	3.4215	90%



TEST #6K: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

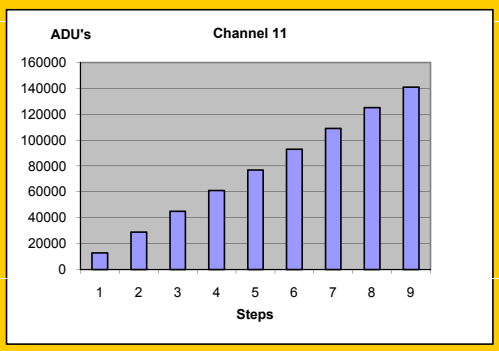
BrdTst6_006 / Channel 10					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13109	13131	13120.3	3.28205	10%
0x333	29099	29122	29111.4	3.13177	20%
0x4cc	45090	45112	45101	3.20993	30%
0x666	61120	61144	61131.9	3.23146	40%
0x800	77150	77172	77161.3	3.126	50%
0x999	93144	93169	93155.8	3.27446	60%
0xb33	109174	109198	109186	3.11903	70%
0xccc	125166	125190	125178	3.26093	80%
0xe66	141200	141222	141210	3.16428	90%



TEST #6L: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

BrdTst6_006 / Channel 11					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12962	12985	12973.1	3.34594	10%
0x333	28954	28978	28966.5	3.30328	20%
0x4cc	44950	44973	44961.5	3.4305	30%
0x666	60982	61005	60993.6	3.12339	40%
0x800	77016	77039	77026.8	3.2972	50%
0x999	93011	93034	93023.2	3.42895	60%
0xb33	109041	109067	109055	3.29331	70%
0xccc	125042	125067	125053	3.31149	80%
0xe66	141077	141102	141088	3.23284	90%



Stage 13. Other Bit Tests. Table 11

Electronic Serial Number	0xDB8EEC		Board Serial Number	5
Firmware Version	0x193		Name Of Person Testing	S. Holm
Ident Register	0x502		Board passed Functional Tests	YES