DES 12 Channel Board - Functional Tests: CCD Acquisition Board Revision 1.0

Stage 1. Preparation of documentation and configuration settings - Table 1.

Board Part Number	22		Board Serial Number	0xDB8EC0
Date Of Tests	May 2010		Name Of Person Testing	S. Holm
Suggested Filename To Save	CCDACQ_12Ch_REPORT_BOARD27.xl		Sequence number: Test	

Stage 3. Power plane short test - Table 2.

Supply Name	Short test to ground: Impedance to ground	Test Point	
+1.2VD	49.00	TP43	~50 ohms
+1.8VD	2M	TPB12	> 1K ohm
+2.5VD	17K	TPB11	> 1K ohm
+3.3VD	4.3K	D13	> 1K ohm
+5VD	18K	D14	> 1K ohm
+5VA	5M	C267	> 1K ohm
-5VA	500k	C270	> 1K ohm
+15VA	2.1M	C288	> 1K ohm
-15VA	2.1M	C282	> 1K ohm
-28VA	300K	C307	> 1K ohm

Stage 4. Firmware programming tests - Table 3.

JTAG Order	Designator	Device	Load File	Check Sum or User Code
1	U122	XCF08PFS48C PROM	CcdAcqFpgaV41.mcs	0014ef670
2	U114	Spartan3 XC3S2000 FPGA	ccdacqfpgav41.bit	5102801

Stage 5. Power Consumption - Table 4.

Supply Name	Power Supply Consumption: Measured Voltage at test point	Measured Current on power supply	Test Point	
+1.2VD	1.21	N/A	TP43	
+1.8VD	1.80	N/A	TPB12	
+2.5VD	2.51	N/A	TPB11	
+3.3VD	3.27	0.214	D13	
+5VD	5.20	0.158	D14	
+5VA	5.00	0.6	C267	
-5VA	-5.02	0.439	C270	
+15VA	15.00	0.558	C288	
-15VA	-15.03	0.407	C282	
-28VA	-28.00	0.208	C307	
Vref 0+	10.03	N/A	R534	Vsub+ Reference(+10v)
Vref 0-	-2.48	N/A	R525	Vsub - Reference(-2.5v)
Vref Offset	2.50	N/A	R573	ADC Offset Reference(+2.5v)
Vclamp	1.88	N/A	VIA	ADC Clamp Voltage(+1.8v)
ADC Ref.	2.50	N/A	VIA	ADC Reference Voltage(+2.5v)
Vref 1+	2.50	N/A	R537	Vru and Vrl + Reference(+2.5v)
Vref 1-	-9.99	N/A	R535	Vru and Vrl - Reference(-10v)
Vref 2+	5.01	N/A	R563	Vog + Reference(+5v)
Vref 2-	-2.48	N/A	R555	Vog - Reference(-2.5v)
Vref 3+	2.50	N/A	R543	Vdd + Reference(+2.5v)
Vref 3-	-9.93	N/A	R571	Vdd - Reference(-10v)

Power Dissipation:
27.0 Watts

~27 watts +/- 5%

Stage 7. Basic Bus Transactions - **D**igital **Register** Tests - Table 5.

Register name	Put an X on any bit that has an error: 31-24	23-16	15-08	07-00	Function	Test name: Pattern	Walking 0's	Walking 1's
CDS Control			00000000	00000000	16 bit R/W			
Digital Output	00000000	00000000	00000000	00000000	32 bit R/W			
ADC Config.			0000	00000000	12 bit R/W			
Offset DAC			0000	00000000	12 bit R/W			
Bias DAC			0000	00000000	12 bit R/W			
Telemetry Config.				0000	4 bit R/W			
Auxilary Config.			00	00000000	10 bit R/W			
Redirect				0000	4 bit R/W			
Pixel Transfer				00000000	8 bit R/W			
Micro SEQ			00000000	00000000	16 bit R/W			
RAM Buffer			00000000	00000000	16 bit R/W			
LED Control				0000	4 bit R/W			
Control			00000000	00000000	16 bit R/W			
All Register Test	00000000	00000000	00000000	00000000	16 bit R/W	**Passed**	**Passed**	**Passed**

Stage 8. Bias Voltage settings and output enables testing - Table 8

DAC Value	410	Bias Voltage Test Data 2048	3686	50% rms Noise	10-90% Rise Time			
Signal	volts	volts	volts	uV	millisec.	Fanout Brd	Slope	Offset
Vru 0	-13.14	-5.62	1.87	<10	1	BIAS 3	218.25	3276.77
Vru 1	-13.14	-5.62	1.87	<10	1	BIAS 4	218.25	3276.77
Vru 2	-13.15	-5.62	1.87	<10	1	BIAS 5	218.11	3276.68
Vru 3	-13.13	-5.62	1.87	<10	1	BIAS 6	218.40	3276.86
Vru 4	-13.11	-5.62	1.87	<10	1	BIAS 7	218.69	3277.05
Vru 5	-13.13	-5.62	1.87	<10	1	BIAS 8	218.40	3276.86
Vru 6	-13.13	-5.62	1.87	NA	NA	BIAS 9	218.40	3276.86
Vru 7	-13.13	-5.62	1.87	NA	NA	BIAS 10	218.40	3276.86
Vrl 0	-13.11	-5.62	1.87	<10	1	BIAS 11	218.69	3277.05
Vrl 1	-13.11	-5.62	1.87	<10	1	BIAS 12	218.69	3277.05
Vrl 2	-13.12	-5.62	1.87	<10	1	BIAS 13	218.55	3276.96
Vrl 3	-13.10	-5.62	1.87	<10	1	BIAS 14	218.84	3277.14
Vrl 4	-13.14	-5.62	1.87	<10	1	BIAS 15	218.25	3276.77
Vrl 5	-13.11	-5.62	1.87	<10	1	BIAS 16	218.69	3277.05
Vrl 6	-13.12	-5.62	1.87	NA	NA	BIAS 17	218.55	3276.96
Vrl 7	-13.13	-5.62	1.87	NA	NA	BIAS 18	218.40	3276.86
Vog 0	-1.73	1.26	4.25	<10	1	BIAS 19	547.83	1357.74
Vog 1	-1.73	1.26	4.25	<10	1	BIAS 20	547.83	1357.74
Vog 2	-1.74	1.26	4.25	<10	1	BIAS 21	546.91	1360.72
Vog 3	-1.73	1.26	4.25	<10	1	BIAS 22	547.83	1357.74
Vog 4	-1.73	1.26	4.25	<10	1	BIAS 23	547.83	1357.74
Vog 5	-1.73	1.26	4.25	<10	1	BIAS 24	547.83	1357.74
Vog 6	-1.73	1.26	4.25	NA	NA	BIAS 25	547.83	1357.74
Vog 7	-1.73	1.26	4.25	NA	NA	BIAS 26	547.83	1357.74
Vdd 0	-21.80	-9.33	3.14	<10	20	BIAS 27	131.36	3273.54
Vdd 1	-21.84	-9.35	3.15	<10	20	BIAS 28	131.09	3273.28
Vdd 2	-21.75	-9.31	3.13	<10	20	BIAS 29	131.67	3273.87
Vdd 3	-21.68	-9.28	3.12	<10	20	BIAS 30	132.10	3273.86
Vdd 4	-21.73	-9.30	3.13	<10	20	BIAS 21	131.78	3273.53
Vdd 5	-21.77	-9.32	3.14	<10	20	BIAS 32	131.51	3273.27
Vdd 6	-21.77	-9.32	3.14	NA	NA	BIAS 33	131.51	3273.27
Vdd 7	-21.76	-9.31	3.14	NA	NA	BIAS 34	131.57	3272.88

Vru	Slope		Offset
Mean	218.36	Mean	3276.84
Stdev	0.1588084	Stdev	0.100214301
Average	218.36352	Average	3276.840129
	Dac #	Average voltage	
	0	-15.0	
	4095	3.8	

Vrl	Slope		Offset
Mean	218.58	Mean	3276.98
Stdev	0.1748722	Stdev	0.109990928
Average	218.58223	Average	3276.977872
	Dac #	Average voltage	
	0	-15.0	
	4095	3.7	

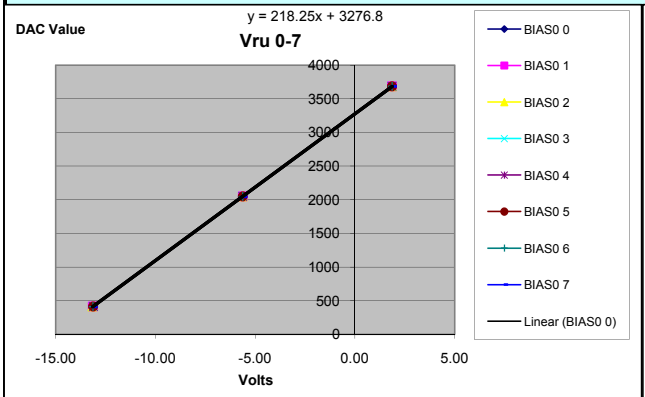
Vog	Slope		Offset
Mean	547.71	Mean	1358.11
Stdev	0.3026329	Stdev	0.984230161
Average	547.7117	Average	1358.111134
	Dac #	Average voltage	
	0	-2.5	
	4095	5.0	

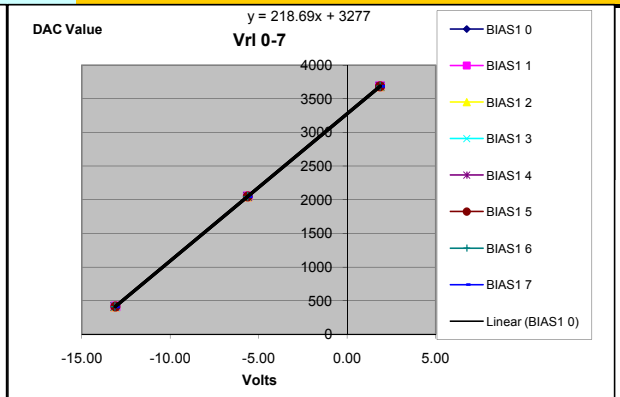
Vdd	Slope		Offset
Mean	131.57	Mean	3273.44
Stdev	0.2765078	Stdev	0.311142141
Average	131.57345	Average	3273.437136
	Dac #	Average voltage	
	0	-24.9	
	4095	6.3	

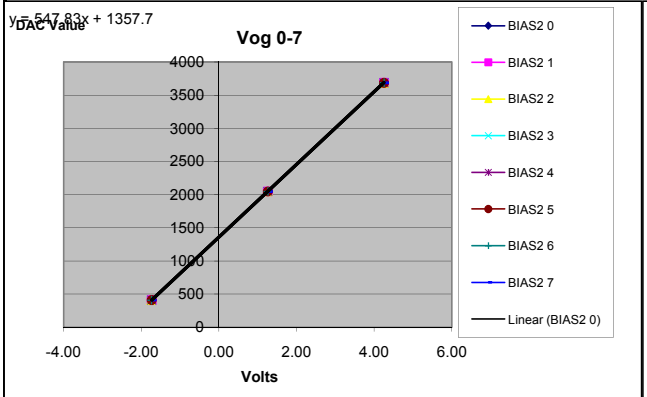
Notes and Observations

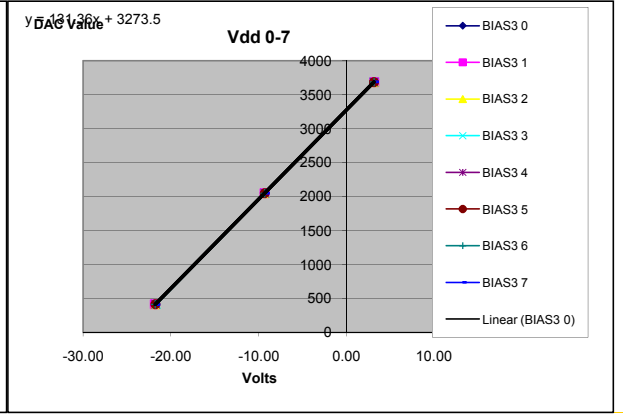
Checked for oscillations using a Agilent Oscilloscpe on AC.**OK**

average min & max voltages
(dac# -offset)/slope=voltage









Stage 8B. Telemetry System Tests - Table 7 (Bias Telemetry Tests)

DAC Value: 410 / 3686

Signal	Telemetry Return Values 10%	90%	Bias Signals Set Volts 10%	90%	Resolved Values for Telemetry Channel Slope	Offset
Vru 0	-1729	424	-13.14	1.87	143.4377	155.77
Vru 1	-1733	424	-13.14	1.87	143.7042	155.27
Vru 2	-1738	425	-13.15	1.87	144.0080	155.71
Vru 3	-1733	425	-13.13	1.87	143.8667	155.97
Vru 4	-1732	424	-13.11	1.87	143.9252	154.86
Vru 5	-1731	424	-13.13	1.87	143.6667	155.34
Vru 6	-1733	424	-13.13	1.87	143.8000	155.09
Vru 7	-1729	424	-13.13	1.87	143.5333	155.59
Vrl 0	-1737	424	-13.11	1.87	144.2590	154.24
Vrl 1	-1735	424	-13.11	1.87	144.1255	154.49
Vrl 2	-1737	424	-13.12	1.87	144.1628	154.42
Vrl 3	-1736	424	-13.10	1.87	144.2886	154.18
Vrl 4	-1735	424	-13.14	1.87	143.8374	155.02
Vrl 5	-1736	424	-13.11	1.87	144.1923	154.36
Vrl 6	-1740	424	-13.12	1.87	144.3629	154.04
Vrl 7	-1738	424	-13.13	1.87	144.1333	154.47
Vog 0	-359	868	-1.73	4.25	205.1839	-4.03
Vog 1	-358	868	-1.73	4.25	205.0167	-3.32
Vog 2	-359	868	-1.74	4.25	204.8414	-2.58
Vog 3	-358	868	-1.73	4.25	205.0167	-3.32
Vog 4	-358	868	-1.73	4.25	205.0167	-3.32
Vog 5	-358	868	-1.73	4.25	205.0167	-3.32
Vog 6	-358	868	-1.73	4.25	205.0167	-3.32
Vog 7	-358	868	-1.73	4.25	205.0167	-3.32
Vdd 0	-1690	575	-21.80	3.14	90.8180	289.83
Vdd 1	-1688	576	-21.84	3.15	90.5962	290.62
Vdd 2	-1678	575	-21.75	3.13	90.5547	291.56
Vdd 3	-1680	574	-21.68	3.12	90.8871	290.43
Vdd 4	-1678	574	-21.73	3.13	90.5873	290.46
Vdd 5	-1681	575	-21.77	3.14	90.5660	290.62
Vdd 6	-1672	575	-21.77	3.14	90.2047	291.76
Vdd 7	-1687	576	-21.76	3.14	90.8835	290.63

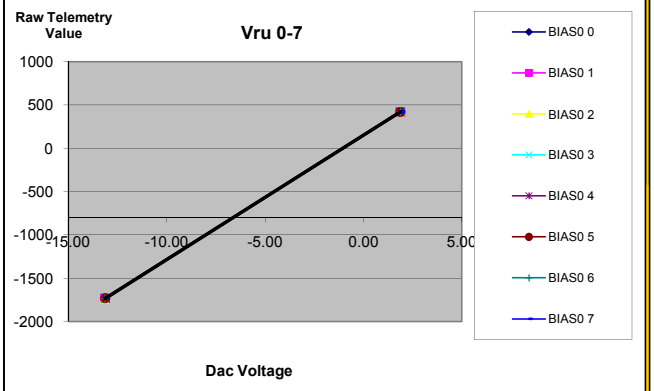
AVERAGE

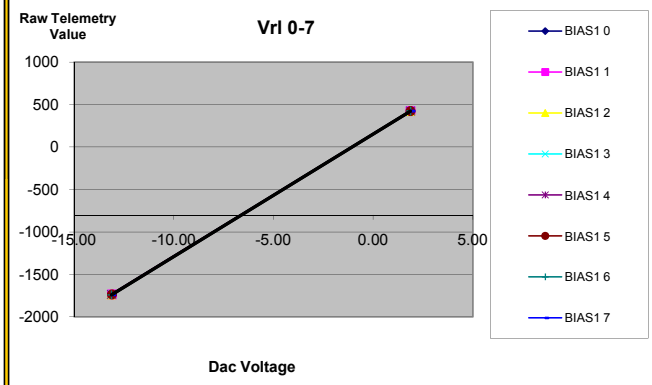
Vru	Slope		Offset
Mean	143.74	Mean	155.45
Stdev	0.1825055	Stdev	0.3493153

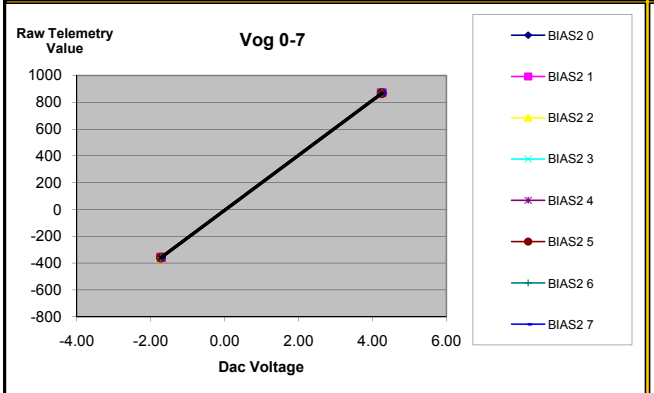
Vrl	Slope		Offset
Mean	144.17	Mean	154.40
Stdev	0.1473364	Stdev	0.2755191

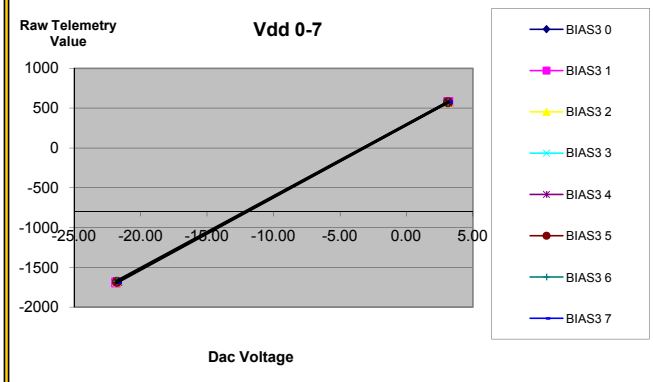
Vog	Slope		Offset
Mean	205.02	Mean	-3.32
Stdev	0.085654	Stdev	0.3640294

Vdd	Slope		Offset
Mean	90.64	Mean	290.74
Stdev	0.2118	Stdev	0.5864585









Stage 8C. Bias Voltage output enables testing - Table 8

Place a line through Bias Voltage name if enable/disable switch works

Vru 0	Vru 1	Vru 2	Vru 3	Vru 4	Vru 5
Vrl 0	Vrl 1	Vrl 2	Vrl 3	Vrl 4	Vrl 5
Vog 0	Vog 1	Vog 2	Vog 3	Vog 4	Vog 5
Vdd 0	Vdd 1	Vdd 2	Vdd 3	Vdd 4	Vdd 5

Stage 9. Vsub and Heater Control testing - Table 9

DAC Value	Vsub Measured Voltage Test Data 10%	50%	90%
Signal	volts	volts	volts
Vsub - rate	-1.23	3.77	8.78
Vsub - Limit	-1.23	3.77	8.78
Vsub0	0.00	0.00	0.00
	Vsub Enable Bit - pass		

DAC Value	Telemetery Readback Test Data 10%	50%	90%
Signal	dec	dec	dec
Vbias 0	154	302	681
Vbias 1	-23	697	1416
RTD1	221	NA	NA
RTD2	249	NA	NA
RTD3	275	NA	NA
RTD4	301	NA	NA
RTD5	326	NA	NA
RTD6	352	NA	NA
Reference 4096	836	NA	NA
eference buffere	836	NA	NA

Stage 10. Video Offset DAC Tests - Table 10.

	DAC Value 410				DAC Value 2048				DAC Value 3686			
ADC	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU
0	0.250	NA	NA	17275	1.250		NA	81206	2.250	NA	500ms	145133
1	0.250	NA	NA	16996	1.250		NA	81060	2.250	NA	500ms	145122
2	0.250	NA	NA	17165	1.250		NA	81165	2.250	NA	500ms	145168
3	0.250	NA	NA	16870	1.250		NA	80940	2.250	NA	500ms	145007
4	0.250	NA	NA	16931	1.250		NA	80964	2.250	NA	500ms	144992
5	0.250	NA	NA	17119	1.250		NA	81144	2.250	NA	500ms	145169
6	0.250	NA	NA	17123	1.250		NA	81172	2.250	NA	500ms	145231
7	0.250	NA	NA	17234	1.250		NA	81212	2.250	NA	500ms	145188
8	0.250	NA	NA	16951	1.250		NA	81002	2.250	NA	500ms	145056
9	0.250	NA	NA	17087	1.250		NA	81104	2.250	NA	500ms	145123
10	0.250	NA	NA	16874	1.250		NA	81003	2.250	NA	500ms	145128
11	0.250	NA	NA	16984	1.250		NA	81033	2.250	NA	500ms	145089

ADC	DC Volts		Data Set		
Channel	Slope	Offset	410	2048	3686
0	1638.000	0.500	0.250	1.250	2.250
1	1638.000	0.500	0.250	1.250	2.250
2	1638.000	0.500	0.250	1.250	2.250
3	1638.000	0.500	0.250	1.250	2.250
4	1638.000	0.500	0.250	1.250	2.250
5	1638.000	0.500	0.250	1.250	2.250
6	1638.000	0.500	0.250	1.250	2.250
7	1638.000	0.500	0.250	1.250	2.250
8	1638.000	0.500	0.250	1.250	2.250
9	1638.000	0.500	0.250	1.250	2.250
10	1638.000	0.500	0.250	1.250	2.250
11	1638.000	0.500	0.250	1.250	2.250

(dac# -offset)/slope=Voltage

ADC	ADU's		Data Set		
Channel	Slope	Offset	410	2048	3686
0	0.026	-32.64	17275	81206	145133
1	0.026	-24.57	16996	81060	145122
2	0.026	-29.29	17165	81165	145168
3	0.026	-21.32	16870	80940	145007
4	0.026	-23.14	16931	80964	144992
5	0.026	-27.97	17119	81144	145169
6	0.026	-27.83	17123	81172	145231
7	0.026	-31.25	17234	81212	145188
8	0.026	-23.47	16951	81002	145056
9	0.026	-27.19	17087	81104	145123
10	0.026	-21.03	16874	81003	145128
11	0.026	-24.30	16984	81033	145089

(dac# -offset)/slope=ADU

Notes and Observations

Checked for oscillations using a Agilent Oscilloscope on AC. OK

Stage 11. CDS Control Functions and Video Channel Performanc

TEST #1: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit is held static. The purpose of this test is to verify the correct operation of the ADC devices and measure the noise of the Offset voltage generators, ADC buffer amplifiers and ADC devices

Noise Test 1

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	81202	8.12E+04	81210.8	2.24622
CH 1	81057	8.11E+04	81065.7	2.29251
CH 2	81162	8.12E+04	81170.8	2.19405
CH 3	80941	8.10E+04	80950.2	2.28987
CH 4	80959	8.10E+04	80967	2.1553
CH 5	81141	8.12E+04	81149.7	2.29678
CH 6	81170	8.12E+04	81178.4	2.30948
CH 7	81209	8.12E+04	81217.4	2.39963
CH 8	81000	8.10E+04	81009.7	2.26669
CH 9	81103	81121	81112.8	2.33712
CH 10	80998	81016	81007.6	2.399
CH 11	81031	81048	81039.9	2.38414

TEST #2: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the invert/non-invert and the DC Restore switches are held static.

Noise Test 2

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76380	7.64E+04	76390.9	2.75902
CH 1	76850	7.69E+04	76860.1	2.73195
CH 2	76562	7.66E+04	76572.6	2.74707
CH 3	76812	7.68E+04	76821.9	2.6866
CH 4	76136	7.62E+04	76146.8	2.77635
CH 5	77013	7.70E+04	77023.2	2.75319
CH 6	77032	7.71E+04	77041.7	2.68732
CH 7	77045	7.71E+04	77055	2.79636
CH 8	76425	7.64E+04	76434.9	2.79928
CH 9	77003	77023	77013	2.68778
CH 10	76394	76414	76403.7	2.95169
CH 11	76907	76928	76917.6	2.87306

TEST #3: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the DC Restore switch is held static.

Noise Test 3

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76371	7.64E+04	76381.4	3.01851
CH 1	76846	7.69E+04	76857.3	2.98496
CH 2	76561	7.66E+04	76574.2	2.99351
CH 3	76806	7.68E+04	76818.1	2.88114
CH 4	76132	7.62E+04	76143.2	2.94749
CH 5	77017	7.70E+04	77026.9	2.90521
CH 6	77027	7.71E+04	77041.6	2.89975
CH 7	77049	7.71E+04	77059.4	3.06414
CH 8	76417	7.64E+04	76426.8	3.01404
CH 9	77002	77026	77014.7	2.98887
CH 10	76400	76421	76410.7	3.00592
CH 11	76909	76931	76920.7	3.09934

TEST #4: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition.

Noise Test 4

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76363	7.64E+04	76374.1	3.03626
CH 1	76849	7.69E+04	76860.8	3.15782
CH 2	76568	7.66E+04	76578	3.02126
CH 3	76806	7.68E+04	76818.1	3.00409
CH 4	76173	7.62E+04	76183.3	2.96303
CH 5	77005	7.70E+04	77016.3	3.20574
CH 6	77037	7.71E+04	77047.3	3.01201
CH 7	77019	7.70E+04	77030.1	3.06881
CH 8	76455	7.65E+04	76468.4	2.9278
CH 9	76920	76947	76935.9	3.17025
CH 10	76416	76439	76427	3.14677
CH 11	76873	76895	76884.1	3.22678

TEST #5: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the circuitry set to high GAIN.

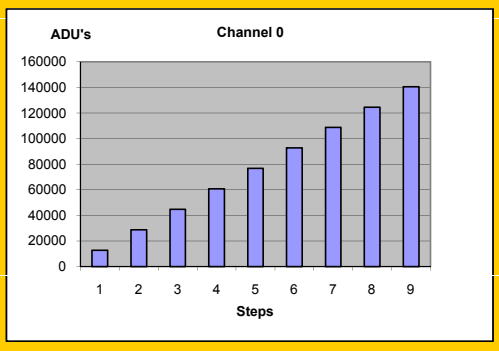
Noise Test 5

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76371	7.64E+04	76383.8	3.70517
CH 1	76861	7.69E+04	76874.4	3.69274
CH 2	76584	7.66E+04	76596.5	3.5143
CH 3	76813	7.68E+04	76825.2	3.57146
CH 4	76174	7.62E+04	76186.9	3.62625
CH 5	77001	7.70E+04	77015.2	3.66634
CH 6	77036	7.71E+04	77048.7	3.61849
CH 7	77017	7.70E+04	77030.6	3.59756
CH 8	76508	7.65E+04	76521.2	3.60959
CH 9	76923	76950	76936.6	3.67743
CH 10	76476	76503	76489.8	3.64843
CH 11	76871	76897	76884.7	3.85903

TEST #6A: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

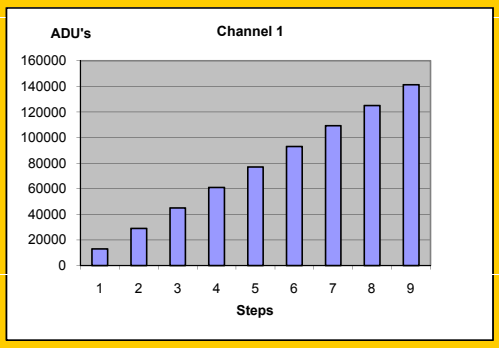
BrdTst6_006 / Channel 0					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12740	12764	12752.3	3.10712	10%
0x333	28704	28725	28713.6	3.16344	20%
0x4cc	44667	44690	44677.9	3.14215	30%
0x666	60666	60688	60677.9	2.97878	40%
0x800	76666	76690	76678.3	2.98495	50%
0x999	92629	92654	92641.4	3.16061	60%
0xb33	108630	108654	108642	3.11507	70%
0xccc	124598	124621	124609	2.99179	80%
0xe66	140599	140622	140609	3.09096	90%



TEST #6B: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

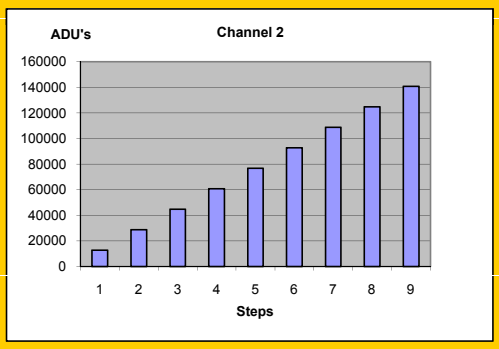
BrdTst6_006 / Channel 1					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13038	13062	13049.9	3.20406	10%
0x333	29034	29058	29045.4	3.29808	20%
0x4cc	45027	45052	45039.6	3.21623	30%
0x666	61063	61084	61074	3.02159	40%
0x800	77096	77121	77109.1	3.31753	50%
0x999	93093	93117	93107	2.99009	60%
0xb33	109129	109151	109141	3.20243	70%
0xccc	125125	125149	125137	3.17512	80%
0xe66	141159	141182	141171	3.02158	90%



TEST #6C: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

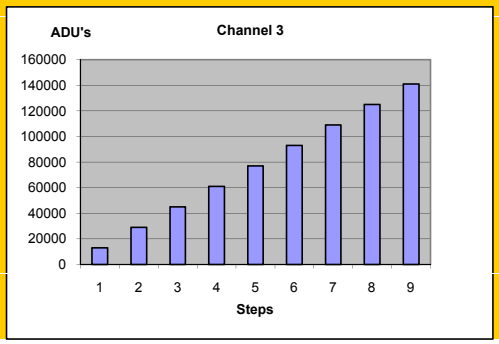
BrdTst6_006 / Channel 2					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12863	12884	12872.9	3.03188	10%
0x333	28844	28866	28854.1	3.01471	20%
0x4cc	44824	44846	44835.1	3.07631	30%
0x666	60844	60864	60853.8	2.98891	40%
0x800	76862	76883	76872.4	3.01661	50%
0x999	92845	92864	92855.2	3.03518	60%
0xb33	108865	108885	108875	3.09938	70%
0xccc	124847	124868	124858	3.01611	80%
0xe66	140868	140889	140878	3.03481	90%



TEST #6D: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

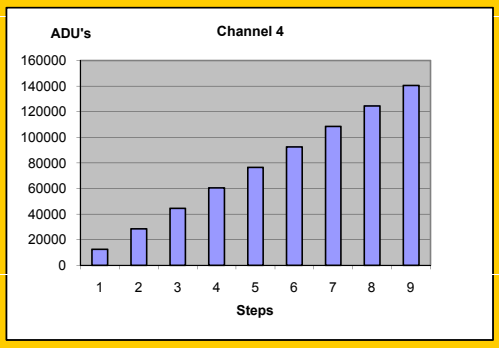
BrdTst6_006 / Channel 3					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12970	12992	12981.3	3.18117	10%
0x333	28969	28993	28980.5	3.05264	20%
0x4cc	44966	44988	44976.1	3.15327	30%
0x666	61003	61027	61013.5	3.14741	40%
0x800	77037	77060	77048.1	3.17191	50%
0x999	93036	93058	93046.3	3.10933	60%
0xb33	109072	109094	109084	3.11401	70%
0xccc	125072	125094	125084	3.14472	80%
0xe66	141111	141135	141121	3.09037	90%



TEST #6E: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

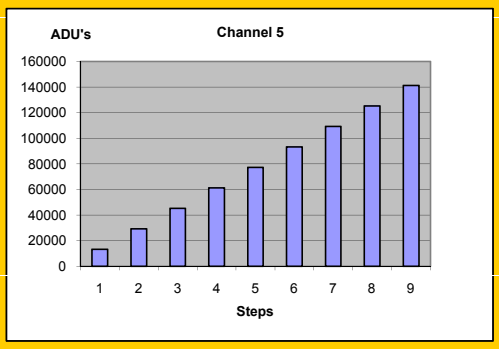
BrdTst6_006 / Channel 4					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12435	12459	12447	3.10802	10%
0x333	28426	28451	28435.7	3.16962	20%
0x4cc	44410	44432	44421.3	3.14655	30%
0x666	60438	60461	60449.6	2.92766	40%
0x800	76463	76485	76474.3	3.07812	50%
0x999	92452	92474	92462.9	3.1164	60%
0xb33	108481	108504	108491	3.12667	70%
0xccc	124467	124491	124479	3.18324	80%
0xe66	140498	140518	140508	3.1616	90%



TEST #6F: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

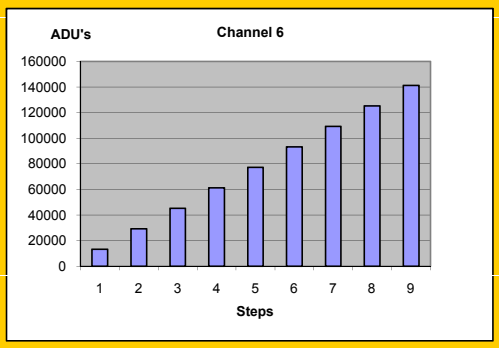
BrdTst6_006 / Channel 5					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13237	13260	13247.6	3.22843	10%
0x333	29225	29249	29235.6	3.22466	20%
0x4cc	45209	45232	45219.9	3.09587	30%
0x666	61233	61258	61245.3	3.20263	40%
0x800	77253	77278	77266.2	3.31136	50%
0x999	93241	93264	93253.2	3.09675	60%
0xb33	109270	109292	109280	3.1603	70%
0xccc	125255	125277	125265	3.06197	80%
0xe66	141281	141303	141292	3.18632	90%



TEST #6G: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

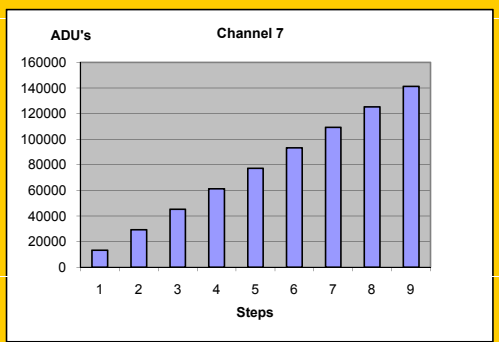
BrdTst6_006 / Channel 6					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13221	13241	13231.6	3.0611	10%
0x333	29214	29237	29225.3	3.1036	20%
0x4cc	45206	45229	45217.4	2.95596	30%
0x666	61239	61262	61249.9	2.9768	40%
0x800	77271	77295	77282.8	3.11612	50%
0x999	93266	93288	93277.1	3.10427	60%
0xb33	109299	109323	109311	3.1502	70%
0xccc	125292	125318	125306	3.1385	80%
0xe66	141326	141349	141339	3.09386	90%



TEST #6H: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

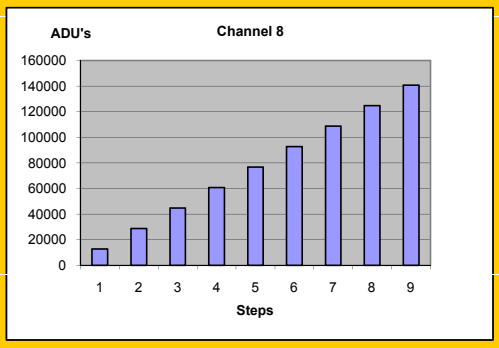
BrdTst6_006 / Channel 7					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13279	13301	13290.1	3.17575	10%
0x333	29254	29278	29266.8	3.32607	20%
0x4cc	45227	45250	45237.5	3.01297	30%
0x666	61241	61263	61251.9	3.04829	40%
0x800	77250	77277	77261.7	3.21421	50%
0x999	93225	93248	93236.3	3.04113	60%
0xb33	109239	109264	109253	3.16659	70%
0xccc	125215	125236	125226	3.19096	80%
0xe66	141231	141251	141241	3.14126	90%



TEST #6I: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

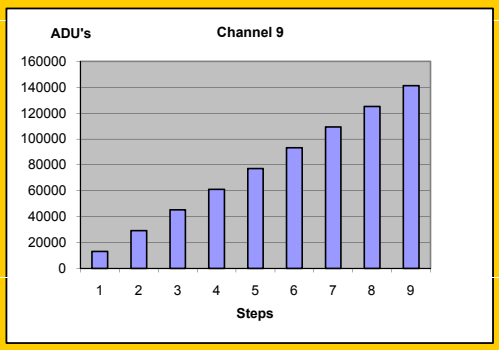
BrdTst6_006 / Channel 8					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12675	12700	12687.9	3.20235	10%
0x333	28671	28694	28682.1	3.16208	20%
0x4cc	44662	44684	44674	2.97939	30%
0x666	60696	60718	60707.5	2.98429	40%
0x800	76729	76751	76738.5	3.01918	50%
0x999	92722	92744	92733.9	3.05987	60%
0xb33	108754	108778	108767	3.11802	70%
0xccc	124749	124772	124761	3.12636	80%
0xe66	140785	140807	140795	3.1998	90%



TEST #6J: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

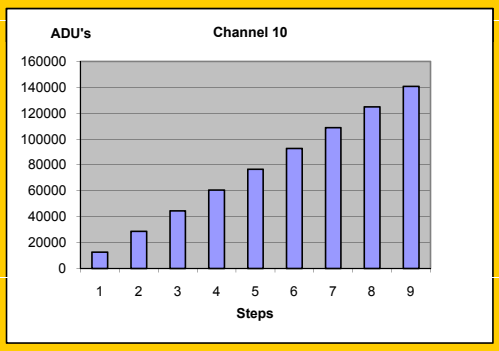
BrdTst6_006 / Channel 9					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13174	13197	13186	3.04591	10%
0x333	29160	29182	29171.4	3.10608	20%
0x4cc	45141	45166	45154.1	3.22257	30%
0x666	61166	61190	61179.1	3.20186	40%
0x800	77196	77218	77206.4	3.11328	50%
0x999	93180	93204	93193	3.18931	60%
0xb33	109209	109231	109220	3.02889	70%
0xccc	125193	125218	125205	3.11613	80%
0xe66	141219	141241	141229	3.16262	90%



TEST #6K: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

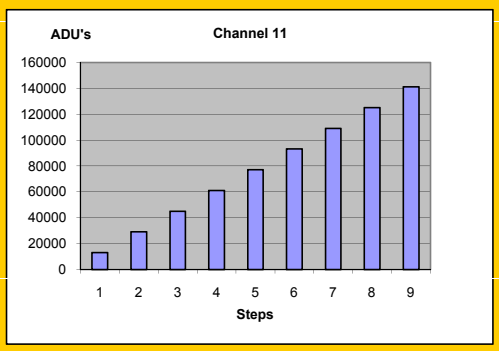
BrdTst6_006 / Channel 10					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12569	12590	12579.6	2.96792	10%
0x333	28582	28603	28592.1	3.21607	20%
0x4cc	44590	44612	44601.3	3.18398	30%
0x666	60642	60664	60652.9	3.17001	40%
0x800	76693	76715	76704.8	3.05025	50%
0x999	92706	92732	92719.1	3.19454	60%
0xb33	108761	108785	108772	3.15429	70%
0xccc	124770	124796	124783	3.14338	80%
0xe66	140826	140847	140836	3.03624	90%



TEST #6L: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

BrdTst6_006 / Channel 11					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13089	13114	13102	3.13825	10%
0x333	29084	29109	29096.4	3.21536	20%
0x4cc	45076	45099	45086.7	3.21424	30%
0x666	61108	61133	61120.1	3.2913	40%
0x800	77145	77166	77155.1	3.00833	50%
0x999	93136	93160	93147.4	3.21172	60%
0xb33	109169	109193	109182	3.25517	70%
0xccc	125164	125185	125175	3.17394	80%
0xe66	141197	141219	141208	3.19178	90%



Stage 13. Other Bit Tests. Table 11

Electronic Serial Number	0xDB8EC0		Board Serial Number	22
Firmware Version	0x193		Name Of Person Testing	S. Holm
Ident Register	0x502		Board passed Functional Tests	YES