DES 12 Channel Board - Functional Tests: CCD Acquisition Board Revision 1.0

Stage 1. Preparation of documentation and configuration settings - Table 1.

Board Part Number	26		Board Serial Number	0xDB6FA8
Date Of Tests	August 2010		Name Of Person Testing	S. Holm
Suggested Filename To Save	CCDACQ_12Ch_REPORT_BOARD12.xl		Sequence number: Test	

Stage 3. Power plane short test - Table 2.

Supply Name	Short test to ground: Impedance to ground	Test Point	
+1.2VD	57.00	TP43	~50 ohms
+1.8VD	2.5M	TPB12	> 1K ohm
+2.5VD	18K	TPB11	> 1K ohm
+3.3VD	5K	D13	> 1K ohm
+5VD	18K	D14	> 1K ohm
+5VA	4M	C267	> 1K ohm
-5VA	300K	C270	> 1K ohm
+15VA	500K	C288	> 1K ohm
-15VA	500K	C282	> 1K ohm
-28VA	2.5M	C307	> 1K ohm

Stage 4. Firmware programming tests - Table 3.

JTAG Order	Designator	Device	Load File	Check Sum or User Code
1	U122	XCF08PFS48C PROM	CcdAcqFpgaV41.mcs	0014ef670
2	U114	Spartan3 XC3S2000 FPGA	ccdacqfpgav41.bit	5102801

Stage 5. Power Consumption - Table 4.

Supply Name	Power Supply Consumption: Measured Voltage at test point	Measured Current on power supply	Test Point	
+1.2VD	1.20	N/A	TP43	
+1.8VD	1.81	N/A	TPB12	
+2.5VD	2.50	N/A	TPB11	
+3.3VD	3.29	0.167	D13	
+5VD	5.20	0.157	D14	
+5VA	4.85	0.622	C267	
-5VA	-5.00	0.433	C270	
+15VA	14.95	0.558	C288	
-15VA	-15.07	0.405	C282	
-28VA	-27.87	0.21	C307	
Vref 0+	10.02	N/A	R534	Vsub+ Reference(+10v)
Vref 0-	-2.49	N/A	R525	Vsub - Reference(-2.5v)
Vref Offset	2.50	N/A	R573	ADC Offset Reference(+2.5v)
Vclamp	1.87	N/A	VIA	ADC Clamp Voltage(+1.8v)
ADC Ref.	2.50	N/A	VIA	ADC Reference Voltage(+2.5v)
Vref 1+	2.50	N/A	R537	Vru and Vrl + Reference(+2.5v)
Vref 1-	-9.99	N/A	R535	Vru and Vrl - Reference(-10v)
Vref 2+	4.99	N/A	R563	Vog + Reference(+5v)
Vref 2-	-2.49	N/A	R555	Vog - Reference(-2.5v)
Vref 3+	2.50	N/A	R543	Vdd + Reference(+2.5v)
Vref 3-	-10.00	N/A	R571	Vdd - Reference(-10v)

Power Dissipation:
26.8 Watts

~27 watts +/- 5%

Stage 7. Basic Bus Transactions - **D**igital **Register** Tests - Table 5.

Register name	Put an X on any bit that has an error: 31-24	23-16	15-08	07-00	Function	Test name: Pattern	Walking 0's	Walking 1's
CDS Control			00000000	00000000	16 bit R/W			
Digital Output	00000000	00000000	00000000	00000000	32 bit R/W			
ADC Config.			0000	00000000	12 bit R/W			
Offset DAC			0000	00000000	12 bit R/W			
Bias DAC			0000	00000000	12 bit R/W			
Telemetry Config.				0000	4 bit R/W			
Auxilary Config.			00	00000000	10 bit R/W			
Redirect				0000	4 bit R/W			
Pixel Transfer				00000000	8 bit R/W			
Micro SEQ			00000000	00000000	16 bit R/W			
RAM Buffer			00000000	00000000	16 bit R/W			
LED Control				0000	4 bit R/W			
Control			00000000	00000000	16 bit R/W			
All Register Test	00000000	00000000	00000000	00000000	16 bit R/W	**Passed**	**Passed**	**Passed**

Stage 8. Bias Voltage settings and output enables testing - Table 8

DAC Value	Bias Voltage Test Data 410	2048	3686	50% rms Noise	10-90% Rise Time			
Signal	volts	volts	volts	uV	millisec.	Fanout Brd	Slope	Offset
Vru 0	-13.12	-5.62	1.88	<10	1	BIAS 3	218.40	3275.41
Vru 1	-13.12	-5.62	1.88	<10	1	BIAS 4	218.40	3275.41
Vru 2	-13.10	-5.61	1.88	<10	1	BIAS 5	218.69	3274.86
Vru 3	-13.13	-5.63	1.88	<10	1	BIAS 6	218.25	3276.05
Vru 4	-13.11	-5.62	1.88	<10	1	BIAS 7	218.55	3275.50
Vru 5	-13.13	-5.62	1.88	<10	1	BIAS 8	218.25	3275.32
Vru 6	-13.12	-5.62	1.88	NA	NA	BIAS 9	218.40	3275.41
Vru 7	-13.13	-5.62	1.88	NA	NA	BIAS 10	218.25	3275.32
Vrl 0	-13.11	-5.62	1.88	<10	1	BIAS 11	218.55	3275.50
Vrl 1	-13.11	-5.62	1.88	<10	1	BIAS 12	218.55	3275.50
Vrl 2	-13.12	-5.62	1.88	<10	1	BIAS 13	218.40	3275.41
Vrl 3	-13.13	-5.62	1.88	<10	1	BIAS 14	218.25	3275.32
Vrl 4	-13.12	-5.62	1.88	<10	1	BIAS 15	218.40	3275.41
Vrl 5	-13.10	-5.62	1.88	<10	1	BIAS 16	218.69	3275.59
Vrl 6	-13.11	-5.62	1.88	NA	NA	BIAS 17	218.55	3275.50
Vrl 7	-13.09	-5.62	1.88	NA	NA	BIAS 18	218.84	3275.68
Vog 0	-1.74	1.25	4.24	<10	1	BIAS 19	547.83	1363.22
Vog 1	-1.74	1.25	4.24	<10	1	BIAS 20	547.83	1363.22
Vog 2	-1.74	1.25	4.24	<10	1	BIAS 21	547.83	1363.22
Vog 3	-1.74	1.25	4.24	<10	1	BIAS 22	547.83	1363.22
Vog 4	-1.74	1.25	4.24	<10	1	BIAS 23	547.83	1363.22
Vog 5	-1.74	1.25	4.24	<10	1	BIAS 24	547.83	1363.22
Vog 6	-1.74	1.25	4.24	NA	NA	BIAS 25	547.83	1363.22
Vog 7	-1.74	1.25	4.24	NA	NA	BIAS 26	547.83	1363.22
Vdd 0	-21.85	-9.37	3.12	<10	20	BIAS 27	131.20	3276.88
Vdd 1	-21.88	-9.39	3.12	<10	20	BIAS 28	131.04	3277.59
Vdd 2	-21.92	-9.40	3.12	<10	20	BIAS 29	130.83	3277.81
Vdd 3	-21.88	-9.38	3.12	<10	20	BIAS 30	131.04	3277.16
Vdd 4	-21.84	-9.37	3.12	<10	20	BIAS 21	131.25	3276.94
Vdd 5	-21.96	-9.42	3.12	<10	20	BIAS 32	130.62	3278.46
Vdd 6	-21.89	-9.39	3.12	NA	NA	BIAS 33	130.99	3277.54
Vdd 7	-21.90	-9.39	3.12	NA	NA	BIAS 34	130.94	3277.48

Vru	Slope		Offset
Mean	218.40	Mean	3275.41
Stdev	0.145681	Stdev	0.302262563
Average	218.40008	Average	3275.407787
	Dac #	Average voltage	
	0	-14.0	
	4095	3.8	

Vrl	Slope		Offset
Mean	218.53	Mean	3275.49
Stdev	0.1699118	Stdev	0.104960155
Average	218.52754	Average	3275.486728
	Dac #	Average voltage	
	0	-15.0	
	4095	3.8	

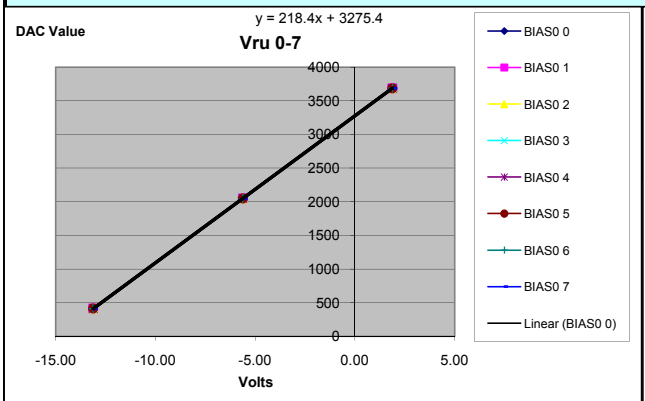
Vog	Slope		Offset
Mean	547.83	Mean	1363.22
Stdev	0	Stdev	0
Average	547.82609	Average	1363.217391
	Dac #	Average voltage	
	0	-2.5	
	4095	5.0	

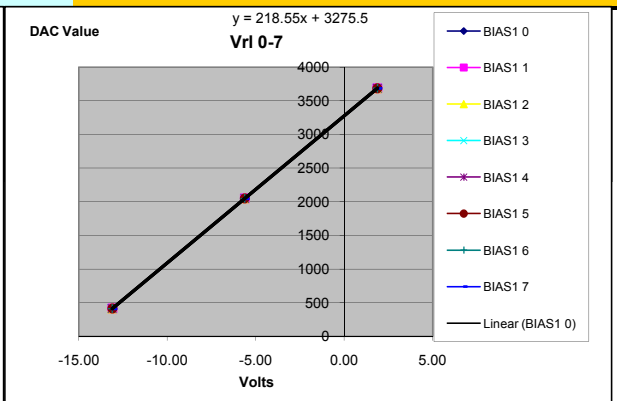
Vdd	Slope		Offset
Mean	130.99	Mean	3277.48
Stdev	0.1868753	Stdev	0.479525947
Average	130.98786	Average	3277.481667
	Dac #	Average voltage	
	0	-25.0	
	4095	6.2	

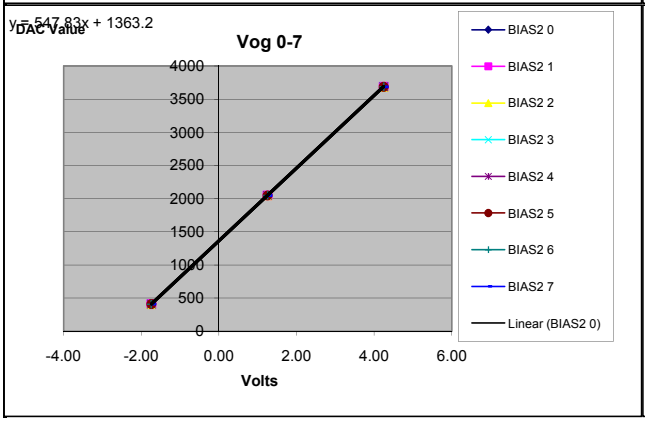
Notes and Observations

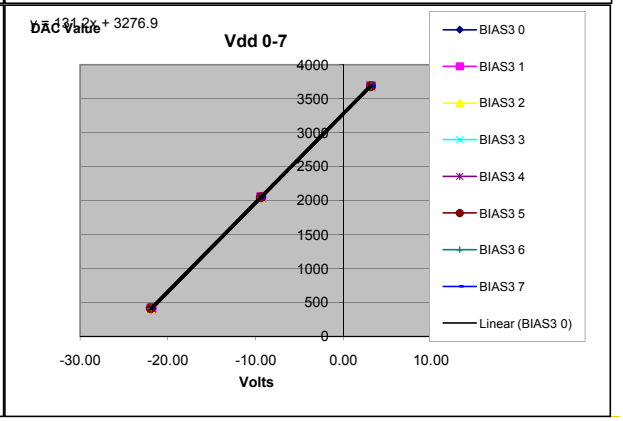
Checked for oscillations using a Agilent Oscilloscpe on AC.**OK**

average min & max voltages
(dac# -offset)/slope=voltage









Stage 8B. Telemetry System Tests - Table 7 (Bias Telemetry Tests)

DAC Value	410	3686	Bias Signals Set Volts		Resolved Values for Telemetry Channel	
	Telemetry Return Values					
Signal	10%	90%	10%	90%	Slope	Offset
Vru 0	-1756	424	-13.12	1.88	145.3333	150.77
Vru 1	-1757	423	-13.12	1.88	145.3333	149.77
Vru 2	-1754	423	-13.10	1.88	145.3271	149.79
Vru 3	-1758	424	-13.13	1.88	145.3698	150.70
Vru 4	-1757	423	-13.11	1.88	145.4303	149.59
Vru 5	-1757	424	-13.13	1.88	145.3031	150.83
Vru 6	-1762	423	-13.12	1.88	145.6667	149.15
Vru 7	-1760	423	-13.13	1.88	145.4364	149.58
Vrl 0	-1737	423	-13.11	1.88	144.0961	152.10
Vrl 1	-1734	423	-13.11	1.88	143.8959	152.48
Vrl 2	-1738	423	-13.12	1.88	144.0667	152.15
Vrl 3	-1736	423	-13.13	1.88	143.8374	152.59
Vrl 4	-1741	423	-13.12	1.88	144.2667	151.78
Vrl 5	-1741	423	-13.10	1.88	144.4593	151.42
Vrl 6	-1744	422	-13.11	1.88	144.4963	150.35
Vrl 7	-1745	423	-13.09	1.88	144.8230	150.73
Vog 0	-361	867	-1.74	4.24	205.3512	-3.69
Vog 1	-360	867	-1.74	4.24	205.1839	-2.98
Vog 2	-361	867	-1.74	4.24	205.3512	-3.69
Vog 3	-360	867	-1.74	4.24	205.1839	-2.98
Vog 4	-361	867	-1.74	4.24	205.3512	-3.69
Vog 5	-361	867	-1.74	4.24	205.3512	-3.69
Vog 6	-361	866	-1.74	4.24	205.1839	-3.98
Vog 7	-361	867	-1.74	4.24	205.3512	-3.69
Vdd 0	-1709	574	-21.85	3.12	91.4297	288.74
Vdd 1	-1715	574	-21.88	3.12	91.5600	288.33
Vdd 2	-1722	575	-21.92	3.12	91.7332	288.79
Vdd 3	-1713	574	-21.88	3.12	91.4800	288.58
Vdd 4	-1713	574	-21.84	3.12	91.6266	288.13
Vdd 5	-1726	576	-21.96	3.12	91.7863	289.63
Vdd 6	-1721	574	-21.89	3.12	91.7633	287.70
Vdd 7	-1726	575	-21.90	3.12	91.9664	288.06

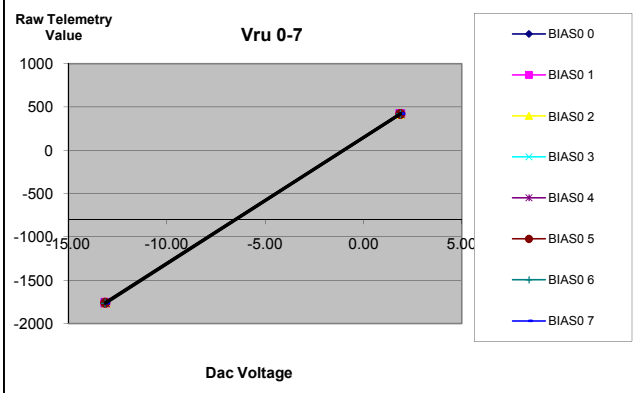
AVERAGE

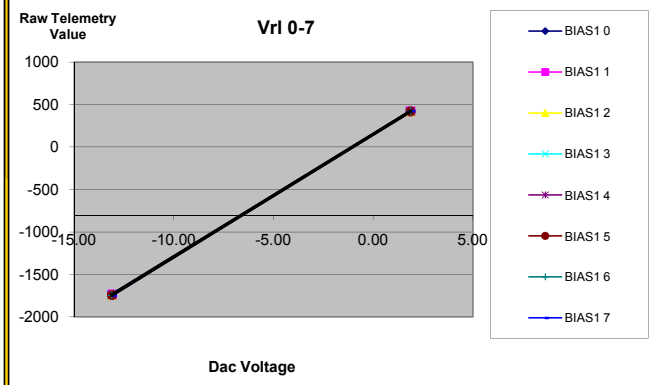
Vru	Slope		Offset
Mean	145.40	Mean	150.02
Stdev	0.1105966	Stdev	0.6071911

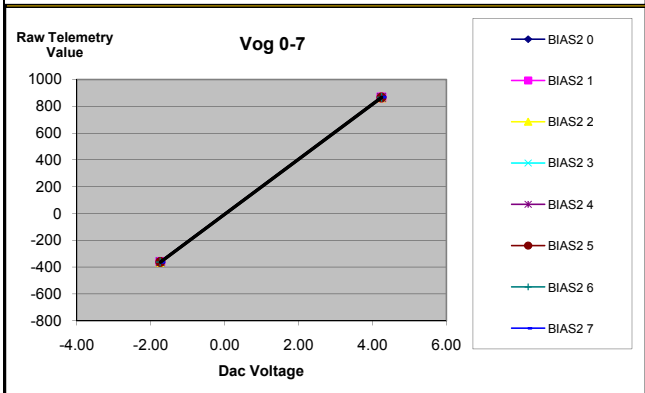
Vrl	Slope		Offset
Mean	144.24	Mean	151.70
Stdev	0.3133502	Stdev	0.7587045

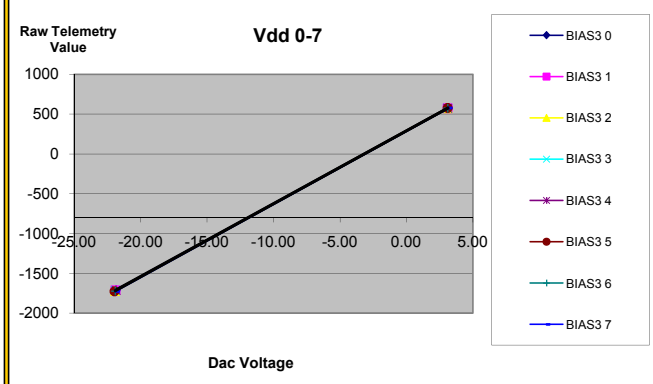
Vog	Slope		Offset
Mean	205.29	Mean	-3.55
Stdev	0.080957	Stdev	0.3411963

Vdd	Slope		Offset
Mean	91.67	Mean	288.50
Stdev	0.1665406	Stdev	0.54993









Stage 8C. Bias Voltage output enables testing - Table 8

Place a line through Bias Voltage name if enable/disable switch works

Vru 0	Vru 1	Vru 2	Vru 3	Vru 4	Vru 5
Vrl 0	Vrl 1	Vrl 2	Vrl 3	Vrl 4	Vrl 5
Vog 0	Vog 1	Vog 2	Vog 3	Vog 4	Vog 5
Vdd 0	Vdd 1	Vdd 2	Vdd 3	Vdd 4	Vdd 5

Stage 9. Vsub and Heater Control testing - Table 9

DAC Value	Vsub Measured Voltage Test Data 10%	50%	90%
Signal	volts	volts	volts
Vsub - rate	-1.24	3.76	8.74
Vsub - Limit	-1.24	3.76	8.74
Vsub0	0.00	0.00	0.00
	Vsub Enable Bit - pass		

DAC Value	Telemetery Readback Test Data 10%	50%	90%
Signal	dec	dec	dec
Vbias 0	153	271	452
Vbias 1	-27	694	1415
RTD1	219	NA	NA
RTD2	249	NA	NA
RTD3	275	NA	NA
RTD4	303	NA	NA
RTD5	324	NA	NA
RTD6	350	NA	NA
Reference 4096	836	NA	NA
eference buffere	836	NA	NA

Stage 10. Video Offset DAC Tests - Table 10.

	DAC Value 410				DAC Value 2048				DAC Value 3686			
ADC	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU
0	0.250	NA	NA	16944	1.250		NA	81086	2.250	NA	500ms	145220
1	0.250	NA	NA	17046	1.250		NA	81117	2.250	NA	500ms	145183
2	0.250	NA	NA	17245	1.250		NA	81221	2.250	NA	500ms	145182
3	0.250	NA	NA	16905	1.250		NA	81074	2.250	NA	500ms	145221
4	0.250	NA	NA	16954	1.250		NA	81041	2.250	NA	500ms	145113
5	0.250	NA	NA	17078	1.250		NA	81123	2.250	NA	500ms	145164
6	0.250	NA	NA	17109	1.250		NA	81178	2.250	NA	500ms	145233
7	0.250	NA	NA	17176	1.250		NA	81166	2.250	NA	500ms	145141
8	0.250	NA	NA	16954	1.250		NA	81067	2.250	NA	500ms	145173
9	0.250	NA	NA	17110	1.250		NA	81147	2.250	NA	500ms	145181
10	0.250	NA	NA	16906	1.250		NA	81056	2.250	NA	500ms	145208
11	0.250	NA	NA	17022	1.250		NA	81063	2.250	NA	500ms	145105

145220

ADC	DC Volts		Data Set		
Channel	Slope	Offset	410	2048	3686
0	1638.000	0.500	0.250	1.250	2.250
1	1638.000	0.500	0.250	1.250	2.250
2	1638.000	0.500	0.250	1.250	2.250
3	1638.000	0.500	0.250	1.250	2.250
4	1638.000	0.500	0.250	1.250	2.250
5	1638.000	0.500	0.250	1.250	2.250
6	1638.000	0.500	0.250	1.250	2.250
7	1638.000	0.500	0.250	1.250	2.250
8	1638.000	0.500	0.250	1.250	2.250
9	1638.000	0.500	0.250	1.250	2.250
10	1638.000	0.500	0.250	1.250	2.250
11	1638.000	0.500	0.250	1.250	2.250

(dac# -offset)/slope=Voltage

ADC	ADU's		Data Set		
Channel	Slope	Offset	410	2048	3686
0	0.026	-22.76	16944	81086	145220
1	0.026	-25.83	17046	81117	145183
2	0.026	-31.65	17245	81221	145182
3	0.026	-21.69	16905	81074	145221
4	0.026	-23.44	16954	81041	145113
5	0.026	-26.81	17078	81123	145164
6	0.026	-26.78	17109	81178	145330
7	0.026	-30.08	17176	81166	145103
8	0.026	-23.63	16954	81067	145118
9	0.026	-27.29	17110	81147	145232
10	0.026	-22.02	16906	81056	145161
11	0.026	-25.06	17022	81063	145146

(dac# -offset)/slope=ADU

Notes and Observations

Checked for oscillations using a Agilent Oscilloscope on AC. OK

Stage 11. CDS Control Functions and Video Channel Performanc

TEST #1: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit is held static. The purpose of this test is to verify the correct operation of the ADC devices and measure the noise of the Offset voltage generators, ADC buffer amplifiers and ADC devices

Noise Test 1

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	81078	81095	81086.4	2.28705
CH 1	81110	81126	81117.9	2.32928
CH 2	81209	81228	81219.6	2.31946
CH 3	81064	81081	81071.6	2.3562
CH 4	81033	81048	81040.3	2.22091
CH 5	81114	81131	81122.6	2.30888
CH 6	81165	81182	81173.6	2.27056
CH 7	81156	81173	81165.6	2.35284
CH 8	81057	81074	81065.7	2.28333
CH 9	81141	81158	81149.4	2.36709
CH 10	81050	81067	81058.1	2.41919
CH 11	81056	81072	81064.5	2.3562

TEST #2: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the invert/non-invert and the DC Restore switches are held static.

Noise Test 2

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76449	76468	76458.9	2.80004
CH 1	76701	76721	76710.9	2.8069
CH 2	76597	76620	76608.4	2.83384
CH 3	77010	77032	77021.2	2.88438
CH 4	76206	76224	76215.4	2.75064
CH 5	76764	76782	76772.9	2.68472
CH 6	77096	77117	77107.7	2.72488
CH 7	76936	76957	76946.5	2.82866
CH 8	76521	76541	76530.3	2.70992
CH 9	77090	77109	77099.3	2.7906
CH 10	76494	76514	76503.7	2.87134
CH 11	76692	76712	76702.1	2.84697

TEST #3: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the DC Restore switch is held static.

Noise Test 3

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76447	76470	76458.4	3.03085
CH 1	76693	76716	76703	3.01005
CH 2	76586	76608	76596.6	2.83985
CH 3	77008	77030	77018.2	3.06146
CH 4	76201	76222	76212.6	2.96909
CH 5	76758	76783	76768.6	2.97399
CH 6	77096	77116	77106.2	2.96445
CH 7	76934	76954	76943.3	3.05766
CH 8	76523	76546	76533	2.99188
CH 9	77087	77109	77096.9	3.00287
CH 10	76496	76522	76508.4	3.12784
CH 11	76686	76707	76696.9	3.03195

TEST #4: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition.

Noise Test 4

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76441	76462	76450.7	2.9069
CH 1	76695	76717	76706.8	3.06613
CH 2	76588	76612	76600	3.17052
CH 3	77007	77030	77018	3.1945
CH 4	76235	76257	76247.4	3.00758
CH 5	76745	76770	76757	3.15089
CH 6	77107	77131	77117.5	3.27355
CH 7	76889	76911	76899.6	3.16286
CH 8	76562	76585	76573.7	3.1103
CH 9	77002	77025	77013.4	3.28808
CH 10	76513	76538	76526.9	3.20524
CH 11	76645	76668	76654.9	3.22347

TEST #5: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the circuitry set to high GAIN.

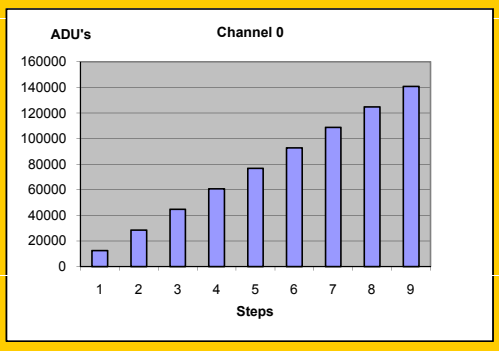
Noise Test 5

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76450	76475	76461.4	3.69553
CH 1	76704	76736	76719.2	3.6877
CH 2	76605	76631	76617.9	3.65156
CH 3	77011	77039	77024	3.61613
CH 4	76239	76265	76251.9	3.57073
CH 5	76743	76769	76755.8	3.70575
CH 6	77105	77133	77118.8	3.70361
CH 7	76887	76915	76900.8	3.67436
CH 8	76614	76640	76627.4	3.67929
CH 9	77000	77027	77012.8	3.7602
CH 10	76580	76604	76591	3.72494
CH 11	76643	76668	76655.1	3.75537

TEST #6A: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

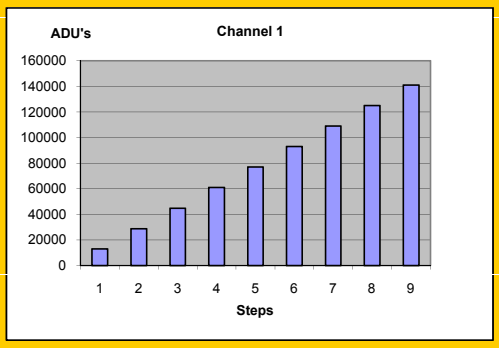
BrdTst6_006 / Channel 0					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12608	12630	12618.7	3.12824	10%
0x333	28621	28645	28632.1	3.10548	20%
0x4cc	44635	44657	44645.8	3.07796	30%
0x666	60687	60709	60697.2	3.13262	40%
0x800	76741	76764	76752	3.12695	50%
0x999	92754	92776	92764.4	3.06965	60%
0xb33	108805	108829	108817	3.19331	70%
0xccc	124822	124845	124833	3.04826	80%
0xe66	140874	140897	140886	3.14006	90%



TEST #6B: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

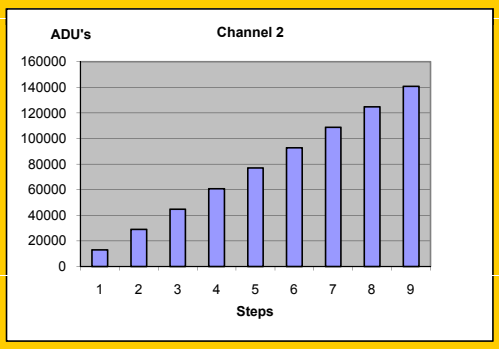
BrdTst6_006 / Channel 1					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12882	12903	12892.1	3.10241	10%
0x333	28873	28897	28884	3.17073	20%
0x4cc	44870	44893	44882	3.03034	30%
0x666	60900	60925	60913.3	3.12582	40%
0x800	76934	76959	76947.4	3.26438	50%
0x999	92932	92953	92943.6	3.06738	60%
0xb33	108965	108988	108976	3.07945	70%
0xccc	124965	124987	124976	3.08811	80%
0xe66	140999	141023	141011	3.06789	90%



TEST #6C: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

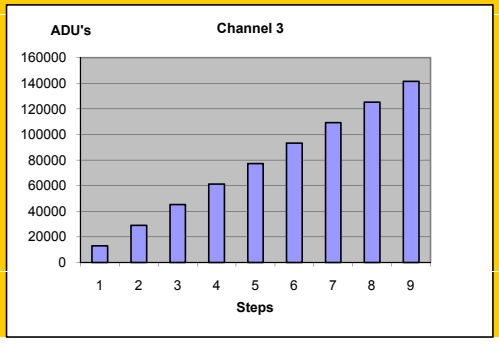
BrdTst6_006 / Channel 2					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12922	12943	12932.6	3.11051	10%
0x333	28892	28915	28903.1	3.11206	20%
0x4cc	44864	44887	44875.7	3.17777	30%
0x666	60873	60897	60885.1	3.1666	40%
0x800	76880	76903	76892.6	3.13294	50%
0x999	92855	92876	92865.5	2.98827	60%
0xb33	108864	108889	108875	3.17119	70%
0xccc	124840	124862	124851	3.14771	80%
0xe66	140850	140871	140860	3.11595	90%



TEST #6D: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

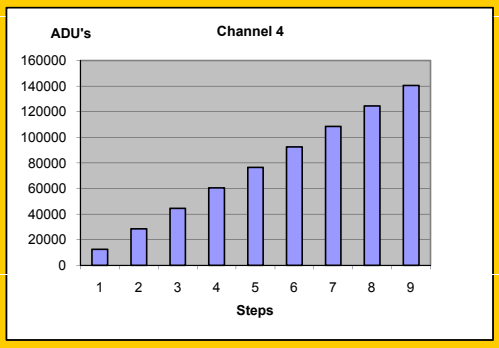
BrdTst6_006 / Channel 3					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13089	13115	13103.2	3.22274	10%
0x333	29108	29132	29119.8	3.13526	20%
0x4cc	45130	45153	45141.7	3.17725	30%
0x666	61185	61207	61197.1	3.17982	40%
0x800	77240	77263	77251.3	3.04571	50%
0x999	93257	93280	93268.7	3.0216	60%
0xb33	109312	109335	109326	3.15191	70%
0xccc	125340	125362	125351	3.13318	80%
0xe66	141397	141420	141408	3.21361	90%



TEST #6E: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

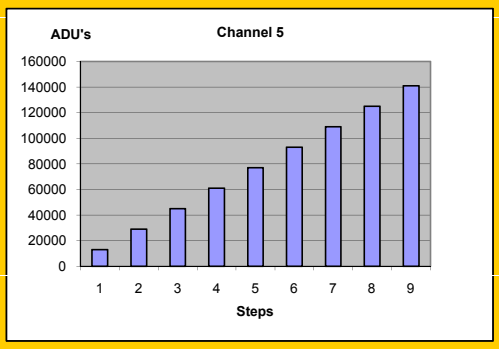
BrdTst6_006 / Channel 4					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12466	12489	12477.3	3.15037	10%
0x333	28466	28489	28477.1	3.11181	20%
0x4cc	44463	44484	44472.9	3.12275	30%
0x666	60500	60524	60511.4	3.05782	40%
0x800	76540	76561	76550.7	3.09624	50%
0x999	92540	92565	92552	3.18196	60%
0xb33	108581	108604	108591	3.08492	70%
0xccc	124577	124602	124591	3.07791	80%
0xe66	140619	140640	140629	3.17662	90%



TEST #6F: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

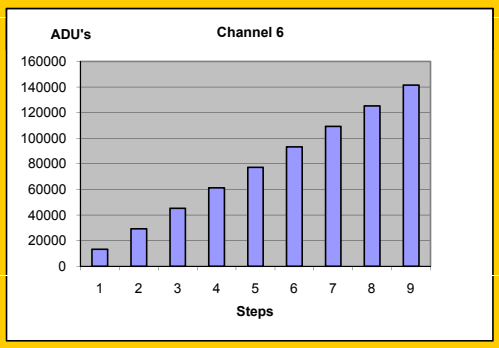
BrdTst6_006 / Channel 5					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12974	12998	12986	3.14333	10%
0x333	28965	28987	28975.2	3.21378	20%
0x4cc	44950	44973	44962.6	3.12546	30%
0x666	60979	61003	60991.5	3.12353	40%
0x800	77007	77031	77019.1	3.12853	50%
0x999	92997	93021	93009.3	3.18228	60%
0xb33	109026	109050	109039	3.13732	70%
0xccc	125017	125043	125029	3.18933	80%
0xe66	141048	141070	141058	2.98005	90%



TEST #6G: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

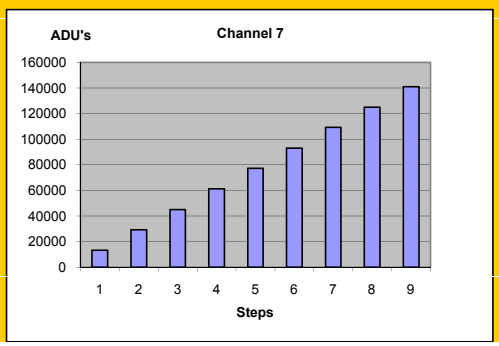
BrdTst6_006 / Channel 6					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13290	13312	13301	3.04195	10%
0x333	29281	29306	29294.1	3.15787	20%
0x4cc	45277	45300	45287.8	3.17327	30%
0x666	61309	61332	61319.9	3.12734	40%
0x800	77345	77366	77356.1	3.15237	50%
0x999	93342	93364	93352.9	3.10301	60%
0xb33	109374	109395	109385	3.15124	70%
0xccc	125370	125393	125382	3.17671	80%
0xe66	141405	141426	141414	3.05528	90%



TEST #6H: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

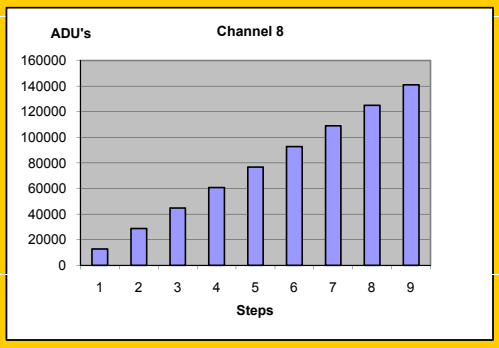
BrdTst6_006 / Channel 7					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13170	13193	13182.3	3.13994	10%
0x333	29147	29169	29157.3	3.05359	20%
0x4cc	45116	45138	45127.1	3.17926	30%
0x666	61130	61154	61140.8	3.07277	40%
0x800	77139	77162	77150.7	3.26665	50%
0x999	93111	93135	93123.6	3.17252	60%
0xb33	109126	109149	109138	3.04458	70%
0xccc	125101	125125	125112	3.15305	80%
0xe66	141114	141138	141126	3.11801	90%



TEST #6I: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

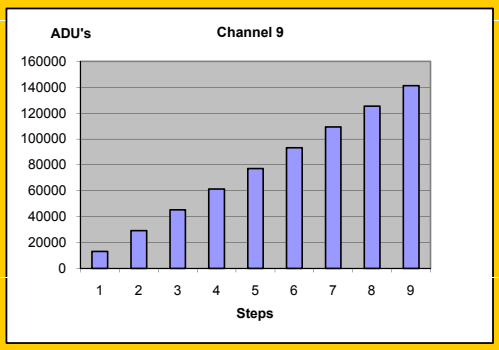
BrdTst6_006 / Channel 8					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12735	12758	12747.2	3.1595	10%
0x333	28742	28766	28754.8	3.13557	20%
0x4cc	44749	44772	44760.3	3.1059	30%
0x666	60797	60819	60808	3.14062	40%
0x800	76840	76864	76851.1	3.0201	50%
0x999	92844	92867	92855.9	3.09173	60%
0xb33	108892	108915	108903	3.12714	70%
0xccc	124901	124921	124911	3.16269	80%
0xe66	140950	140973	140961	3.16241	90%



TEST #6J: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

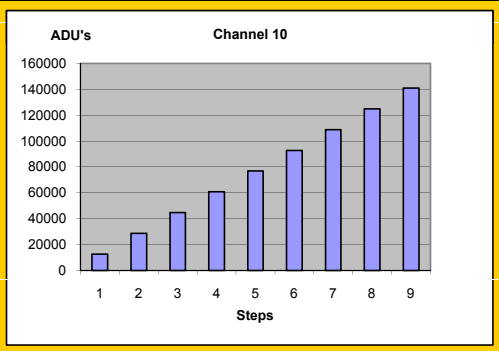
BrdTst6_006 / Channel 9					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13230	13253	13243.2	3.15739	10%
0x333	29222	29244	29232.9	3.13698	20%
0x4cc	45206	45230	45217.9	3.19234	30%
0x666	61233	61255	61245.2	3.13616	40%
0x800	77262	77284	77273.1	3.20495	50%
0x999	93253	93274	93263.9	3.1384	60%
0xb33	109282	109305	109293	3.13939	70%
0xccc	125269	125290	125280	3.09733	80%
0xe66	141298	141320	141309	3.18179	90%



TEST #6K: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

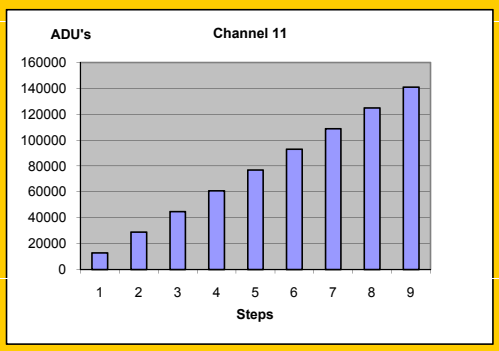
BrdTst6_006 / Channel 10					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12652	12673	12662	3.17944	10%
0x333	28666	28690	28678.3	3.15879	20%
0x4cc	44684	44709	44697.1	3.13684	30%
0x666	60740	60766	60753.2	3.03046	40%
0x800	76795	76818	76807.2	3.19501	50%
0x999	92814	92837	92825.1	3.10189	60%
0xb33	108866	108893	108882	3.03803	70%
0xccc	124892	124914	124902	3.08988	80%
0xe66	140949	140970	140960	3.18352	90%



TEST #6L: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

BrdTst6_006 / Channel 11					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12871	12895	12883.7	3.29659	10%
0x333	28864	28888	28874.7	3.20256	20%
0x4cc	44853	44878	44865.6	3.08462	30%
0x666	60885	60907	60895.2	3.13209	40%
0x800	76909	76932	76921.8	3.22051	50%
0x999	92898	92922	92911.4	3.22886	60%
0xb33	108931	108952	108942	3.11788	70%
0xccc	124925	124946	124935	3.15722	80%
0xe66	140953	140978	140965	3.1035	90%



Stage 13. Other Bit Tests. Table 11

Electronic Serial Number	0xDB6FA8		Board Serial Number	26
Firmware Version	0x193		Name Of Person Testing	S. Holm
Ident Register	0x502		Board passed Functional Tests	YES