DES 12 Channel Board - Functional Tests: CCD Acquisition Board Revision 1.0

Stage 1. Preparation of documentation and configuration settings - Table 1.

Board Part Number	9		Board Serial Number	0xDB8F8D
Date Of Tests	May 2010		Name Of Person Testing	S. Holm
Suggested Filename To Save	CCDACQ_12Ch_REPORT_BOARD9.xls		Sequence number: Test	

Stage 3. Power plane short test - Table 2.

Supply Name	Short test to ground: Impedance to ground	Test Point	
+1.2VD	61.50	TP43	~50 ohms
+1.8VD	1.5M	TPB12	> 1K ohm
+2.5VD	18K	TPB11	> 1K ohm
+3.3VD	5.7K	D13	> 1K ohm
+5VD	18.6K	D14	> 1K ohm
+5VA	4M	C267	> 1K ohm
-5VA	300K	C270	> 1K ohm
+15VA	500K	C288	> 1K ohm
-15VA	500K	C282	> 1K ohm
-28VA	2.6M	C307	> 1K ohm

Stage 4. Firmware programming tests - Table 3.

JTAG Order	Designator	Device	Load File	Check Sum or User Code
1	U122	XCF08PFS48C PROM	CcdAcqFpgaV41.mcs	0014ef670
2	U114	Spartan3 XC3S2000 FPGA	ccdacqfpgav41.bit	5102801

Stage 5. Power Consumption - Table 4.

Supply Name	Power Supply Consumption: Measured Voltage at test point	Measured Current on power supply	Test Point	
+1.2VD	1.20	N/A	TP43	
+1.8VD	1.80	N/A	TPB12	
+2.5VD	2.50	N/A	TPB11	
+3.3VD	3.30	0.088	D13	
+5VD	5.20	0.148	D14	
+5VA	5.00	0.55	C267	
-5VA	-5.00	0.43	C270	
+15VA	14.90	0.55	C288	
-15VA	-15.00	0.4	C282	
-28VA	-27.87	0.2	C307	
Vref 0+	10.07	N/A	R534	Vsub+ Reference(+10v)
Vref 0-	-2.48	N/A	R525	Vsub - Reference(-2.5v)
Vref Offset	2.50	N/A	R573	ADC Offset Reference(+2.5v)
Vclamp	1.88	N/A	VIA	ADC Clamp Voltage(+1.8v)
ADC Ref.	2.50	N/A	VIA	ADC Reference Voltage(+2.5v)
Vref 1+	2.50	N/A	R537	Vru and Vrl + Reference(+2.5v)
Vref 1-	-10.02	N/A	R535	Vru and Vrl - Reference(-10v)
Vref 2+	4.99	N/A	R563	Vog + Reference(+5v)
Vref 2-	-2.48	N/A	R555	Vog - Reference(-2.5v)
Vref 3+	2.50	N/A	R543	Vdd + Reference(+2.5v)
Vref 3-	-9.95	N/A	R571	Vdd - Reference(-10v)

Power Dissipation:
25.7 Watts

~27 watts +/- 5%

Stage 7. Basic Bus Transactions - **D**igital **Register** Tests - Table 5.

Register name	Put an X on any bit that has an error: 31-24	23-16	15-08	07-00	Function	Test name: Pattern	Walking 0's	Walking 1's
CDS Control			00000000	00000000	16 bit R/W			
Digital Output	00000000	00000000	00000000	00000000	32 bit R/W			
ADC Config.			0000	00000000	12 bit R/W			
Offset DAC			0000	00000000	12 bit R/W			
Bias DAC			0000	00000000	12 bit R/W			
Telemetry Config.				0000	4 bit R/W			
Auxilary Config.				00 00000000	10 bit R/W			
Redirect				0000	4 bit R/W			
Pixel Transfer				00000000	8 bit R/W			
Micro SEQ			00000000	00000000	16 bit R/W			
RAM Buffer			00000000	00000000	16 bit R/W			
LED Control				0000	4 bit R/W			
Control			00000000	00000000	16 bit R/W			
All Register Test	00000000	00000000	00000000	00000000	16 bit R/W	**Passed**	**Passed**	**Passed**

Stage 8. Bias Voltage settings and output enables testing - Table 8

DAC Value	Bias Voltage Test Data 410	2048	3686	50% rms Noise	10-90% Rise Time			
Signal	volts	volts	volts	uV	millisec.	Fanout Brd	Slope	Offset
Vru 0	-13.16	-5.64	1.87	<10	1	BIAS 3	217.96	3278.04
Vru 1	-13.16	-5.64	1.87	<10	1	BIAS 4	217.96	3278.04
Vru 2	-13.16	-5.64	1.87	<10	1	BIAS 5	217.96	3278.04
Vru 3	-13.16	-5.64	1.87	<10	1	BIAS 6	217.96	3278.04
Vru 4	-13.16	-5.64	1.87	<10	1	BIAS 7	217.96	3278.04
Vru 5	-13.16	-5.64	1.87	<10	1	BIAS 8	217.96	3278.04
Vru 6	-13.16	-5.64	1.87	NA	NA	BIAS 9	217.96	3278.04
Vru 7	-13.16	-5.64	1.87	NA	NA	BIAS 10	217.96	3278.04
Vrl 0	-13.16	-5.64	1.87	<10	1	BIAS 11	217.96	3278.04
Vrl 1	-13.16	-5.64	1.87	<10	1	BIAS 12	217.96	3278.04
Vrl 2	-13.16	-5.64	1.87	<10	1	BIAS 13	217.96	3278.04
Vrl 3	-13.16	-5.64	1.87	<10	1	BIAS 14	217.96	3278.04
Vrl 4	-13.16	-5.64	1.87	<10	1	BIAS 15	217.96	3278.04
Vrl 5	-13.16	-5.64	1.87	<10	1	BIAS 16	217.96	3278.04
Vrl 6	-13.16	-5.64	1.87	NA	NA	BIAS 17	217.96	3278.04
Vrl 7	-13.16	-5.64	1.87	NA	NA	BIAS 18	217.96	3278.04
Vog 0	-1.74	1.25	4.24	<10	1	BIAS 19	547.83	1363.22
Vog 1	-1.74	1.25	4.24	<10	1	BIAS 20	547.83	1363.22
Vog 2	-1.74	1.25	4.24	<10	1	BIAS 21	547.83	1363.22
Vog 3	-1.74	1.25	4.24	<10	1	BIAS 22	547.83	1363.22
Vog 4	-1.74	1.25	4.24	<10	1	BIAS 23	547.83	1363.22
Vog 5	-1.74	1.25	4.24	<10	1	BIAS 24	547.83	1363.22
Vog 6	-1.74	1.25	4.24	NA	NA	BIAS 25	547.83	1363.22
Vog 7	-1.74	1.25	4.24	NA	NA	BIAS 26	547.83	1363.22
Vdd 0	-21.78	-9.33	3.13	<10	20	BIAS 27	131.51	3274.58
Vdd 1	-21.74	-9.31	3.12	<10	20	BIAS 28	131.78	3274.85
Vdd 2	-21.71	-9.30	3.12	<10	20	BIAS 29	131.94	3274.58
Vdd 3	-21.73	-9.30	3.12	<10	20	BIAS 30	131.83	3274.47
Vdd 4	-21.80	-9.34	3.13	<10	20	BIAS 21	131.41	3274.91
Vdd 5	-21.71	-9.29	3.12	<10	20	BIAS 32	131.94	3274.14
Vdd 6	-21.75	-9.31	3.13	NA	NA	BIAS 33	131.67	3273.87
Vdd 7	-21.80	-9.34	3.13	NA	NA	BIAS 34	131.41	3274.91

Vru	Slope		Offset
Mean	217.96	Mean	3278.04
Stdev	5.684E-14	Stdev	4.54747E-13
Average	217.96404	Average	3278.043731
	Dac #	Average voltage	
	0	-15.0	
	4095	3.8	

Vrl	Slope		Offset
Mean	217.96	Mean	3278.04
Stdev	5.684E-14	Stdev	4.54747E-13
Average	217.96404	Average	3278.043731
	Dac #	Average voltage	
	0	-15.0	
	4095	3.8	

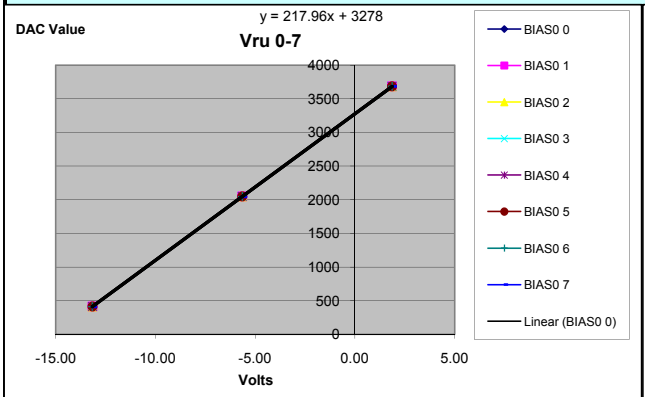
Vog	Slope		Offset
Mean	547.83	Mean	1363.22
Stdev	0	Stdev	0
Average	547.82609	Average	1363.217391
	Dac #	Average voltage	
	0	-2.5	
	4095	5.0	

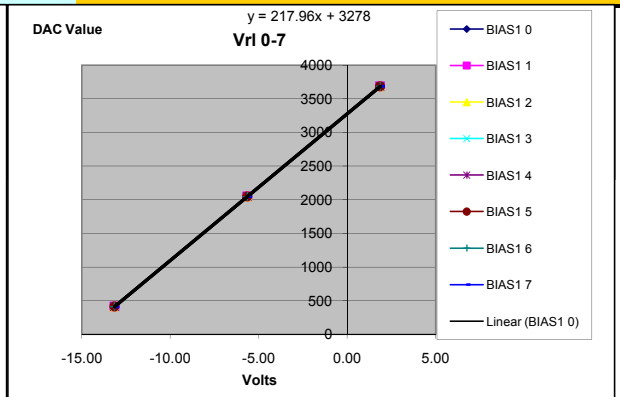
Vdd	Slope		Offset
Mean	131.69	Mean	3274.54
Stdev	0.2062322	Stdev	0.353498954
Average	131.68558	Average	3274.538124
	Dac #	Average voltage	
	0	-24.9	
	4095	6.2	

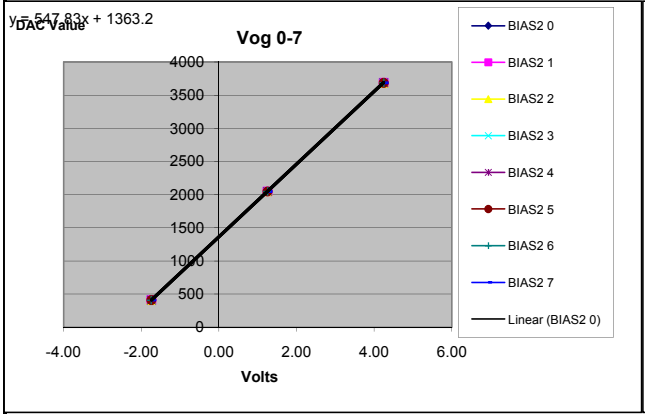
Notes and Observations

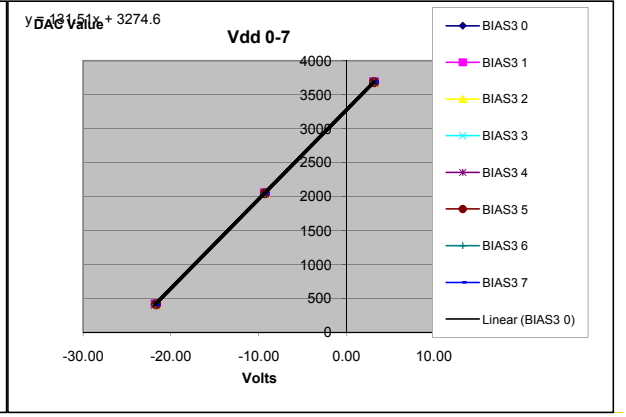
Checked for oscillations using a Agilent Oscilloscpe on AC.**OK**

average min & max voltages
(dac# -offset)/slope=voltage









Stage 8B. Telemetry System Tests - Table 7 (Bias Telemetry Tests)

DAC Value	410	3686	Bias Signals Set Volts		Resolved Values for Telemetry Channel	
	Telemetry Return Values					
Signal	10%	90%	10%	90%	Slope	Offset
Vru 0	-1741	422	-13.16	1.87	143.9122	152.88
Vru 1	-1739	422	-13.16	1.87	143.7791	153.13
Vru 2	-1743	423	-13.16	1.87	144.1118	153.51
Vru 3	-1740	422	-13.16	1.87	143.8456	153.01
Vru 4	-1744	423	-13.16	1.87	144.1783	153.39
Vru 5	-1742	422	-13.16	1.87	143.9787	152.76
Vru 6	-1743	422	-13.16	1.87	144.0452	152.64
Vru 7	-1742	423	-13.16	1.87	144.0452	153.64
Vrl 0	-1743	421	-13.16	1.87	143.9787	151.76
Vrl 1	-1749	422	-13.16	1.87	144.4444	151.89
Vrl 2	-1742	422	-13.16	1.87	143.9787	152.76
Vrl 3	-1747	422	-13.16	1.87	144.3114	152.14
Vrl 4	-1747	422	-13.16	1.87	144.3114	152.14
Vrl 5	-1746	422	-13.16	1.87	144.2448	152.26
Vrl 6	-1748	421	-13.16	1.87	144.3114	151.14
Vrl 7	-1747	422	-13.16	1.87	144.3114	152.14
Vog 0	-360	865	-1.74	4.24	204.8495	-3.56
Vog 1	-361	865	-1.74	4.24	205.0167	-4.27
Vog 2	-360	865	-1.74	4.24	204.8495	-3.56
Vog 3	-360	865	-1.74	4.24	204.8495	-3.56
Vog 4	-360	865	-1.74	4.24	204.8495	-3.56
Vog 5	-360	865	-1.74	4.24	204.8495	-3.56
Vog 6	-361	865	-1.74	4.24	205.0167	-4.27
Vog 7	-360	865	-1.74	4.24	204.8495	-3.56
Vdd 0	-1712	576	-21.78	3.13	91.8507	288.51
Vdd 1	-1709	576	-21.74	3.12	91.9147	289.23
Vdd 2	-1704	576	-21.71	3.12	91.8244	289.51
Vdd 3	-1711	576	-21.73	3.12	92.0322	288.86
Vdd 4	-1712	576	-21.80	3.13	91.7770	288.74
Vdd 5	-1708	576	-21.71	3.12	91.9855	289.01
Vdd 6	-1713	576	-21.75	3.13	92.0016	288.03
Vdd 7	-1713	576	-21.80	3.13	91.8171	288.61

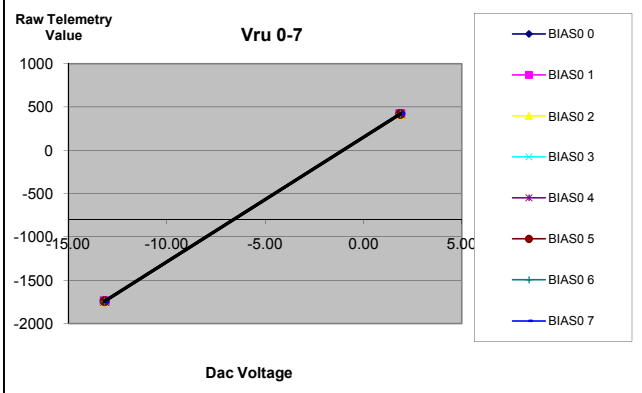
AVERAGE

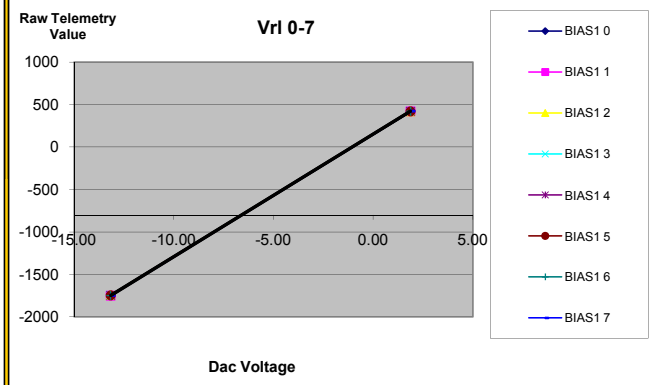
Vru	Slope		Offset
Mean	143.99	Mean	153.12
Stdev	0.1264029	Stdev	0.3395362

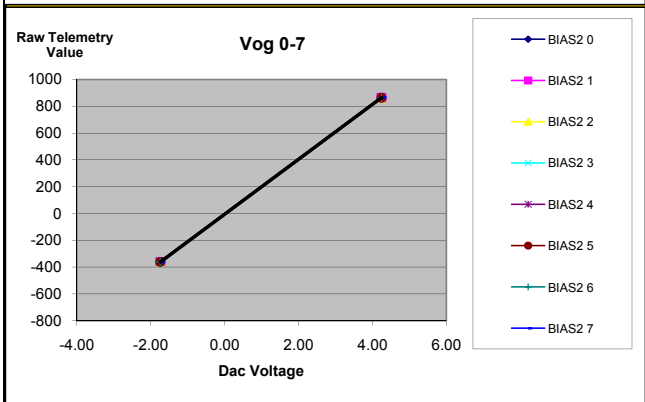
Vrl	Slope		Offset
Mean	144.24	Mean	152.03
Stdev	0.157579	Stdev	0.4345052

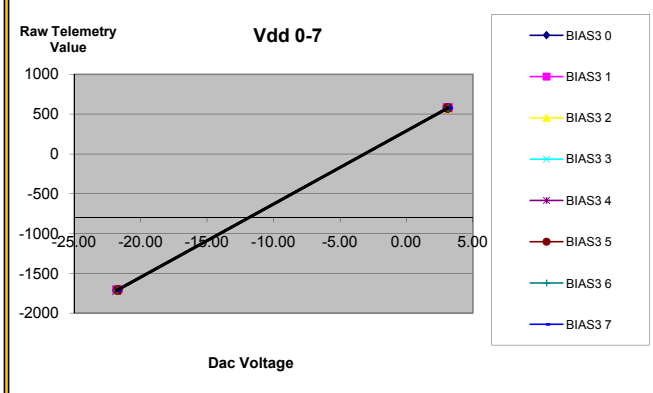
Vog	Slope		Offset
Mean	204.89	Mean	-3.74
Stdev	0.0724102	Stdev	0.307019

Vdd	Slope		Offset
Mean	91.90	Mean	288.81
Stdev	0.0904732	Stdev	0.4238317









Stage 8C. Bias Voltage output enables testing - Table 8

Place a line through Bias Voltage name if enable/disable switch works

Vru 0	Vru 1	Vru 2	Vru 3	Vru 4	Vru 5
Vrl 0	Vrl 1	Vrl 2	Vrl 3	Vrl 4	Vrl 5
Vog 0	Vog 1	Vog 2	Vog 3	Vog 4	Vog 5
Vdd 0	Vdd 1	Vdd 2	Vdd 3	Vdd 4	Vdd 5

Stage 9. Vsub and Heater Control testing - Table 9

DAC Value	Vsub Measured Voltage Test Data 10%	50%	90%
Signal	volts	volts	volts
Vsub - rate	-1.23	3.79	8.81
Vsub - Limit	-1.23	3.79	8.81
Vsub0	0.00	0.00	0.00
	Vsub Enable Bit - pass		

DAC Value	Telemetery Readback Test Data 10%	50%	90%
Signal	dec	dec	dec
Vbias 0	152	152	462
Vbias 1	-27	700	1427
RTD1	219	NA	NA
RTD2	248	NA	NA
RTD3	274	NA	NA
RTD4	303	NA	NA
RTD5	324	NA	NA
RTD6	351	NA	NA
Reference 4096	836	NA	NA
eference buffere	836	NA	NA

Stage 10. Video Offset DAC Tests - Table 10.

	DAC Value 410				DAC Value 2048				DAC Value 3686			
ADC	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU
0	0.250	NA	NA	16869	1.250		NA	80956	2.250	NA	500ms	145051
1	0.250	NA	NA	16953	1.250		NA	81029	2.250	NA	500ms	145104
2	0.250	NA	NA	16929	1.250		NA	80968	2.250	NA	500ms	145009
3	0.250	NA	NA	16820	1.250		NA	80922	2.250	NA	500ms	145025
4	0.250	NA	NA	17114	1.250		NA	81142	2.250	NA	500ms	145177
5	0.250	NA	NA	17189	1.250		NA	81221	2.250	NA	500ms	145250
6	0.250	NA	NA	17347	1.250		NA	81336	2.250	NA	500ms	145327
7	0.250	NA	NA	17074	1.250		NA	81153	2.250	NA	500ms	145241
8	0.250	NA	NA	17003	1.250		NA	81114	2.250	NA	500ms	145224
9	0.250	NA	NA	17078	1.250		NA	81154	2.250	NA	500ms	145237
10	0.250	NA	NA	17120	1.250		NA	81101	2.250	NA	500ms	145092
11	0.250	NA	NA	17133	1.250		NA	81156	2.250	NA	500ms	145170

ADC	DC Volts		Data Set		
Channel	Slope	Offset	410	2048	3686
0	1638.000	0.500	0.250	1.250	2.250
1	1638.000	0.500	0.250	1.250	2.250
2	1638.000	0.500	0.250	1.250	2.250
3	1638.000	0.500	0.250	1.250	2.250
4	1638.000	0.500	0.250	1.250	2.250
5	1638.000	0.500	0.250	1.250	2.250
6	1638.000	0.500	0.250	1.250	2.250
7	1638.000	0.500	0.250	1.250	2.250
8	1638.000	0.500	0.250	1.250	2.250
9	1638.000	0.500	0.250	1.250	2.250
10	1638.000	0.500	0.250	1.250	2.250
11	1638.000	0.500	0.250	1.250	2.250

(dac# -offset)/slope=Voltage

ADC	ADU's		Data Set		
Channel	Slope	Offset	410	2048	3686
0	0.026	-21.09	16869	80956	145051
1	0.026	-23.38	16953	81029	145104
2	0.026	-23.00	16929	80968	145009
3	0.026	-19.79	16820	80922	145025
4	0.026	-27.77	17114	81142	145177
5	0.026	-29.73	17189	81221	145250
6	0.026	-34.04	17347	81336	145327
7	0.026	-26.38	17074	81153	145241
8	0.026	-24.42	17003	81114	145224
9	0.026	-26.52	17078	81154	145237
10	0.026	-28.22	17120	81101	145092
11	0.026	-28.41	17133	81156	145170

(dac# -offset)/slope=ADU

Notes and Observations

Checked for oscillations using a Agilent Oscilloscope on AC. OK

Stage 11. CDS Control Functions and Video Channel Performanc

TEST #1: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit is held static. The purpose of this test is to verify the correct operation of the ADC devices and measure the noise of the Offset voltage generators, ADC buffer amplifiers and ADC devices

Noise Test 1

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	64945	64964	64954.8	2.28141
CH 1	65019	65036	65027.6	2.33974
CH 2	64962	64981	64972	2.3663
CH 3	64909	64925	64916.7	2.2176
CH 4	65147	65164	65154.9	2.17852
CH 5	65225	65241	65233	2.30283
CH 6	65350	65367	65358.2	2.38609
CH 7	65144	65161	65152.6	2.37275
CH 8	65096	65112	65104.4	2.275
CH 9	65148	65166	65156.7	2.39992
CH 10	65115	65131	65122.4	2.20508
CH 11	65156	65175	65166.5	2.4194

TEST #2: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the invert/non-invert and the DC Restore switches are held static.

Noise Test 2

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	64943	64963	64955.4	2.2782
CH 1	65020	65036	65027.9	2.33657
CH 2	64964	64980	64971.6	2.34135
CH 3	64907	64926	64916.7	2.23814
CH 4	65148	65162	65154.8	2.13615
CH 5	65225	65241	65233.1	2.36985
CH 6	65350	65368	65358.4	2.3894
CH 7	65143	65161	65152	2.35916
CH 8	65097	65113	65104.7	2.26364
CH 9	65147	65165	65156.3	2.41661
CH 10	65113	65131	65122.7	2.18925
CH 11	65158	65176	65167.1	2.4099

TEST #3: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the DC Restore switch is held static.

Noise Test 3

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	64945	64964	64955.2	2.25915
CH 1	65019	65036	65028	2.31295
CH 2	64964	64979	64971.6	2.37056
CH 3	64909	64925	64916.6	2.25936
CH 4	65147	65164	65154.9	2.14774
CH 5	65224	65241	65233.1	2.35615
CH 6	65351	65368	65358.9	2.37117
CH 7	65144	65161	65152.4	2.35592
CH 8	65096	65112	65104.4	2.24755
CH 9	65149	65166	65156.7	2.43058
CH 10	65114	65132	65123	2.21366
CH 11	65158	65175	65166.5	2.49657

TEST #4: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition.

Noise Test 4

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	64946	64965	64955.7	2.21844
CH 1	65020	65036	65027.4	2.28446
CH 2	64964	64981	64972.6	2.32025
CH 3	64908	64924	64916.5	2.24267
CH 4	65146	65163	65154.5	2.10564
CH 5	65225	65242	65233.4	2.3067
CH 6	65348	65368	65358.6	2.35463
CH 7	65143	65161	65152.3	2.42693
CH 8	65097	65113	65104.4	2.28404
CH 9	65148	65165	65156.3	2.39245
CH 10	65114	65130	65122.3	2.15421
CH 11	65158	65174	65166.6	2.42197

TEST #5: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the circuitry set to high GAIN.

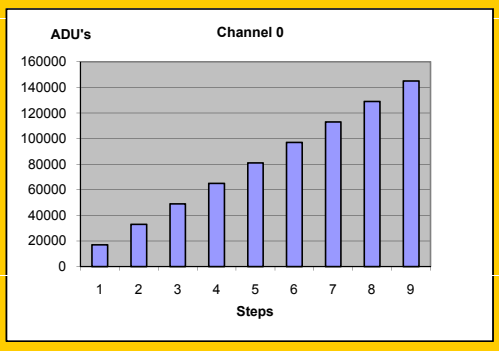
Noise Test 5

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	64945	64963	64955.1	2.28196
CH 1	65019	65036	65028	2.33757
CH 2	64964	64980	64972.4	2.34904
CH 3	64910	64926	64916.9	2.26111
CH 4	65147	65162	65154.6	2.15675
CH 5	65225	65244	65233	2.34979
CH 6	65349	65368	65358.8	2.35847
CH 7	65143	65161	65152.3	2.35319
CH 8	65095	65112	65104.2	2.28259
CH 9	65148	65165	65156.2	2.43906
CH 10	65114	65130	65123.1	2.18846
CH 11	65157	65175	65166.2	2.41124

TEST #6A: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

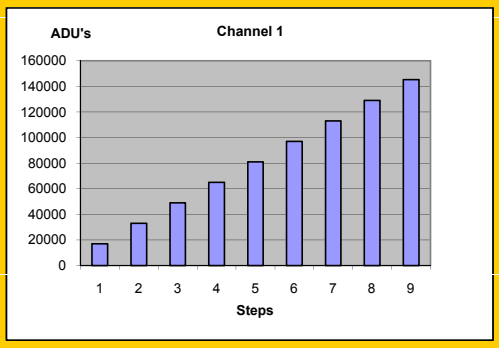
BrdTst6_006 / Channel 0					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	16897	16915	16905.1	2.31226	10%
0x333	32902	32918	32909	2.32168	20%
0x4cc	48905	48922	48913.4	2.15045	30%
0x666	64947	64963	64955.4	2.26315	40%
0x800	80987	81003	80994.4	2.24066	50%
0x999	96989	97006	96997.7	2.18741	60%
0xb33	113030	113047	113040	2.2896	70%
0xccc	129038	129055	129046	2.29587	80%
0xe66	145081	145097	145088	2.28298	90%



TEST #6B: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

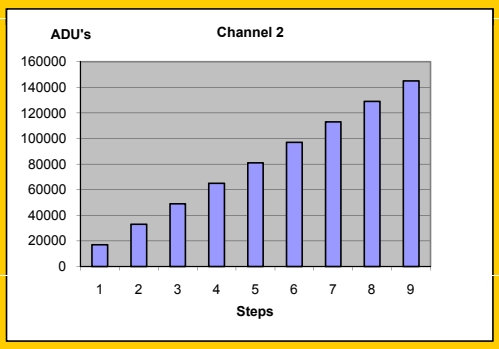
BrdTst6_006 / Channel 1					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	16981	17000	16990.3	2.43487	10%
0x333	32982	33000	32991.1	2.39907	20%
0x4cc	48979	48997	48988.1	2.41298	30%
0x666	65019	65036	65027.6	2.3104	40%
0x800	81054	81072	81063	2.36439	50%
0x999	97057	97074	97064.8	2.38799	60%
0xb33	113094	113115	113104	2.38368	70%
0xccc	129094	129111	129102	2.39835	80%
0xe66	145134	145149	145141	2.39993	90%



TEST #6C: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

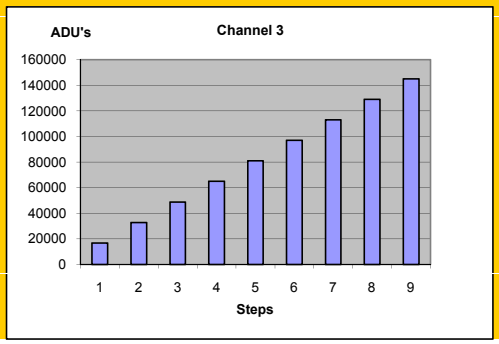
BrdTst6_006 / Channel 2					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	16955	16973	16964.6	2.35902	10%
0x333	32944	32961	32952.6	2.35468	20%
0x4cc	48939	48954	48945.9	2.22612	30%
0x666	64964	64981	64972.4	2.30533	40%
0x800	80996	81012	81004	2.32415	50%
0x999	96989	97005	96997.3	2.33709	60%
0xb33	113015	113032	113023	2.34044	70%
0xccc	129010	129025	129017	2.333	80%
0xe66	145036	145053	145044	2.38411	90%



TEST #6D: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

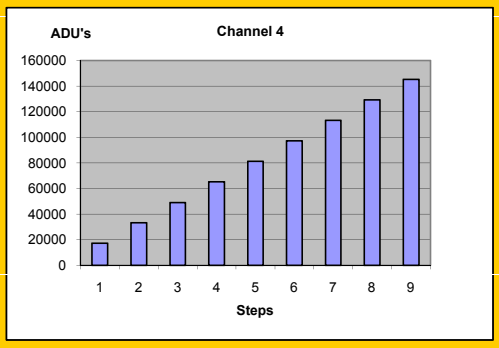
BrdTst6_006 / Channel 3					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	16849	16866	16858.5	2.33155	10%
0x333	32857	32874	32865.1	2.38831	20%
0x4cc	48863	48878	48871.2	2.35918	30%
0x666	64908	64927	64916.5	2.28082	40%
0x800	80952	80970	80960.2	2.3181	50%
0x999	96958	96975	96966.2	2.34121	60%
0xb33	113003	113020	113012	2.35049	70%
0xccc	129010	129027	129019	2.40052	80%
0xe66	145057	145073	145065	2.40891	90%



TEST #6E: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

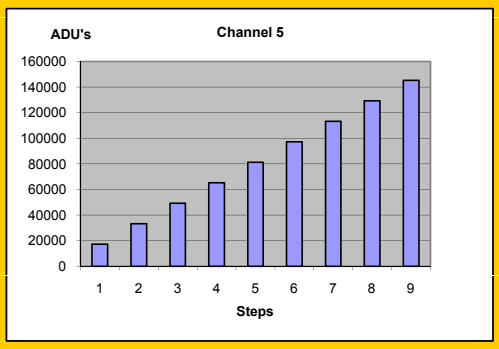
BrdTst6_006 / Channel 4					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	17142	17159	17149.5	2.28911	10%
0x333	33129	33146	33138	2.15342	20%
0x4cc	49120	49136	49127.7	2.26345	30%
0x666	65147	65163	65154.6	2.14962	40%
0x800	81170	81187	81178.5	2.28004	50%
0x999	97160	97176	97167.2	2.29459	60%
0xb33	113186	113202	113193	2.32169	70%
0xccc	129176	129194	129185	2.23844	80%
0xe66	145201	145220	145211	2.31273	90%



TEST #6F: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

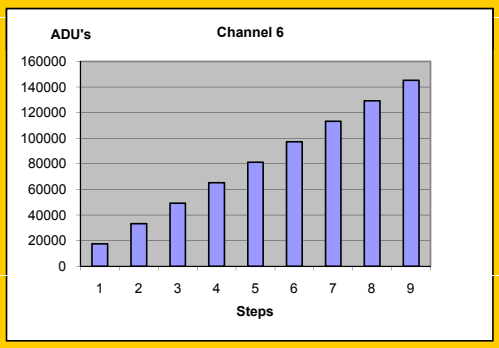
BrdTst6_006 / Channel 5					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	17220	17237	17228.5	2.35716	10%
0x333	33209	33225	33217.3	2.2715	20%
0x4cc	49197	49215	49205.5	2.24945	30%
0x666	65223	65240	65233	2.28816	40%
0x800	81252	81269	81260.5	2.36253	50%
0x999	97243	97260	97251.4	2.4417	60%
0xb33	113270	113286	113278	2.35871	70%
0xccc	129259	129277	129267	2.34496	80%
0xe66	145285	145302	145293	2.41623	90%



TEST #6G: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

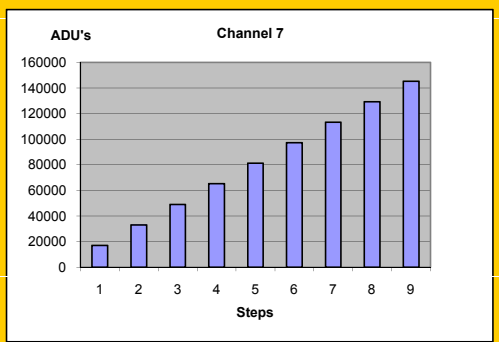
BrdTst6_006 / Channel 6					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	17378	17394	17385.7	2.36	10%
0x333	33357	33374	33364.5	2.41821	20%
0x4cc	49333	49350	49342.1	2.3479	30%
0x666	65352	65368	65358.9	2.3769	40%
0x800	81365	81383	81374.2	2.3703	50%
0x999	97342	97358	97350.1	2.3152	60%
0xb33	113358	113377	113368	2.39189	70%
0xccc	129336	129354	129346	2.29328	80%
0xe66	145355	145372	145363	2.37565	90%



TEST #6H: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

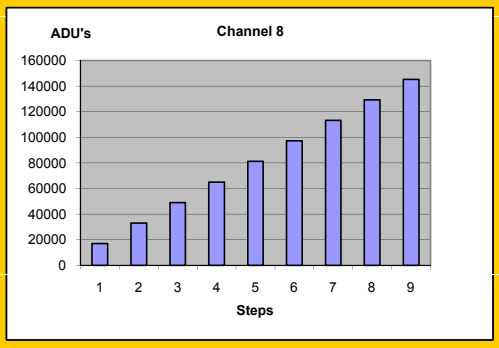
BrdTst6_006 / Channel 7					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	17102	17118	17109.6	2.33007	10%
0x333	33103	33122	33111.6	2.42203	20%
0x4cc	49104	49121	49112.4	2.46545	30%
0x666	65144	65161	65152.3	2.40026	40%
0x800	81181	81198	81190.7	2.37128	50%
0x999	97182	97200	97191.6	2.4265	60%
0xb33	113221	113240	113231	2.4813	70%
0xccc	129225	129242	129234	2.34503	80%
0xe66	145264	145282	145273	2.46307	90%



TEST #6I: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

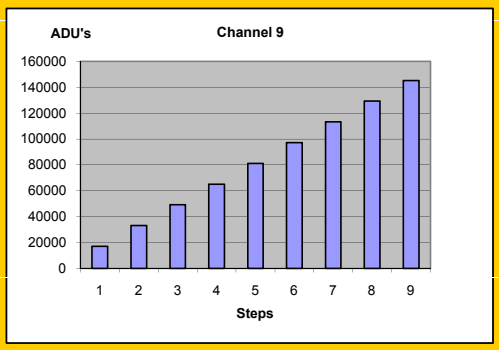
BrdTst6_006 / Channel 8					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	17033	17050	17042	2.19691	10%
0x333	33043	33060	33051.4	2.3062	20%
0x4cc	49049	49065	49056.9	2.34379	30%
0x666	65097	65113	65104.5	2.25816	40%
0x800	81138	81157	81149	2.30198	50%
0x999	97151	97168	97158.5	2.29691	60%
0xb33	113197	113213	113205	2.28036	70%
0xccc	129203	129221	129212	2.30195	80%
0xe66	145250	145267	145258	2.31914	90%



TEST #6J: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

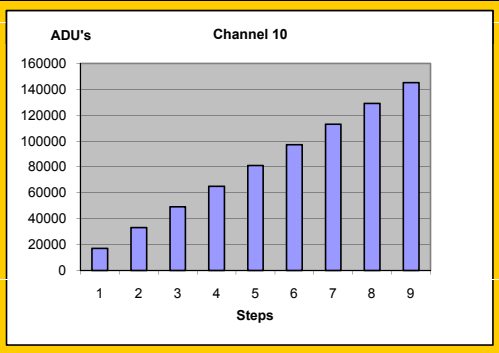
BrdTst6_006 / Channel 9					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	17105	17121	17113.5	2.34973	10%
0x333	33108	33124	33115.4	2.38454	20%
0x4cc	49106	49125	49116	2.42415	30%
0x666	65148	65165	65156.7	2.40855	40%
0x800	81178	81197	81188.8	2.21574	50%
0x999	97179	97197	97188.4	2.50512	60%
0xb33	113217	113237	113228	2.41653	70%
0xccc	129221	129239	129230	2.45701	80%
0xe66	145262	145278	145270	2.41474	90%



TEST #6K: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

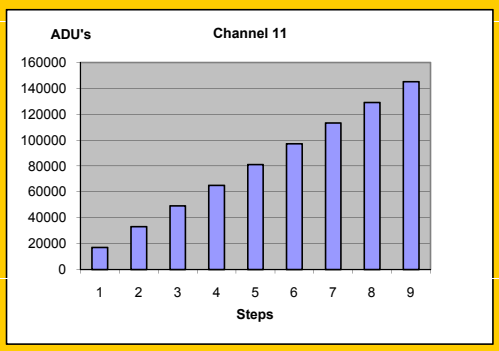
BrdTst6_006 / Channel 10					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	17145	17162	17153.2	2.36938	10%
0x333	33122	33138	33130.4	2.37814	20%
0x4cc	49099	49115	49107.1	2.17311	30%
0x666	65115	65131	65123	2.16131	40%
0x800	81131	81149	81140.7	2.33658	50%
0x999	97112	97129	97120.2	2.31631	60%
0xb33	113127	113143	113135	2.37492	70%
0xccc	129104	129121	129113	2.33022	80%
0xe66	145118	145138	145128	2.41265	90%



TEST #6L: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

BrdTst6_006 / Channel 11					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	17159	17176	17168.6	2.36427	10%
0x333	33148	33165	33155.6	2.47746	20%
0x4cc	49132	49149	49141	2.30763	30%
0x666	65157	65176	65166.6	2.40368	40%
0x800	81176	81193	81184.5	2.32834	50%
0x999	97160	97178	97169.9	2.32645	60%
0xb33	113187	113203	113195	2.44006	70%
0xccc	129173	129190	129182	2.42614	80%
0xe66	145198	145217	145208	2.41642	90%



Stage 13. Other Bit Tests. Table 11

Electronic Serial Number	0xDB8F8D		Board Serial Number	9
Firmware Version	0x193		Name Of Person Testing	S. Holm
Ident Register	0x502		Board passed Functional Tests	YES