DES 12 Channel Board - Functional Tests: CCD Acquisition Board Revision 1.0

Stage 1. Preparation of documentation and configuration settings - Table 1.

Board Part Number	13	Board Serial Number	0xDB8F92
Date Of Tests	July 2010	Name Of Person Testing	S. Holm
Suggested Filename To Save	CCDACQ_12Ch_REPORT_BOARD6.xls	Sequence number: Test	

Stage 3. Power plane short test - Table 2.

Supply Name	Short test to ground: Impedance to ground	Test Point	
+1.2VD	58.00	TP43	~50 ohms
+1.8VD	2M	TPB12	> 1K ohm
+2.5VD	10K	TPB11	> 1K ohm
+3.3VD	7K	D13	> 1K ohm
+5VD	15K	D14	> 1K ohm
+5VA	4M	C267	> 1K ohm
-5VA	40K	C270	> 1K ohm
+15VA	400K	C288	> 1K ohm
-15VA	400K	C282	> 1K ohm
-28VA	2.5M	C307	> 1K ohm

Stage 4. Firmware programming tests - Table 3.

JTAG Order	Designator	Device	Load File	Check Sum or User Code
1	U122	XCF08PFS48C PROM	CcdAcqFpgaV41.mcs	0014ef670
2	U114	Spartan3 XC3S2000 FPGA	ccdacqfpgav41.bit	5102801

Stage 5. Power Consumption - Table 4.

Supply Name	Power Supply Consumption: Measured Voltage at test point	Measured Current on power supply	Test Point	
+1.2VD	1.20	N/A	TP43	
+1.8VD	1.80	N/A	TPB12	
+2.5VD	2.50	N/A	TPB11	
+3.3VD	3.30	0.198	D13	
+5VD	5.20	0.15	D14	
+5VA	4.95	0.612	C267	
-5VA	-4.50	0.43	C270	
+15VA	14.90	0.555	C288	
-15VA	-15.00	0.406	C282	
-28VA	-27.80	0.199	C307	
Vref 0+	10.02	N/A	R534	Vsub+ Reference(+10v)
Vref 0-	-2.49	N/A	R525	Vsub - Reference(-2.5v)
Vref Offset	2.50	N/A	R573	ADC Offset Reference(+2.5v)
Vclamp	1.87	N/A	VIA	ADC Clamp Voltage(+1.8v)
ADC Ref.	2.50	N/A	VIA	ADC Reference Voltage(+2.5v)
Vref 1+	2.50	N/A	R537	Vru and Vrl + Reference(+2.5v)
Vref 1-	-10.03	N/A	R535	Vru and Vrl - Reference(-10v)
Vref 2+	5.00	N/A	R563	Vog + Reference(+5v)
Vref 2-	-2.49	N/A	R555	Vog - Reference(-2.5v)
Vref 3+	2.50	N/A	R543	Vdd + Reference(+2.5v)
Vref 3-	-10.02	N/A	R571	Vdd - Reference(-10v)

Power Dissipation:
26.3 Watts

~27 watts +/- 5%

Stage 7. Basic Bus Transactions - **D**igital **Register** Tests - Table 5.

Register name	Put an X on any bit that has an error: 31-24	23-16	15-08	07-00	Function	Test name: Pattern	Walking 0's	Walking 1's
CDS Control			00000000	00000000	16 bit R/W			
Digital Output	00000000	00000000	00000000	00000000	32 bit R/W			
ADC Config.			0000	00000000	12 bit R/W			
Offset DAC			0000	00000000	12 bit R/W			
Bias DAC			0000	00000000	12 bit R/W			
Telemetry Config.				0000	4 bit R/W			
Auxilary Config.			00	00000000	10 bit R/W			
Redirect				0000	4 bit R/W			
Pixel Transfer				00000000	8 bit R/W			
Micro SEQ			00000000	00000000	16 bit R/W			
RAM Buffer			00000000	00000000	16 bit R/W			
LED Control				0000	4 bit R/W			
Control			00000000	00000000	16 bit R/W			
All Register Test	00000000	00000000	00000000	00000000	16 bit R/W	**Passed**	**Passed**	**Passed**

Stage 8. Bias Voltage settings and output enables testing - Table 8

DAC Value	Bias Voltage Test Data 410	2048	3686	50% rms Noise	10-90% Rise Time			
Signal	volts	volts	volts	uV	millisec.	Fanout Brd	Slope	Offset
Vru 0	-13.18	-5.65	1.87	<10	1	BIAS 3	217.67	3278.59
Vru 1	-13.18	-5.65	1.87	<10	1	BIAS 4	217.67	3278.59
Vru 2	-13.18	-5.65	1.87	<10	1	BIAS 5	217.67	3278.59
Vru 3	-13.18	-5.65	1.87	<10	1	BIAS 6	217.67	3278.59
Vru 4	-13.18	-5.65	1.87	<10	1	BIAS 7	217.67	3278.59
Vru 5	-13.17	-5.65	1.87	<10	1	BIAS 8	217.82	3278.68
Vru 6	-13.19	-5.66	1.87	NA	NA	BIAS 9	217.53	3279.22
Vru 7	-13.16	-5.65	1.87	NA	NA	BIAS 10	217.96	3278.77
Vrl 0	-13.19	-5.65	1.87	<10	1	BIAS 11	217.53	3278.49
Vrl 1	-13.20	-5.66	1.87	<10	1	BIAS 12	217.39	3279.13
Vrl 2	-13.17	-5.66	1.87	<10	1	BIAS 13	217.82	3279.40
Vrl 3	-13.18	-5.65	1.87	<10	1	BIAS 14	217.67	3278.59
Vrl 4	-13.19	-5.66	1.87	<10	1	BIAS 15	217.53	3279.22
Vrl 5	-13.19	-5.66	1.87	<10	1	BIAS 16	217.53	3279.22
Vrl 6	-13.17	-5.65	1.87	NA	NA	BIAS 17	217.82	3278.68
Vrl 7	-13.17	-5.65	1.87	NA	NA	BIAS 18	217.82	3278.68
Vog 0	-1.74	1.25	4.25	<10	1	BIAS 19	546.91	1362.54
Vog 1	-1.74	1.25	4.25	<10	1	BIAS 20	546.91	1362.54
Vog 2	-1.74	1.25	4.25	<10	1	BIAS 21	546.91	1362.54
Vog 3	-1.74	1.25	4.25	<10	1	BIAS 22	546.91	1362.54
Vog 4	-1.75	1.25	4.25	<10	1	BIAS 23	546.00	1365.50
Vog 5	-1.75	1.25	4.25	<10	1	BIAS 24	546.00	1365.50
Vog 6	-1.75	1.25	4.25	NA	NA	BIAS 25	546.00	1365.50
Vog 7	-1.75	1.25	4.25	NA	NA	BIAS 26	546.00	1365.50
Vdd 0	-22.03	-9.46	3.12	<10	20	BIAS 27	130.26	3279.81
Vdd 1	-21.96	-9.43	3.10	<10	20	BIAS 28	130.73	3280.75
Vdd 2	-22.07	-9.48	3.12	<10	20	BIAS 29	130.05	3280.46
Vdd 3	-22.04	-9.46	3.12	<10	20	BIAS 30	130.21	3279.76
Vdd 4	-21.98	-9.44	3.11	<10	20	BIAS 21	130.57	3280.15
Vdd 5	-21.96	-9.43	3.11	<10	20	BIAS 32	130.67	3279.82
Vdd 6	-21.96	-9.43	3.11	NA	NA	BIAS 33	130.67	3279.82
Vdd 7	-22.02	-9.45	3.11	NA	NA	BIAS 34	130.36	3280.36

Vru	Slope		Offset
Mean	217.71	Mean	3278.70
Stdev	0.1200162	Stdev	0.20616622
Average	217.71063	Average	3278.699615
	Dac #	Average voltage	
	0	-15.0	
	4095	3.8	

Vrl	Slope		Offset
Mean	217.64	Mean	3278.93
Stdev	0.1575491	Stdev	0.328982967
Average	217.63834	Average	3278.925486
	Dac #	Average voltage	
	0	-15.1	
	4095	3.8	

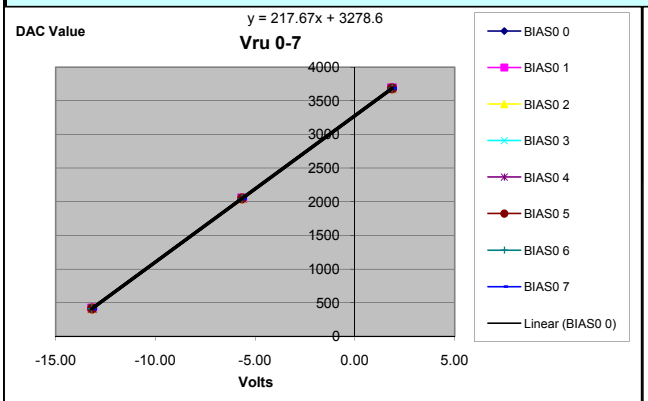
Vog	Slope		Offset
Mean	546.46	Mean	1364.02
Stdev	0.4555056	Stdev	1.480900294
Average	546.45551	Average	1364.0191
	Dac #	Average voltage	
	0	-2.5	
	4095	5.0	

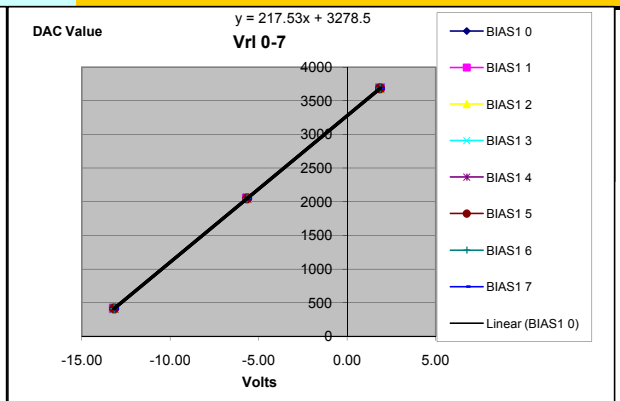
Vdd	Slope		Offset
Mean	130.44	Mean	3280.11
Stdev	0.2378972	Stdev	0.348462996
Average	130.44041	Average	3280.11426
	Dac #	Average voltage	
	0	-25.1	
	4095	6.3	

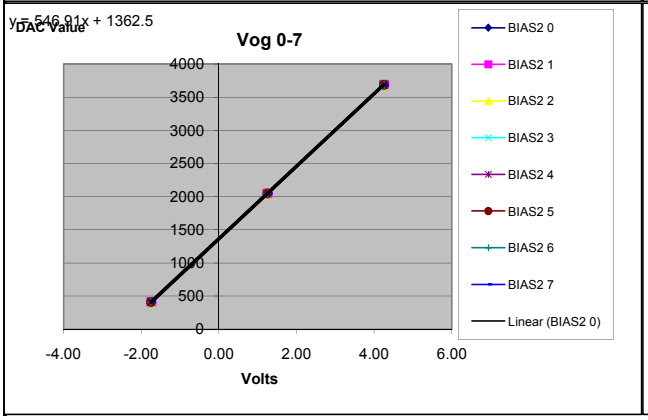
Notes and Observations

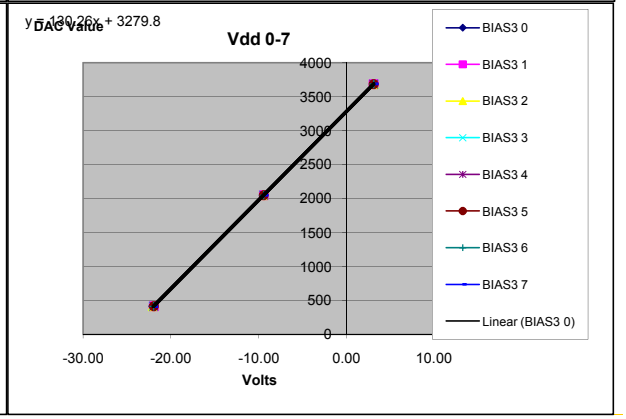
Checked for oscillations using a Agilent Oscilloscpe on AC.**OK**

average min & max voltages
(dac# -offset)/slope=voltage









Stage 8B. Telemetry System Tests - Table 7 (Bias Telemetry Tests)

DAC Value	410	3686	Bias Signals Set Volts		Resolved Values for Telemetry Channel	
	Telemetry Return Values					
Signal	10%	90%	10%	90%	Slope	Offset
Vru 0	-1753	422	-13.18	1.87	144.5183	151.75
Vru 1	-1753	422	-13.18	1.87	144.5183	151.75
Vru 2	-1756	422	-13.18	1.87	144.7176	151.38
Vru 3	-1753	422	-13.18	1.87	144.5183	151.75
Vru 4	-1756	422	-13.18	1.87	144.7176	151.38
Vru 5	-1755	422	-13.17	1.87	144.7473	151.32
Vru 6	-1752	422	-13.19	1.87	144.3559	152.05
Vru 7	-1751	422	-13.16	1.87	144.5775	151.64
Vrl 0	-1756	422	-13.19	1.87	144.6215	151.56
Vrl 1	-1756	422	-13.20	1.87	144.5255	151.74
Vrl 2	-1749	422	-13.17	1.87	144.3484	152.07
Vrl 3	-1752	422	-13.18	1.87	144.4518	151.88
Vrl 4	-1755	422	-13.19	1.87	144.5551	151.68
Vrl 5	-1751	422	-13.19	1.87	144.2895	152.18
Vrl 6	-1757	422	-13.17	1.87	144.8803	151.07
Vrl 7	-1757	422	-13.17	1.87	144.8803	151.07
Vog 0	-361	868	-1.74	4.25	205.1753	-3.99
Vog 1	-361	868	-1.74	4.25	205.1753	-3.99
Vog 2	-361	868	-1.74	4.25	205.1753	-3.99
Vog 3	-361	868	-1.74	4.25	205.1753	-3.99
Vog 4	-361	868	-1.75	4.25	204.8333	-2.54
Vog 5	-361	868	-1.75	4.25	204.8333	-2.54
Vog 6	-361	868	-1.75	4.25	204.8333	-2.54
Vog 7	-361	868	-1.75	4.25	204.8333	-2.54
Vdd 0	-1733	574	-22.03	3.12	91.7296	287.80
Vdd 1	-1731	573	-21.96	3.10	91.9393	287.99
Vdd 2	-1742	575	-22.07	3.12	91.9809	288.02
Vdd 3	-1737	575	-22.04	3.12	91.8919	288.30
Vdd 4	-1732	574	-21.98	3.11	91.9091	288.16
Vdd 5	-1732	574	-21.96	3.11	91.9824	287.93
Vdd 6	-1731	573	-21.96	3.11	91.9027	287.18
Vdd 7	-1739	575	-22.02	3.11	92.0812	288.63

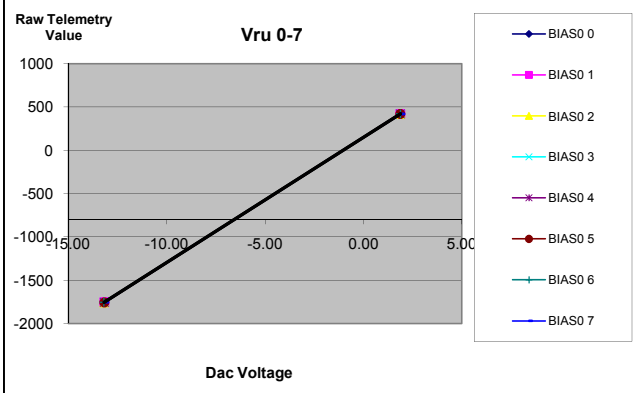
AVERAGE

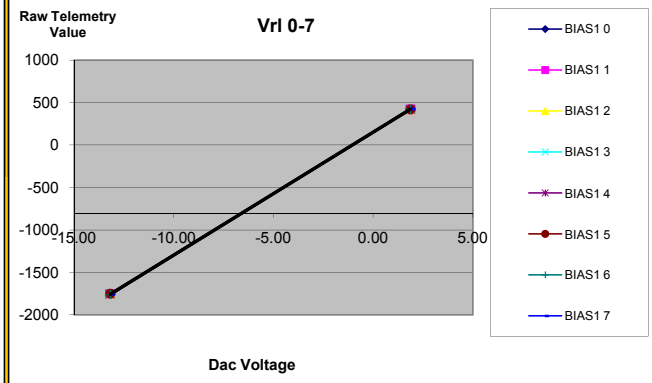
Vru	Slope		Offset
Mean	144.58	Mean	151.63
Stdev	0.1261991	Stdev	0.2359923

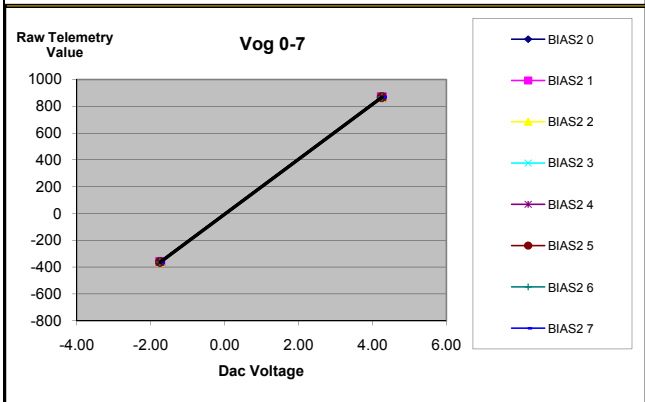
Vrl	Slope		Offset
Mean	144.57	Mean	151.66
Stdev	0.2059081	Stdev	0.3850482

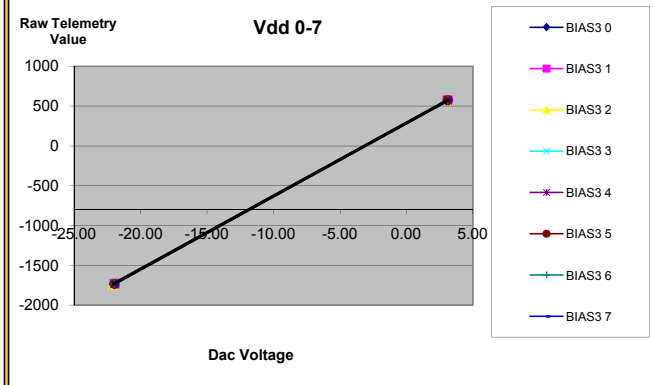
Vog	Slope		Offset
Mean	205.00	Mean	-3.27
Stdev	0.1709794	Stdev	0.7266625

Vdd	Slope		Offset
Mean	91.93	Mean	288.00
Stdev	0.0942135	Stdev	0.3905095









Stage 8C. Bias Voltage output enables testing - Table 8

Place a line through Bias Voltage name if enable/disable switch works

Vru 0	Vru 1	Vru 2	Vru 3	Vru 4	Vru 5
Vrl 0	Vrl 1	Vrl 2	Vrl 3	Vrl 4	Vrl 5
Vog 0	Vog 1	Vog 2	Vog 3	Vog 4	Vog 5
Vdd 0	Vdd 1	Vdd 2	Vdd 3	Vdd 4	Vdd 5

Stage 9. Vsub and Heater Control testing - Table 9

DAC Value	Vsub Measured Voltage Test Data 10%	50%	90%
Signal	volts	volts	volts
Vsub - rate	-1.24	3.76	8.77
Vsub - Limit	-1.24	3.76	8.77
Vsub0	0.00	0.00	0.00
	Vsub Enable Bit - pass		

DAC Value	Telemetery Readback Test Data 10%	50%	90%
Signal	dec	dec	dec
Vbias 0	148	269	454
Vbias 1	-28	696	1420
RTD1	219	NA	NA
RTD2	250	NA	NA
RTD3	274	NA	NA
RTD4	302	NA	NA
RTD5	324	NA	NA
RTD6	352	NA	NA
Reference 4096	836	NA	NA
eference buffere	836	NA	NA

Stage 10. Video Offset DAC Tests - Table 10.

	DAC Value 410				DAC Value 2048				DAC Value 3686			
ADC	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU
0	0.250	NA	NA	16981	1.250		NA	81070	2.250	NA	500ms	145161
1	0.250	NA	NA	16996	1.250		NA	81074	2.250	NA	500ms	145165
2	0.250	NA	NA	17016	1.250		NA	81128	2.250	NA	500ms	145244
3	0.250	NA	NA	17208	1.250		NA	81194	2.250	NA	500ms	145175
4	0.250	NA	NA	16908	1.250		NA	80967	2.250	NA	500ms	145028
5	0.250	NA	NA	16807	1.250		NA	80933	2.250	NA	500ms	145056
6	0.250	NA	NA	17002	1.250		NA	81106	2.250	NA	500ms	145201
7	0.250	NA	NA	17101	1.250		NA	81099	2.250	NA	500ms	145102
8	0.250	NA	NA	17003	1.250		NA	81060	2.250	NA	500ms	145115
9	0.250	NA	NA	17084	1.250		NA	81097	2.250	NA	500ms	145113
10	0.250	NA	NA	17067	1.250		NA	81164	2.250	NA	500ms	145267
11	0.250	NA	NA	17122	1.250		NA	81159	2.250	NA	500ms	145201

ADC	DC Volts		Data Set		
Channel	Slope	Offset	410	2048	3686
0	1638.000	0.500	0.250	1.250	2.250
1	1638.000	0.500	0.250	1.250	2.250
2	1638.000	0.500	0.250	1.250	2.250
3	1638.000	0.500	0.250	1.250	2.250
4	1638.000	0.500	0.250	1.250	2.250
5	1638.000	0.500	0.250	1.250	2.250
6	1638.000	0.500	0.250	1.250	2.250
7	1638.000	0.500	0.250	1.250	2.250
8	1638.000	0.500	0.250	1.250	2.250
9	1638.000	0.500	0.250	1.250	2.250
10	1638.000	0.500	0.250	1.250	2.250
11	1638.000	0.500	0.250	1.250	2.250

(dac# -offset)/slope=Voltage

ADC	ADU's		Data Set		
Channel	Slope	Offset	410	2048	3686
0	0.026	-23.99	16981	81070	145161
1	0.026	-24.36	16996	81074	145165
2	0.026	-24.71	17016	81128	145244
3	0.026	-30.55	17208	81194	145175
4	0.026	-22.33	16908	80967	145028
5	0.026	-19.33	16807	80933	145056
6	0.026	-24.51	17002	81106	145201
7	0.026	-27.65	17101	81099	145102
8	0.026	-24.80	17003	81060	145115
9	0.026	-27.13	17084	81097	145113
10	0.026	-26.10	17067	81164	145267
11	0.026	-27.92	17122	81159	145201

(dac# -offset)/slope=ADU

Notes and Observations

Checked for oscillations using a Agilent Oscilloscope on AC. OK

Stage 11. CDS Control Functions and Video Channel Performanc

TEST #1: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit is held static. The purpose of this test is to verify the correct operation of the ADC devices and measure the noise of the Offset voltage generators, ADC buffer amplifiers and ADC devices

Noise Test 1

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	81066	81085	81075.5	2.17988
CH 1	81077	81094	81084.8	2.35436
CH 2	81129	81146	81138.8	2.16674
CH 3	81188	81208	81198.1	2.40606
CH 4	80972	80988	80979.6	2.0764
CH 5	80926	80942	80933.9	2.15438
CH 6	81102	81118	81110.6	2.17598
CH 7	81100	81116	81107.3	2.21827
CH 8	81061	81076	81069.2	2.25492
CH 9	81096	81112	81103.8	2.35513
CH 10	81164	81180	81172	2.20949
CH 11	81158	81176	81166.6	2.39488

TEST #2: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the invert/non-invert and the DC Restore switches are held static.

Noise Test 2

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76365	76383	76373.4	2.84237
CH 1	76843	76864	76853.8	2.84917
CH 2	76611	76633	76622.7	2.81066
CH 3	76885	76908	76897.6	2.89241
CH 4	76061	76080	76071.4	2.69164
CH 5	76423	76444	76433.7	2.82496
CH 6	76723	76746	76733.5	2.81368
CH 7	76903	76928	76914	2.88645
CH 8	76451	76471	76461.8	2.76802
CH 9	76722	76740	76730.9	2.88313
CH 10	76693	76713	76703.3	2.84149
CH 11	76976	76996	76984.9	2.81101

TEST #3: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the DC Restore switch is held static.

Noise Test 3

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76355	76377	76365.7	3.10174
CH 1	76835	76856	76845.8	3.06501
CH 2	76601	76626	76613.2	3.08547
CH 3	76888	76911	76898.8	3.11303
CH 4	76065	76087	76075.4	3.06379
CH 5	76412	76434	76422.2	3.04251
CH 6	76722	76744	76732.2	3.05543
CH 7	76903	76926	76913.8	3.15671
CH 8	76438	76458	76448.5	2.98317
CH 9	76712	76733	76722.7	3.07253
CH 10	76698	76722	76710.2	3.13405
CH 11	76981	77005	76992.5	3.10528

TEST #4: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition.

Noise Test 4

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76301	76324	76312.5	3.27781
CH 1	76811	76834	76823	3.20864
CH 2	76570	76591	76580.4	3.07876
CH 3	76870	76893	76882.1	3.12791
CH 4	76053	76076	76064.3	3.1592
CH 5	76374	76398	76385.5	3.1896
CH 6	76713	76733	76722.9	2.98683
CH 7	76856	76881	76868.9	3.26882
CH 8	76445	76468	76456.7	3.10623
CH 9	76621	76644	76633.2	3.17176
CH 10	76676	76700	76687.3	3.25102
CH 11	76921	76946	76934.5	3.20843

TEST #5: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the circuitry set to high GAIN.

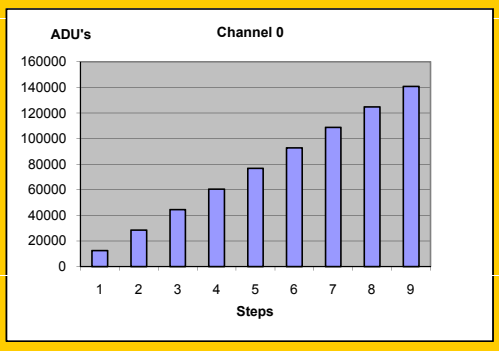
Noise Test 5

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76327	76352	76340	3.49984
CH 1	76829	76854	76842.6	3.62577
CH 2	76598	76625	76612.3	3.71578
CH 3	76881	76907	76893.5	3.71702
CH 4	76072	76100	76085.9	3.65685
CH 5	76379	76408	76393.7	3.65679
CH 6	76715	76742	76728.9	3.64238
CH 7	76861	76888	76875.3	3.7939
CH 8	76500	76528	76514	3.57876
CH 9	76628	76653	76641.3	3.67449
CH 10	76745	76772	76759.9	3.72219
CH 11	76931	76958	76943.8	3.74947

TEST #6A: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

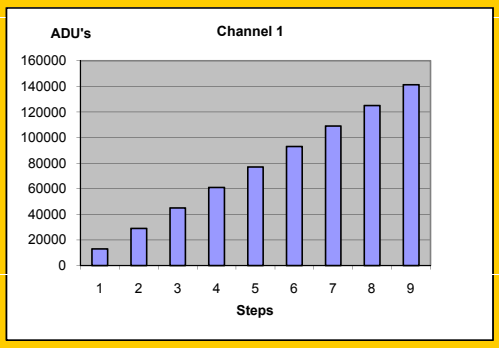
BrdTst6_006 / Channel 0					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12543	12568	12555.7	3.18686	10%
0x333	28544	28566	28555.2	3.20885	20%
0x4cc	44544	44567	44556	3.28503	30%
0x666	60581	60604	60593.1	3.21693	40%
0x800	76628	76650	76638.9	3.23138	50%
0x999	92628	92651	92640.5	3.13965	60%
0xb33	108671	108694	108683	3.17687	70%
0xccc	124672	124696	124686	3.2585	80%
0xe66	140719	140741	140731	3.18998	90%



TEST #6B: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

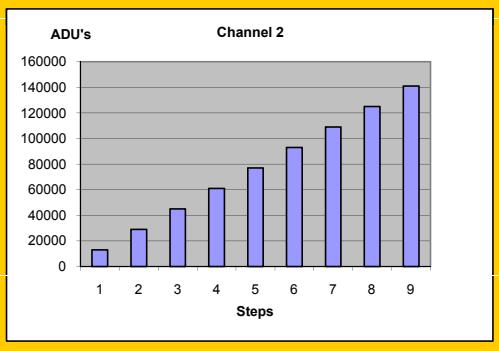
BrdTst6_006 / Channel 1					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12992	13015	13003.3	3.24044	10%
0x333	28992	29013	29002.2	3.20823	20%
0x4cc	44988	45011	44999.8	3.11028	30%
0x666	61026	61051	61037.4	3.25631	40%
0x800	77070	77094	77081.7	3.16451	50%
0x999	93076	93098	93086.6	3.13361	60%
0xb33	109116	109138	109126	3.16129	70%
0xccc	125115	125139	125126	3.08979	80%
0xe66	141156	141181	141169	3.2656	90%



TEST #6C: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

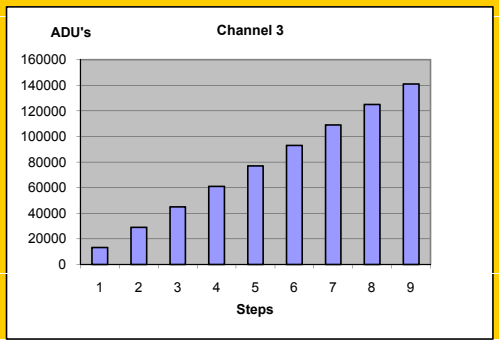
BrdTst6_006 / Channel 2					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12950	12973	12962.7	3.14153	10%
0x333	28934	28957	28946.2	3.05638	20%
0x4cc	44923	44945	44934.2	3.04847	30%
0x666	60946	60969	60957.4	3.0857	40%
0x800	76970	76993	76982	3.1546	50%
0x999	92960	92982	92970.8	3.09666	60%
0xb33	108978	109004	108992	3.21707	70%
0xccc	124980	125004	124992	2.98618	80%
0xe66	141007	141030	141018	3.15677	90%



TEST #6D: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

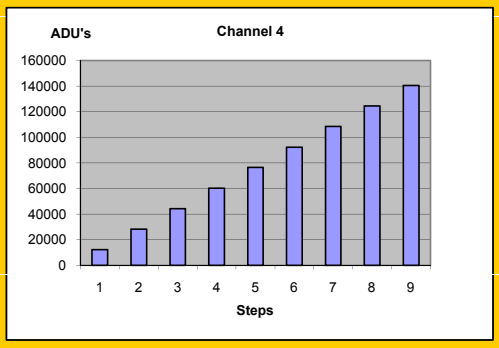
BrdTst6_006 / Channel 3					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13145	13169	13156.5	3.25847	10%
0x333	29119	29142	29130.5	3.27075	20%
0x4cc	45094	45118	45106.2	3.05338	30%
0x666	61109	61130	61119.7	3.25614	40%
0x800	77124	77147	77135.1	3.18742	50%
0x999	93100	93124	93111.4	3.27829	60%
0xb33	109114	109137	109126	3.28924	70%
0xccc	125090	125117	125104	3.28039	80%
0xe66	141109	141133	141120	3.23478	90%



TEST #6E: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

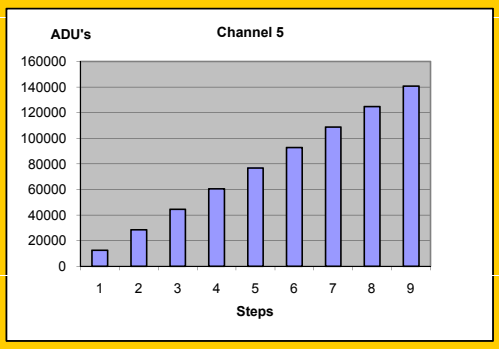
BrdTst6_006 / Channel 4					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12323	12345	12333.6	3.14189	10%
0x333	28316	28337	28326.3	3.10309	20%
0x4cc	44310	44333	44321.4	3.09539	30%
0x666	60342	60366	60353.3	3.13729	40%
0x800	76378	76402	76389.7	2.95383	50%
0x999	92373	92395	92385.2	3.06633	60%
0xb33	108408	108429	108419	2.95221	70%
0xccc	124406	124428	124417	3.20017	80%
0xe66	140445	140466	140455	3.02137	90%



TEST #6F: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

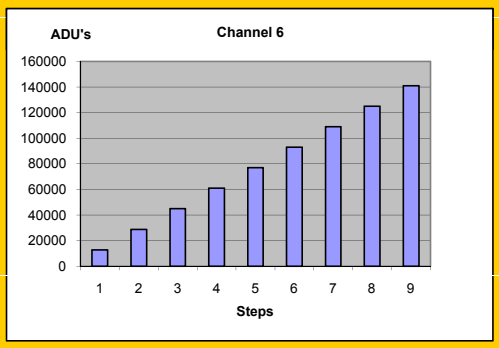
BrdTst6_006 / Channel 5					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12531	12556	12542.5	3.11995	10%
0x333	28540	28560	28549.6	3.12963	20%
0x4cc	44549	44572	44559.9	3.15061	30%
0x666	60596	60616	60605.8	3.08383	40%
0x800	76648	76671	76658.6	3.12375	50%
0x999	92659	92681	92670.5	3.11206	60%
0xb33	108706	108730	108718	3.15915	70%
0xccc	124719	124741	124731	3.12926	80%
0xe66	140770	140791	140781	3.16712	90%



TEST #6G: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

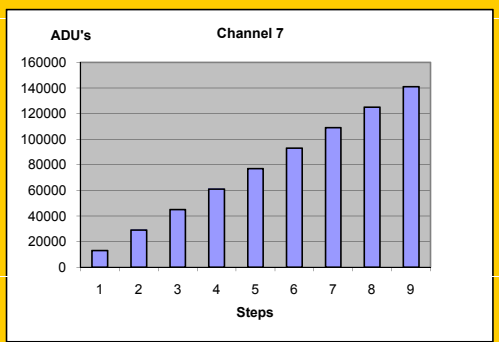
BrdTst6_006 / Channel 6					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12873	12895	12883.6	3.07836	10%
0x333	28874	28898	28887.4	3.13936	20%
0x4cc	44879	44902	44890.8	3.10128	30%
0x666	60922	60947	60934.5	3.19087	40%
0x800	76965	76989	76976.8	3.07383	50%
0x999	92973	92996	92984.3	3.13411	60%
0xb33	109016	109040	109028	3.00806	70%
0xccc	125021	125044	125033	3.12812	80%
0xe66	141068	141090	141079	3.1565	90%



TEST #6H: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

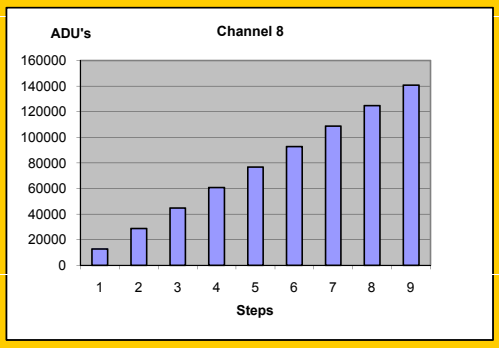
BrdTst6_006 / Channel 7					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13108	13138	13122.3	3.21516	10%
0x333	29088	29111	29099	3.25168	20%
0x4cc	45067	45092	45080.7	3.22394	30%
0x666	61084	61109	61096.5	3.24469	40%
0x800	77105	77129	77117.9	3.23157	50%
0x999	93084	93110	93096.7	3.30095	60%
0xb33	109102	109126	109115	3.24939	70%
0xccc	125087	125110	125098	3.2701	80%
0xe66	141109	141131	141120	3.26708	90%



TEST #6I: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

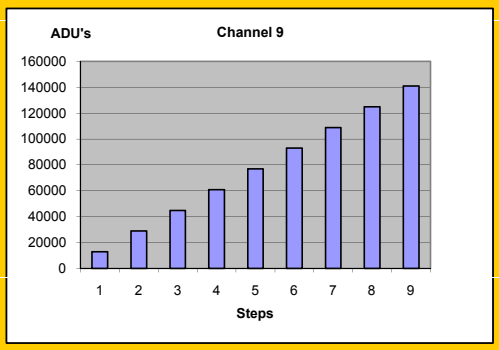
BrdTst6_006 / Channel 8					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12676	12697	12686.5	3.1216	10%
0x333	28668	28692	28678.6	3.04629	20%
0x4cc	44660	44683	44672.1	3.15517	30%
0x666	60693	60714	60704.3	2.89407	40%
0x800	76728	76752	76739.1	3.09249	50%
0x999	92723	92750	92733.5	3.13102	60%
0xb33	108757	108780	108768	3.12096	70%
0xccc	124751	124776	124763	3.20657	80%
0xe66	140786	140811	140799	3.1271	90%



TEST #6J: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

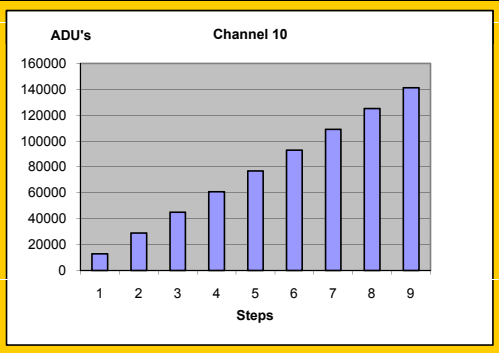
BrdTst6_006 / Channel 9					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12882	12906	12894.5	3.18921	10%
0x333	28868	28890	28879	3.24633	20%
0x4cc	44849	44872	44860.9	3.22614	30%
0x666	60873	60895	60884.4	3.18355	40%
0x800	76894	76918	76906	3.23846	50%
0x999	92877	92903	92890	3.25614	60%
0xb33	108904	108929	108916	3.20703	70%
0xccc	124888	124910	124899	3.20266	80%
0xe66	140916	140940	140928	3.24684	90%



TEST #6K: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

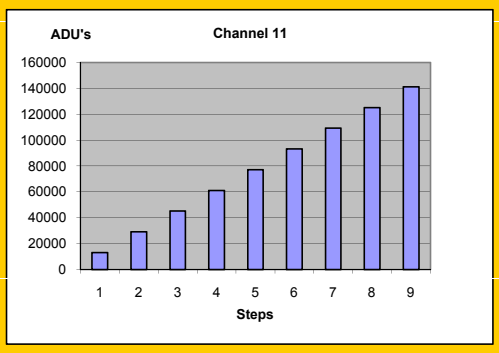
BrdTst6_006 / Channel 10					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12880	12904	12892.3	3.21784	10%
0x333	28885	28907	28895.9	3.03161	20%
0x4cc	44888	44912	44899.8	3.22533	30%
0x666	60931	60954	60941.9	3.22253	40%
0x800	76976	76997	76986.3	3.16801	50%
0x999	92983	93006	92994.1	3.13501	60%
0xb33	109026	109049	109038	3.21451	70%
0xccc	125033	125057	125044	3.06945	80%
0xe66	141082	141103	141092	3.1114	90%



TEST #6L: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

BrdTst6_006 / Channel 11					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13161	13185	13173.7	3.3568	10%
0x333	29152	29174	29163.9	3.25199	20%
0x4cc	45140	45162	45151.3	3.2551	30%
0x666	61169	61193	61180.7	3.24015	40%
0x800	77197	77221	77209.3	3.22966	50%
0x999	93189	93212	93199.6	3.25727	60%
0xb33	109216	109242	109230	3.26287	70%
0xccc	125208	125231	125220	3.03735	80%
0xe66	141241	141265	141254	3.31165	90%



Stage 13. Other Bit Tests. Table 11

Electronic Serial Number	0xDB8F92		Board Serial Number	13
Firmware Version	0x193		Name Of Person Testing	S. Holm
Ident Register	0x502		Board passed Functional Tests	YES