DES 12 Channel Board - Functional Tests: CCD Acquisition Board Revision 1.0

Stage 1. Preparation of documentation and configuration settings - Table 1.

Board Part Number	31		Board Serial Number	0xDB8F7D
Date Of Tests	August 2010		Name Of Person Testing	S. Holm
Suggested Filename To Save	CCDACQ_12Ch_REPORT_BOARD12.xl		Sequence number: Test	

Stage 3. Power plane short test - Table 2.

Supply Name	Short test to ground: Impedance to ground	Test Point	
+1.2VD	65.00	TP43	~50 ohms
+1.8VD	2M	TPB12	> 1K ohm
+2.5VD	2M	TPB11	> 1K ohm
+3.3VD	5K	D13	> 1K ohm
+5VD	18K	D14	> 1K ohm
+5VA	4M	C267	> 1K ohm
-5VA	400K	C270	> 1K ohm
+15VA	500K	C288	> 1K ohm
-15VA	500K	C282	> 1K ohm
-28VA	2.5M	C307	> 1K ohm

Stage 4. Firmware programming tests - Table 3.

JTAG Order	Designator	Device	Load File	Check Sum or User Code
1	U122	XCF08PFS48C PROM	CcdAcqFpgaV41.mcs	0014ef670
2	U114	Spartan3 XC3S2000 FPGA	ccdacqfpgav41.bit	5102801

Stage 5. Power Consumption - Table 4.

Supply Name	Power Supply Consumption: Measured Voltage at test point	Measured Current on power supply	Test Point	
+1.2VD	1.20	N/A	TP43	
+1.8VD	1.81	N/A	TPB12	
+2.5VD	2.50	N/A	TPB11	
+3.3VD	3.30	0.279	D13	
+5VD	5.20	0.15	D14	
+5VA	4.94	0.621	C267	
-5VA	-4.97	0.438	C270	
+15VA	14.96	0.561	C288	
-15VA	-15.07	0.404	C282	
-28VA	-27.90	0.193	C307	
Vref 0+	10.07	N/A	R534	Vsub+ Reference(+10v)
Vref 0-	-2.49	N/A	R525	Vsub - Reference(-2.5v)
Vref Offset	2.50	N/A	R573	ADC Offset Reference(+2.5v)
Vclamp	1.87	N/A	VIA	ADC Clamp Voltage(+1.8v)
ADC Ref.	2.50	N/A	VIA	ADC Reference Voltage(+2.5v)
Vref 1+	2.50	N/A	R537	Vru and Vrl + Reference(+2.5v)
Vref 1-	-10.03	N/A	R535	Vru and Vrl - Reference(-10v)
Vref 2+	5.00	N/A	R563	Vog + Reference(+5v)
Vref 2-	-2.54	N/A	R555	Vog - Reference(-2.5v)
Vref 3+	2.50	N/A	R543	Vdd + Reference(+2.5v)
Vref 3-	-10.04	N/A	R571	Vdd - Reference(-10v)

Power Dissipation:
26.8 Watts

~27 watts +/- 5%

Stage 7. Basic Bus Transactions - **D**igital **Register** Tests - Table 5.

Register name	Put an X on any bit that has an error: 31-24	23-16	15-08	07-00	Function	Test name: Pattern	Walking 0's	Walking 1's
CDS Control			00000000	00000000	16 bit R/W			
Digital Output	00000000	00000000	00000000	00000000	32 bit R/W			
ADC Config.			0000	00000000	12 bit R/W			
Offset DAC			0000	00000000	12 bit R/W			
Bias DAC			0000	00000000	12 bit R/W			
Telemetry Config.				0000	4 bit R/W			
Auxilary Config.			00	00000000	10 bit R/W			
Redirect				0000	4 bit R/W			
Pixel Transfer				00000000	8 bit R/W			
Micro SEQ			00000000	00000000	16 bit R/W			
RAM Buffer			00000000	00000000	16 bit R/W			
LED Control				0000	4 bit R/W			
Control			00000000	00000000	16 bit R/W			
All Register Test	00000000	00000000	00000000	00000000	16 bit R/W	**Passed**	**Passed**	**Passed**

Stage 8. Bias Voltage settings and output enables testing - Table 8

DAC Bias Voltage Test Data 50% 10-90%

Value	410	2048	3686	rms Noise	Rise Time			
Signal	volts	volts	volts	uV	millisec.	Fanout Brd	Slope	Offset
Vru 0	-13.18	-5.66	1.87	<10	1	BIAS 3	217.67	3279.31
Vru 1	-13.18	-5.66	1.87	<10	1	BIAS 4	217.67	3279.31
Vru 2	-13.18	-5.66	1.87	<10	1	BIAS 5	217.67	3279.31
Vru 3	-13.18	-5.66	1.87	<10	1	BIAS 6	217.67	3279.31
Vru 4	-13.18	-5.66	1.87	<10	1	BIAS 7	217.67	3279.31
Vru 5	-13.18	-5.66	1.87	<10	1	BIAS 8	217.67	3279.31
Vru 6	-13.18	-5.66	1.87	NA	NA	BIAS 9	217.67	3279.31
Vru 7	-13.18	-5.66	1.87	NA	NA	BIAS 10	217.67	3279.31
Vrl 0	-13.18	-5.66	1.87	<10	1	BIAS 11	217.67	3279.31
Vrl 1	-13.18	-5.66	1.87	<10	1	BIAS 12	217.67	3279.31
Vrl 2	-13.15	-5.66	1.87	<10	1	BIAS 13	218.11	3279.59
Vrl 3	-13.18	-5.66	1.87	<10	1	BIAS 14	217.67	3279.31
Vrl 4	-13.20	-5.66	1.87	<10	1	BIAS 15	217.39	3279.13
Vrl 5	-13.18	-5.66	1.87	<10	1	BIAS 16	217.67	3279.31
Vrl 6	-13.18	-5.66	1.87	NA	NA	BIAS 17	217.67	3279.31
Vrl 7	-13.17	-5.66	1.87	NA	NA	BIAS 18	217.82	3279.40
Vog 0	-1.75	1.25	4.25	<10	1	BIAS 19	546.00	1365.50
Vog 1	-1.75	1.25	4.25	<10	1	BIAS 20	546.00	1365.50
Vog 2	-1.75	1.25	4.25	<10	1	BIAS 21	546.00	1365.50
Vog 3	-1.75	1.25	4.25	<10	1	BIAS 22	546.00	1365.50
Vog 4	-1.75	1.25	4.25	<10	1	BIAS 23	546.00	1365.50
Vog 5	-1.75	1.25	4.25	<10	1	BIAS 24	546.00	1365.50
Vog 6	-1.75	1.25	4.25	NA	NA	BIAS 25	546.00	1365.50
Vog 7	-1.75	1.25	4.25	NA	NA	BIAS 26	546.00	1365.50
Vdd 0	-21.96	-9.43	3.11	<10	20	BIAS 27	130.67	3279.82
Vdd 1	-22.01	-9.45	3.11	<10	20	BIAS 28	130.41	3280.41
Vdd 2	-22.08	-9.48	3.11	<10	20	BIAS 29	130.05	3281.32
Vdd 3	-22.00	-9.44	3.11	<10	20	BIAS 30	130.47	3280.03
Vdd 4	-21.96	-9.43	3.11	<10	20	BIAS 21	130.67	3279.82
Vdd 5	-21.97	-9.43	3.11	<10	20	BIAS 32	130.62	3279.77
Vdd 6	-22.04	-9.46	3.11	NA	NA	BIAS 33	130.26	3280.68
Vdd 7	-21.99	-9.45	3.11	NA	NA	BIAS 34	130.52	3280.52

Vru	Slope		Offset
Mean	217.67	Mean	3279.31
Stdev	5.684E-14	Stdev	4.54747E-13
Average	217.67439	Average	3279.311447
	Dac #	Average voltage	
	0	-15.0	
	4095	3.8	

Vrl	Slope		Offset
Mean	217.71	Mean	3279.33
Stdev	0.1879036	Stdev	0.119583095
Average	217.71064	Average	3279.334287
	Dac #	Average voltage	
	0	-15.1	
	4095	3.8	

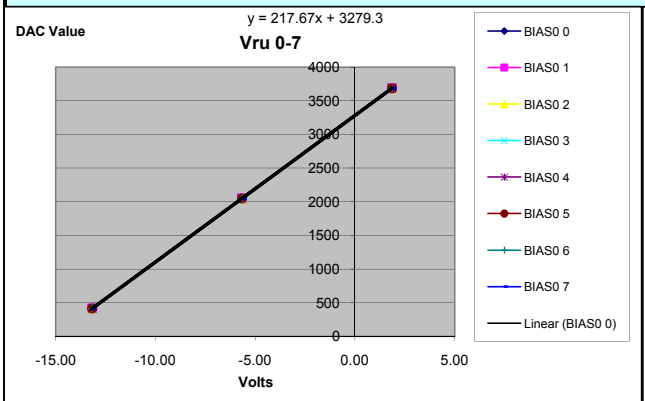
Vog	Slope		Offset
Mean	546.00	Mean	1365.50
Stdev	0	Stdev	0
Average	546	Average	1365.5
	Dac #	Average voltage	
	0	-2.5	
	4095	5.0	

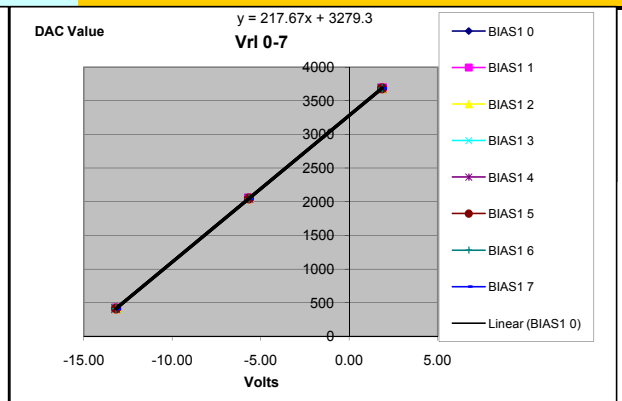
Vdd	Slope		Offset
Mean	130.46	Mean	3280.30
Stdev	0.2033614	Stdev	0.508367179
Average	130.45977	Average	3280.297452
	Dac #	Average voltage	
	0	-25.1	
	4095	6.3	

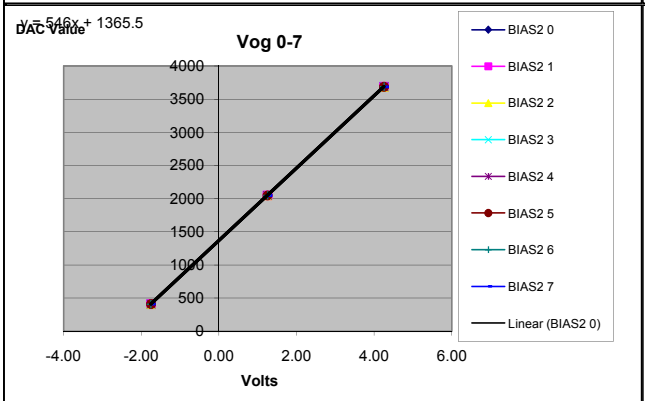
Notes and Observations

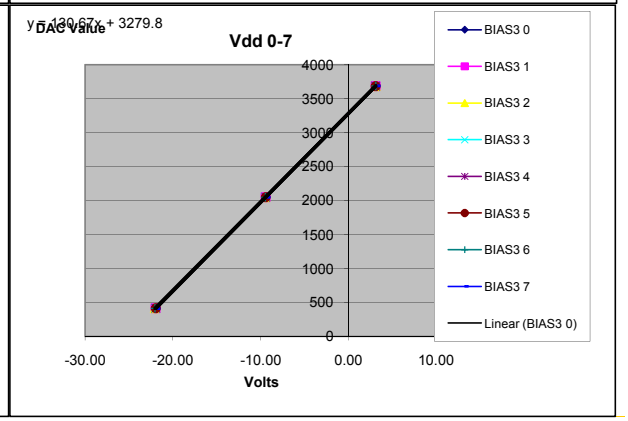
Checked for oscillations using a Agilent Oscilloscpe on AC.**OK**

average min & max voltages
(dac# -offset)/slope=voltage









Stage 8B. Telemetry System Tests - Table 7 (Bias Telemetry Tests)

DAC Value: 410 / 3686

Signal	Telemetry Return Values 10%	90%	Bias Signals Set Volts 10%	90%	Resolved Values for Telemetry Channel Slope	Offset
Vru 0	-1756	422	-13.18	1.87	144.7176	151.38
Vru 1	-1752	422	-13.18	1.87	144.4518	151.88
Vru 2	-1755	422	-13.18	1.87	144.6512	151.50
Vru 3	-1754	422	-13.18	1.87	144.5847	151.63
Vru 4	-1760	422	-13.18	1.87	144.9834	150.88
Vru 5	-1756	422	-13.18	1.87	144.7176	151.38
Vru 6	-1753	422	-13.18	1.87	144.5183	151.75
Vru 7	-1750	422	-13.18	1.87	144.3189	152.12
Vrl 0	-1755	422	-13.18	1.87	144.6512	151.50
Vrl 1	-1755	423	-13.18	1.87	144.7176	152.38
Vrl 2	-1752	421	-13.15	1.87	144.6738	150.46
Vrl 3	-1755	422	-13.18	1.87	144.6512	151.50
Vrl 4	-1752	422	-13.20	1.87	144.2601	152.23
Vrl 5	-1756	423	-13.18	1.87	144.7841	152.25
Vrl 6	-1753	422	-13.18	1.87	144.5183	151.75
Vrl 7	-1754	422	-13.17	1.87	144.6809	151.45
Vog 0	-360	868	-1.75	4.25	204.6667	-1.83
Vog 1	-360	868	-1.75	4.25	204.6667	-1.83
Vog 2	-361	868	-1.75	4.25	204.8333	-2.54
Vog 3	-360	868	-1.75	4.25	204.6667	-1.83
Vog 4	-361	868	-1.75	4.25	204.8333	-2.54
Vog 5	-360	868	-1.75	4.25	204.6667	-1.83
Vog 6	-360	868	-1.75	4.25	204.6667	-1.83
Vog 7	-360	868	-1.75	4.25	204.6667	-1.83
Vdd 0	-1724	573	-21.96	3.11	91.6235	288.05
Vdd 1	-1730	574	-22.01	3.11	91.7197	288.75
Vdd 2	-1736	575	-22.08	3.11	91.7428	289.68
Vdd 3	-1729	574	-22.00	3.11	91.7164	288.76
Vdd 4	-1726	573	-21.96	3.11	91.7032	287.80
Vdd 5	-1728	574	-21.97	3.11	91.7863	288.54
Vdd 6	-1732	575	-22.04	3.11	91.7296	289.72
Vdd 7	-1728	574	-21.99	3.11	91.7131	288.77

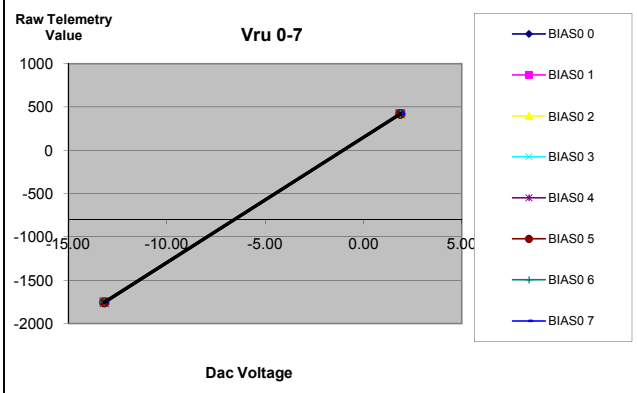
AVERAGE

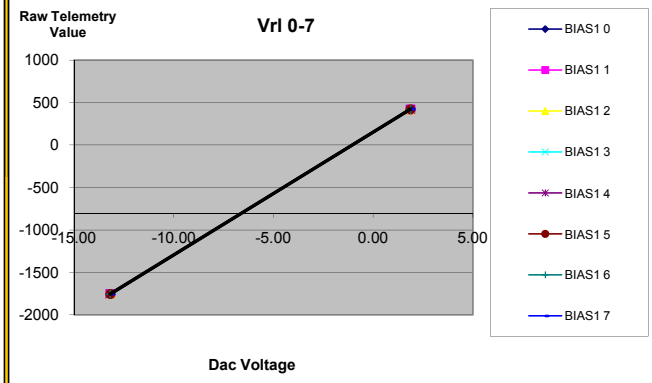
Vru	Slope		Offset
Mean	144.62	Mean	151.56
Stdev	0.1879354	Stdev	0.3514391

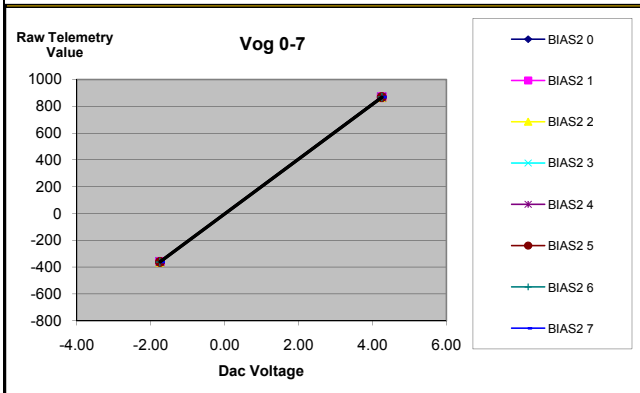
Vrl	Slope		Offset
Mean	144.62	Mean	151.69
Stdev	0.1519758	Stdev	0.5844721

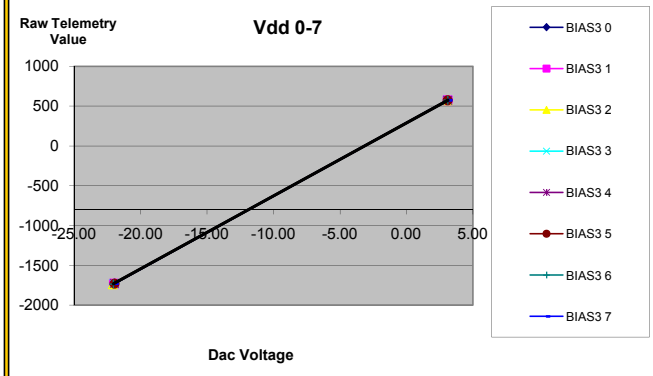
Vog	Slope		Offset
Mean	204.71	Mean	-2.01
Stdev	0.0721688	Stdev	0.3067173

Vdd	Slope		Offset
Mean	91.72	Mean	288.76
Stdev	0.0426992	Stdev	0.6358921









Stage 8C. Bias Voltage output enables testing - Table 8

Place a line through Bias Voltage name if enable/disable switch works

Vru 0	Vru 1	Vru 2	Vru 3	Vru 4	Vru 5
Vrl 0	Vrl 1	Vrl 2	Vrl 3	Vrl 4	Vrl 5
Vog 0	Vog 1	Vog 2	Vog 3	Vog 4	Vog 5
Vdd 0	Vdd 1	Vdd 2	Vdd 3	Vdd 4	Vdd 5

Stage 9. Vsub and Heater Control testing - Table 9

DAC Value	Vsub Measured Voltage Test Data 10%	50%	90%
Signal	volts	volts	volts
Vsub - rate	-1.24	3.78	8.81
Vsub - Limit	-1.24	3.78	8.81
Vsub0	0.00	0.00	0.00
	Vsub Enable Bit - pass		

DAC Value	Telemetery Readback Test Data 10%	50%	90%
Signal	dec	dec	dec
Vbias 0	154	269	419
Vbias 1	-27	698	1424
RTD1	220	NA	NA
RTD2	249	NA	NA
RTD3	275	NA	NA
RTD4	303	NA	NA
RTD5	325	NA	NA
RTD6	352	NA	NA
Reference 4096	837	NA	NA
eference buffere	837	NA	NA

Stage 10. Video Offset DAC Tests - Table 10.

	DAC Value 410				DAC Value 2048				DAC Value 3686			
ADC	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU
0	0.250	NA	NA	17126	1.250		NA	81105	2.250	NA	500ms	145086
1	0.250	NA	NA	17003	1.250		NA	81066	2.250	NA	500ms	145131
2	0.250	NA	NA	17085	1.250		NA	81088	2.250	NA	500ms	145082
3	0.250	NA	NA	17143	1.250		NA	81143	2.250	NA	500ms	145131
4	0.250	NA	NA	17001	1.250		NA	81118	2.250	NA	500ms	145232
5	0.250	NA	NA	17062	1.250		NA	81115	2.250	NA	500ms	145156
6	0.250	NA	NA	17075	1.250		NA	91150	2.250	NA	500ms	145230
7	0.250	NA	NA	17241	1.250		NA	81212	2.250	NA	500ms	145180
8	0.250	NA	NA	16943	1.250		NA	81014	2.250	NA	500ms	145092
9	0.250	NA	NA	16993	1.250		NA	81069	2.250	NA	500ms	145159
10	0.250	NA	NA	17130	1.250		NA	81177	2.250	NA	500ms	145216
11	0.250	NA	NA	16975	1.250		NA	81026	2.250	NA	500ms	145076

ADC	DC Volts		Data Set		
Channel	Slope	Offset	410	2048	3686
0	1638.000	0.500	0.250	1.250	2.250
1	1638.000	0.500	0.250	1.250	2.250
2	1638.000	0.500	0.250	1.250	2.250
3	1638.000	0.500	0.250	1.250	2.250
4	1638.000	0.500	0.250	1.250	2.250
5	1638.000	0.500	0.250	1.250	2.250
6	1638.000	0.500	0.250	1.250	2.250
7	1638.000	0.500	0.250	1.250	2.250
8	1638.000	0.500	0.250	1.250	2.250
9	1638.000	0.500	0.250	1.250	2.250
10	1638.000	0.500	0.250	1.250	2.250
11	1638.000	0.500	0.250	1.250	2.250

(dac# -offset)/slope=Voltage

ADC	ADU's		Data Set		
Channel	Slope	Offset	410	2048	3686
0	0.026	-28.45	17126	81105	145086
1	0.026	-24.73	17003	81066	145131
2	0.026	-27.32	17085	81088	145082
3	0.026	-28.85	17143	81143	145131
4	0.026	-24.35	17001	81118	145232
5	0.026	-26.41	17062	81115	145156
6	0.025	-93.66	17075	91150	145330
7	0.026	-32.08	17241	81212	145103
8	0.026	-22.90	16943	81014	145118
9	0.026	-23.73	16993	81069	145232
10	0.026	-28.58	17130	81177	145161
11	0.026	-23.58	16975	81026	145146

(dac# -offset)/slope=ADU

Notes and Observations

Checked for oscillations using a Agilent Oscilloscope on AC. OK

Stage 11. CDS Control Functions and Video Channel Performanc

TEST #1: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit is held static. The purpose of this test is to verify the correct operation of the ADC devices and measure the noise of the Offset voltage generators, ADC buffer amplifiers and ADC devices

Noise Test 1

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	81095	8.11E+04	81103.8	2.21036
CH 1	81056	8.11E+04	81064.8	2.30436
CH 2	81077	8.11E+04	81085.2	2.2444
CH 3	81136	8.12E+04	81144.5	2.33033
CH 4	81114	8.11E+04	81120.8	2.19083
CH 5	81105	8.11E+04	81112.2	2.3275
CH 6	81142	8.12E+04	81152.5	2.25485
CH 7	81201	8.12E+04	81211	2.38959
CH 8	81011	8.10E+04	81019.3	2.25791
CH 9	81063	81079	81070.6	2.37351
CH 10	81169	81184	81176.5	2.30454
CH 11	81018	81034	81026.7	2.23433

TEST #2: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the invert/non-invert and the DC Restore switches are held static.

Noise Test 2

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76233	7.63E+04	76244.7	2.80614
CH 1	76945	7.70E+04	76955.3	2.8213
CH 2	76536	7.66E+04	76544.4	2.80074
CH 3	76898	7.69E+04	76907.3	2.78805
CH 4	76472	7.65E+04	76483	2.61939
CH 5	76768	7.68E+04	76778	2.90212
CH 6	76988	7.70E+04	76997.7	2.86237
CH 7	76924	7.69E+04	76933.6	2.82858
CH 8	76388	7.64E+04	76398.5	2.74269
CH 9	76944	76964	76953.2	2.93913
CH 10	76587	76607	76597	2.9389
CH 11	76914	76935	76923.7	2.8582

TEST #3: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the DC Restore switch is held static.

Noise Test 3

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76228	7.62E+04	76237.4	2.98899
CH 1	76953	7.70E+04	76964.2	3.00557
CH 2	76530	7.66E+04	76540.1	3.10486
CH 3	76898	7.69E+04	76907.8	3.07397
CH 4	76470	7.65E+04	76482.9	2.85388
CH 5	76760	7.68E+04	76770.3	3.06548
CH 6	76982	7.70E+04	76992.6	3.04177
CH 7	76917	7.69E+04	76929.5	3.0443
CH 8	76386	7.64E+04	76398.1	2.96795
CH 9	76949	76975	76961.3	3.1932
CH 10	76590	76613	76600.1	3.11331
CH 11	76914	76941	76927.9	3.75517

TEST #4: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition.

Noise Test 4

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76218	7.62E+04	76230.1	2.99626
CH 1	76957	7.70E+04	76968.8	3.16879
CH 2	76533	7.66E+04	76545.3	3.12051
CH 3	76895	7.69E+04	76908	3.15838
CH 4	76511	7.65E+04	76522.4	3.11835
CH 5	76751	7.68E+04	76760.8	3.17094
CH 6	76988	7.70E+04	76999.6	3.20474
CH 7	76888	7.69E+04	76900.6	3.0553
CH 8	76432	7.65E+04	76442.2	3.07606
CH 9	76871	76894	76883.6	3.08632
CH 10	76607	76632	76619.8	3.26488
CH 11	76879	76902	76890.4	3.22884

TEST #5: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the circuitry set to high GAIN.

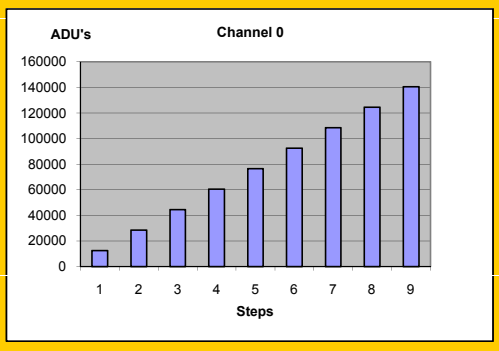
Noise Test 5

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76225	7.63E+04	76239.3	3.57787
CH 1	76967	7.70E+04	76980.9	3.82715
CH 2	76547	7.66E+04	76561.1	3.57591
CH 3	76900	7.69E+04	76913.8	3.60115
CH 4	76514	7.65E+04	76528	3.62913
CH 5	76746	7.68E+04	76759.4	3.69356
CH 6	76988	7.70E+04	77001.6	3.69712
CH 7	76891	7.69E+04	76903	3.68091
CH 8	76481	7.65E+04	76494	3.67226
CH 9	76872	76898	76884.6	3.51886
CH 10	76668	76695	76682	3.79837
CH 11	76878	76904	76890.4	3.74946

TEST #6A: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

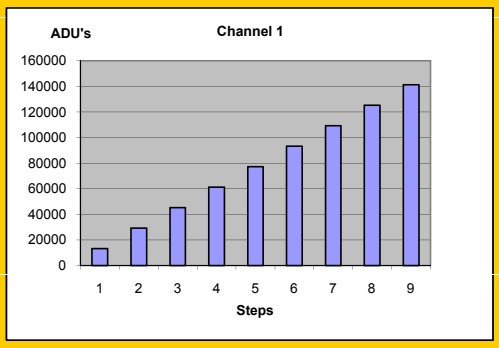
BrdTst6_006 / Channel 0					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12546	12566	12557	3.05471	10%
0x333	28522	28543	28532.2	3.13087	20%
0x4cc	44495	44517	44505.2	3.00082	30%
0x666	60506	60533	60519.7	3.12274	40%
0x800	76521	76546	76533.3	3.11196	50%
0x999	92499	92521	92509.4	3.11273	60%
0xb33	108511	108535	108524	3.08837	70%
0xccc	124488	124513	124500	3.11366	80%
0xe66	140504	140526	140515	3.1856	90%



TEST #6B: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

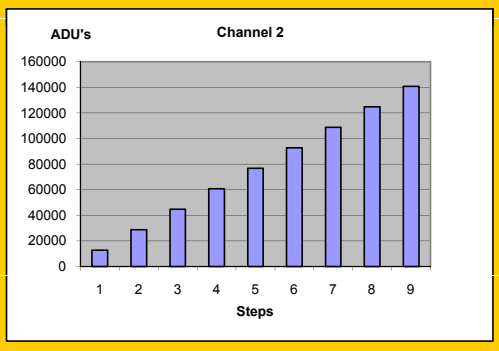
BrdTst6_006 / Channel 1					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13135	13158	13148	3.11242	10%
0x333	29133	29156	29144	3.1032	20%
0x4cc	45128	45148	45138.2	3.06077	30%
0x666	61163	61187	61174.2	3.13598	40%
0x800	77195	77219	77207.4	3.16713	50%
0x999	93194	93216	93204.3	3.05695	60%
0xb33	109230	109250	109240	3.16073	70%
0xccc	125224	125247	125236	3.12699	80%
0xe66	141261	141284	141272	3.2112	90%



TEST #6C: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

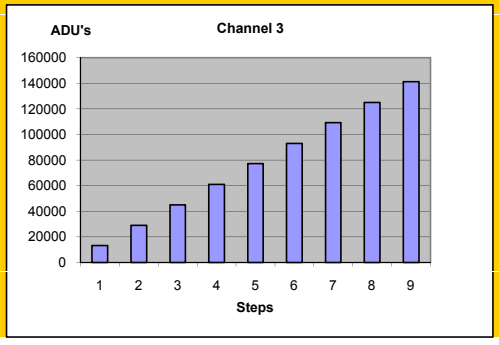
BrdTst6_006 / Channel 2					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12838	12863	12851.3	3.2096	10%
0x333	28821	28844	28831.9	3.16189	20%
0x4cc	44797	44821	44809.6	3.13219	30%
0x666	60816	60842	60829.1	3.11025	40%
0x800	76833	76856	76844.4	3.13673	50%
0x999	92816	92840	92826.8	3.09574	60%
0xb33	108834	108857	108846	3.12117	70%
0xccc	124816	124839	124827	3.11798	80%
0xe66	140836	140857	140847	3.14342	90%



TEST #6D: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

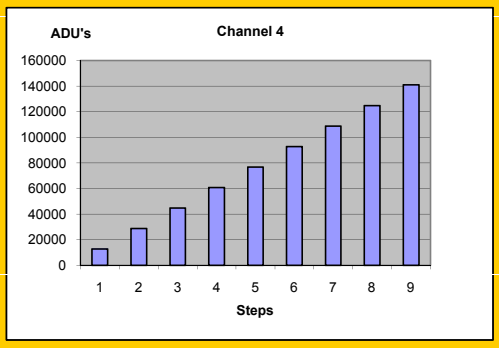
BrdTst6_006 / Channel 3					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13139	13161	13149.7	3.22014	10%
0x333	29117	29141	29130.8	3.17207	20%
0x4cc	45097	45118	45106.7	3.03925	30%
0x666	61114	61137	61125.6	3.05501	40%
0x800	77129	77151	77140.1	3.15362	50%
0x999	93109	93132	93120.4	3.22091	60%
0xb33	109127	109151	109140	3.00599	70%
0xccc	125106	125129	125118	3.19408	80%
0xe66	141127	141150	141139	3.04981	90%



TEST #6E: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

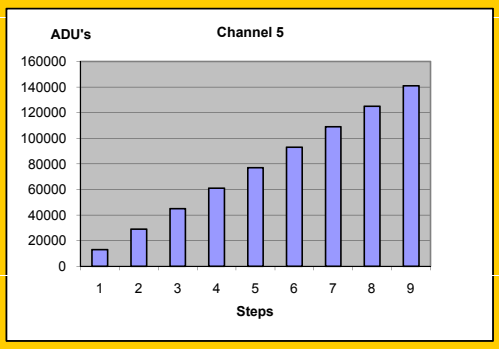
BrdTst6_006 / Channel 4					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12691	12719	12704.7	3.11615	10%
0x333	28704	28725	28714.6	3.14175	20%
0x4cc	44711	44732	44721.5	3.00671	30%
0x666	60758	60785	60770.4	3.05171	40%
0x800	76805	76826	76816.3	3.0983	50%
0x999	92813	92837	92825.1	3.18636	60%
0xb33	108862	108888	108875	3.18779	70%
0xccc	124874	124898	124885	3.1995	80%
0xe66	140923	140944	140934	3.02627	90%



TEST #6F: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

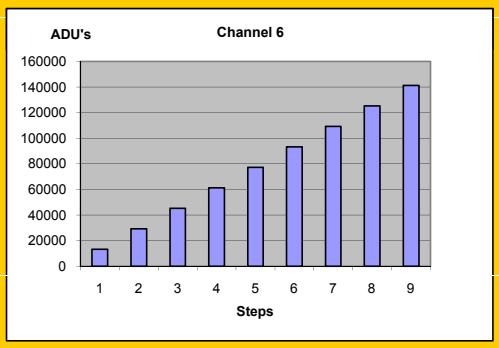
BrdTst6_006 / Channel 5					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12959	12982	12969.9	3.07744	10%
0x333	28952	28974	28962.4	2.9475	20%
0x4cc	44942	44964	44952.7	3.11615	30%
0x666	60974	60996	60984.2	3.13383	40%
0x800	76999	77021	77010.1	3.1176	50%
0x999	92990	93012	93001.6	3.10088	60%
0xb33	109023	109046	109034	3.10096	70%
0xccc	125014	125038	125027	3.21487	80%
0xe66	141047	141071	141059	3.11629	90%



TEST #6G: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

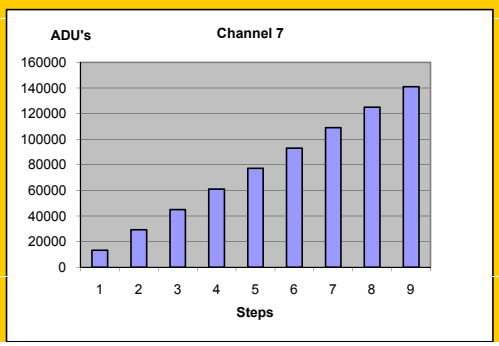
BrdTst6_006 / Channel 6					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13146	13171	13159.7	3.17745	10%
0x333	29148	29170	29158.6	3.05759	20%
0x4cc	45146	45170	45158.1	3.10259	30%
0x666	61184	61207	61195.8	3.14408	40%
0x800	77220	77246	77232.6	3.11333	50%
0x999	93223	93246	93234.1	2.94584	60%
0xb33	109264	109285	109274	3.11284	70%
0xccc	125264	125284	125273	3.14547	80%
0xe66	141302	141326	141313	3.05941	90%



TEST #6H: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

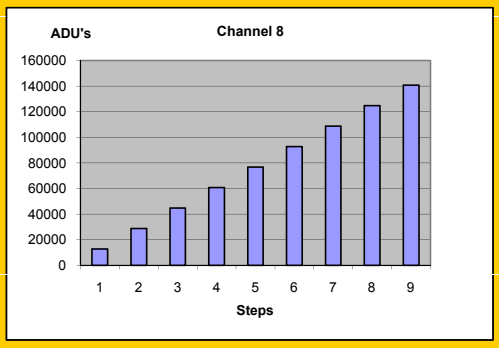
BrdTst6_006 / Channel 7					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13163	13188	13176.7	3.14137	10%
0x333	29137	29160	29149	3.23819	20%
0x4cc	45111	45135	45122.4	3.24139	30%
0x666	61122	61144	61132.5	3.26033	40%
0x800	77132	77154	77143.7	3.15899	50%
0x999	93103	93126	93114.2	3.23265	60%
0xb33	109113	109136	109125	3.08134	70%
0xccc	125088	125113	125102	3.21134	80%
0xe66	141097	141122	141111	3.21731	90%



TEST #6I: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

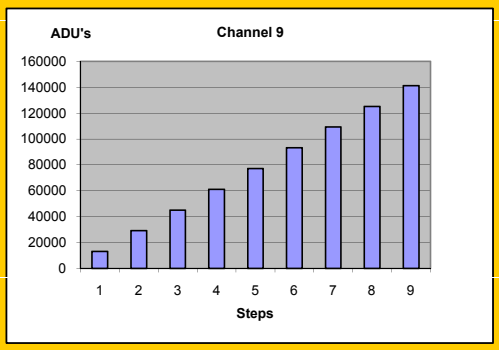
BrdTst6_006 / Channel 8					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12633	12656	12644.2	3.10599	10%
0x333	28633	28656	28644.1	2.99389	20%
0x4cc	44631	44653	44641.7	3.10811	30%
0x666	60671	60692	60681.1	3.12251	40%
0x800	76706	76726	76715.6	3.13243	50%
0x999	92704	92725	92714	3.07359	60%
0xb33	108742	108765	108754	3.0484	70%
0xccc	124743	124764	124753	3.13341	80%
0xe66	140781	140805	140793	3.15678	90%



TEST #6J: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

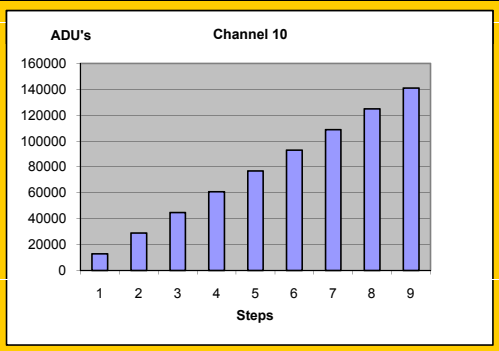
BrdTst6_006 / Channel 9					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13056	13081	13069.5	3.22612	10%
0x333	29061	29084	29072.4	3.12099	20%
0x4cc	45059	45086	45073	3.27199	30%
0x666	61103	61127	61114.7	3.22369	40%
0x800	77142	77164	77152.7	3.08556	50%
0x999	93143	93165	93153.2	3.08923	60%
0xb33	109183	109206	109195	3.24364	70%
0xccc	125185	125207	125197	3.2585	80%
0xe66	141229	141251	141240	3.21282	90%



TEST #6K: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

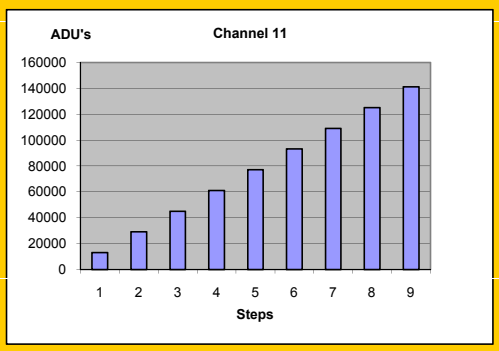
BrdTst6_006 / Channel 10					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12851	12873	12862.3	3.21549	10%
0x333	28840	28862	28851.2	3.18349	20%
0x4cc	44835	44858	44847.1	3.18022	30%
0x666	60865	60886	60876	3.18684	40%
0x800	76887	76909	76898.9	3.04494	50%
0x999	92879	92902	92890.4	3.15525	60%
0xb33	108909	108932	108920	3.1975	70%
0xccc	124907	124929	124918	3.15973	80%
0xe66	140936	140958	140947	3.22652	90%



TEST #6L: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

BrdTst6_006 / Channel 11					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13097	13120	13106.6	3.06997	10%
0x333	29089	29111	29100.3	3.22526	20%
0x4cc	45079	45101	45089.7	3.07698	30%
0x666	61113	61134	61122.9	3.03716	40%
0x800	77145	77168	77156.2	3.05024	50%
0x999	93138	93163	93149.6	3.25426	60%
0xb33	109171	109195	109183	3.24191	70%
0xccc	125164	125186	125175	3.14257	80%
0xe66	141195	141220	141207	3.16031	90%



Stage 13. Other Bit Tests. Table 11

Electronic Serial Number	0xDB8F7D		Board Serial Number	31
Firmware Version	0x193		Name Of Person Testing	S. Holm
Ident Register	0x502		Board passed Functional Tests	YES