DES 12 Channel Board - Functional Tests: CCD Acquisition Board Revision 1.0

Stage 1. Preparation of documentation and configuration settings - Table 1.

Board Part Number	30		Board Serial Number	0xDB8F9B
Date Of Tests	May 2010		Name Of Person Testing	S. Holm
Suggested Filename To Save	CCDACQ_12Ch_REPORT_BOARD16.xl		Sequence number: Test	

Stage 3. Power plane short test - Table 2.

Supply Name	Short test to ground: Impedance to ground	Test Point	
+1.2VD	48.70	TP43	~50 ohms
+1.8VD	2M	TPB12	> 1K ohm
+2.5VD	19K	TPB11	> 1K ohm
+3.3VD	18K	D13	> 1K ohm
+5VD	6K	D14	> 1K ohm
+5VA	4M	C267	> 1K ohm
-5VA	300K	C270	> 1K ohm
+15VA	500K	C288	> 1K ohm
-15VA	500K	C282	> 1K ohm
-28VA	2M	C307	> 1K ohm

Stage 4. Firmware programming tests - Table 3.

JTAG Order	Designator	Device	Load File	Check Sum or User Code
1	U122	XCF08PFS48C PROM	CcdAcqFpgaV41.mcs	0014ef670
2	U114	Spartan3 XC3S2000 FPGA	ccdacqfpgav41.bit	5102801

Stage 5. Power Consumption - Table 4.

Supply Name	Power Supply Consumption: Measured Voltage at test point	Measured Current on power supply	Test Point	
+1.2VD	1.20	N/A	TP43	
+1.8VD	1.80	N/A	TPB12	
+2.5VD	2.50	N/A	TPB11	
+3.3VD	3.29	0.228	D13	
+5VD	5.20	0.15	D14	
+5VA	4.94	0.595	C267	
-5VA	-4.97	0.434	C270	
+15VA	15.13	0.558	C288	
-15VA	-15.07	0.406	C282	
-28VA	-27.97	0.172	C307	
Vref 0+	10.01	N/A	R534	Vsub+ Reference(+10v)
Vref 0-	-2.51	N/A	R525	Vsub - Reference(-2.5v)
Vref Offset	2.50	N/A	R573	ADC Offset Reference(+2.5v)
Vclamp	1.87	N/A	VIA	ADC Clamp Voltage(+1.8v)
ADC Ref.	2.50	N/A	VIA	ADC Reference Voltage(+2.5v)
Vref 1+	2.50	N/A	R537	Vru and Vrl + Reference(+2.5v)
Vref 1-	-10.13	N/A	R535	Vru and Vrl - Reference(-10v)
Vref 2+	4.99	N/A	R563	Vog + Reference(+5v)
Vref 2-	-2.51	N/A	R555	Vog - Reference(-2.5v)
Vref 3+	2.50	N/A	R543	Vdd + Reference(+2.5v)
Vref 3-	-10.08	N/A	R571	Vdd - Reference(-10v)

Power Dissipation:
26.0 Watts

~27 watts +/- 5%

Stage 7. Basic Bus Transactions - **D**igital **Register** Tests - Table 5.

Register name	Put an X on any bit that has an error: 31-24	23-16	15-08	07-00	Function	Test name: Pattern	Walking 0's	Walking 1's
CDS Control			00000000	00000000	16 bit R/W			
Digital Output	00000000	00000000	00000000	00000000	32 bit R/W			
ADC Config.			0000	00000000	12 bit R/W			
Offset DAC			0000	00000000	12 bit R/W			
Bias DAC			0000	00000000	12 bit R/W			
Telemetry Config.				0000	4 bit R/W			
Auxilary Config.				00 00000000	10 bit R/W			
Redirect				0000	4 bit R/W			
Pixel Transfer				00000000	8 bit R/W			
Micro SEQ			00000000	00000000	16 bit R/W			
RAM Buffer			00000000	00000000	16 bit R/W			
LED Control				0000	4 bit R/W			
Control			00000000	00000000	16 bit R/W			
All Register Test	00000000	00000000	00000000	00000000	16 bit R/W	**Passed**	**Passed**	**Passed**

Stage 8. Bias Voltage settings and output enables testing - Table 8

DAC Value	410	Bias Voltage Test Data 2048	3686	50% rms Noise	10-90% Rise Time			
Signal	volts	volts	volts	uV	millisec.	Fanout Brd	Slope	Offset
Vru 0	-13.31	-5.72	1.85	<10	2	BIAS 3	216.09	3285.50
Vru 1	-13.31	-5.72	1.85	<10	2	BIAS 4	216.09	3285.50
Vru 2	-13.31	-5.72	1.85	<10	2	BIAS 5	216.09	3285.50
Vru 3	-13.31	-5.72	1.85	<10	2	BIAS 6	216.09	3285.50
Vru 4	-13.31	-5.72	1.85	<10	2	BIAS 7	216.09	3285.50
Vru 5	-13.31	-5.72	1.85	<10	2	BIAS 8	216.09	3285.50
Vru 6	-13.31	-5.72	1.85	NA	NA	BIAS 9	216.09	3285.50
Vru 7	-13.31	-5.72	1.85	NA	NA	BIAS 10	216.09	3285.50
Vrl 0	-13.31	-5.72	1.85	<10	2	BIAS 11	216.09	3285.50
Vrl 1	-13.31	-5.72	1.85	<10	2	BIAS 12	216.09	3285.50
Vrl 2	-13.31	-5.72	1.85	<10	2	BIAS 13	216.09	3285.50
Vrl 3	-13.31	-5.72	1.85	<10	2	BIAS 14	216.09	3285.50
Vrl 4	-13.31	-5.72	1.85	<10	2	BIAS 15	216.09	3285.50
Vrl 5	-13.31	-5.72	1.85	<10	2	BIAS 16	216.09	3285.50
Vrl 6	-13.31	-5.72	1.85	NA	NA	BIAS 17	216.09	3285.50
Vrl 7	-13.31	-5.72	1.85	NA	NA	BIAS 18	216.09	3285.50
Vog 0	-1.76	1.24	4.24	<10	2	BIAS 19	546.00	1370.96
Vog 1	-1.76	1.24	4.24	<10	2	BIAS 20	546.00	1370.96
Vog 2	-1.76	1.24	4.24	<10	2	BIAS 21	546.00	1370.96
Vog 3	-1.76	1.24	4.24	<10	2	BIAS 22	546.00	1370.96
Vog 4	-1.76	1.24	4.24	<10	2	BIAS 23	546.00	1370.96
Vog 5	-1.76	1.24	4.24	<10	2	BIAS 24	546.00	1370.96
Vog 6	-1.76	1.24	4.24	NA	NA	BIAS 25	546.00	1370.96
Vog 7	-1.76	1.24	4.24	NA	NA	BIAS 26	546.00	1370.96
Vdd 0	-22.02	-9.47	3.09	<10	20	BIAS 27	130.47	3283.08
Vdd 1	-22.05	-9.48	3.10	<10	20	BIAS 28	130.26	3282.42
Vdd 2	-22.08	-9.49	3.10	<10	20	BIAS 29	130.10	3282.68
Vdd 3	-22.01	-9.46	3.09	<10	20	BIAS 30	130.52	3282.70
Vdd 4	-22.13	-9.51	3.11	<10	20	BIAS 21	129.79	3282.34
Vdd 5	-22.10	-9.50	3.10	<10	20	BIAS 32	130.00	3283.00
Vdd 6	-22.09	-9.49	3.11	NA	NA	BIAS 33	130.00	3281.70
Vdd 7	-22.07	-9.49	3.10	NA	NA	BIAS 34	130.15	3282.74

Vru	Slope		Offset
Mean	216.09	Mean	3285.50
Stdev	2.842E-14	Stdev	0
Average	216.09486	Average	3285.50324
	Dac #	Average voltage	
	0	-15.0	
	4095	3.8	

Vrl	Slope		Offset
Mean	216.09	Mean	3285.50
Stdev	2.842E-14	Stdev	0
Average	216.09486	Average	3285.50324
	Dac #	Average voltage	
	0	-15.2	
	4095	3.8	

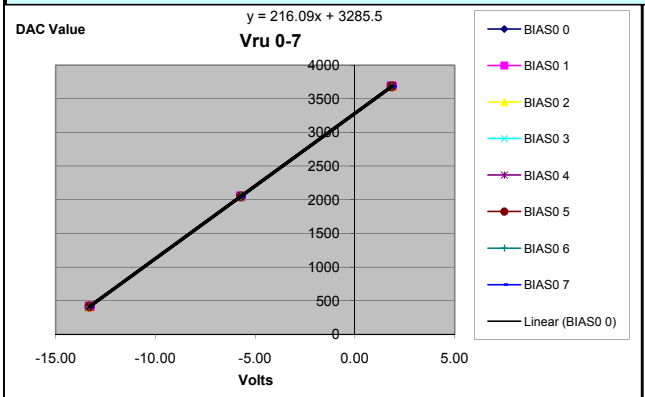
Vog	Slope		Offset
Mean	546.00	Mean	1370.96
Stdev	0	Stdev	2.27374E-13
Average	546	Average	1370.96
	Dac #	Average voltage	
	0	-2.5	
	4095	5.0	

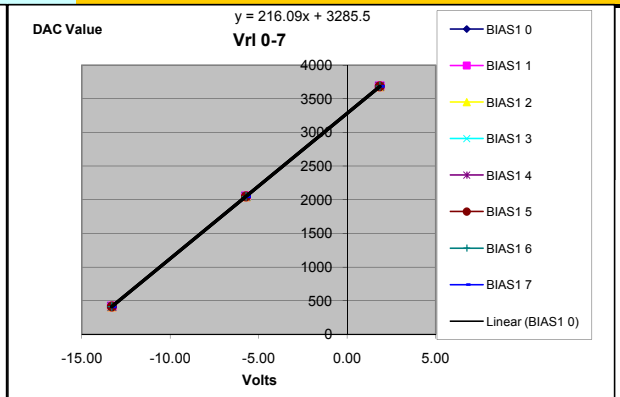
Vdd	Slope		Offset
Mean	130.16	Mean	3282.58
Stdev	0.2290732	Stdev	0.407947765
Average	130.16181	Average	3282.581274
	Dac #	Average voltage	
	0	-25.2	
	4095	6.2	

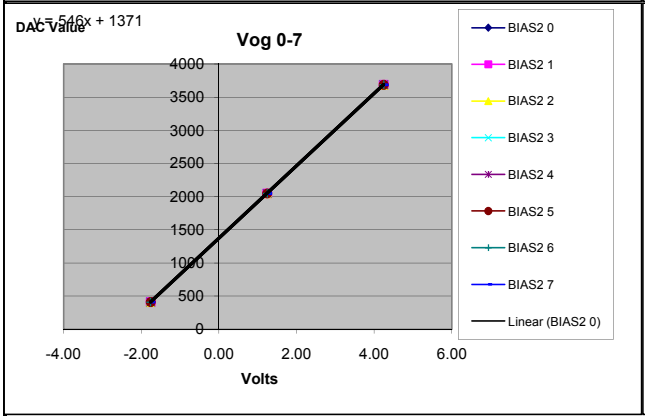
Notes and Observations

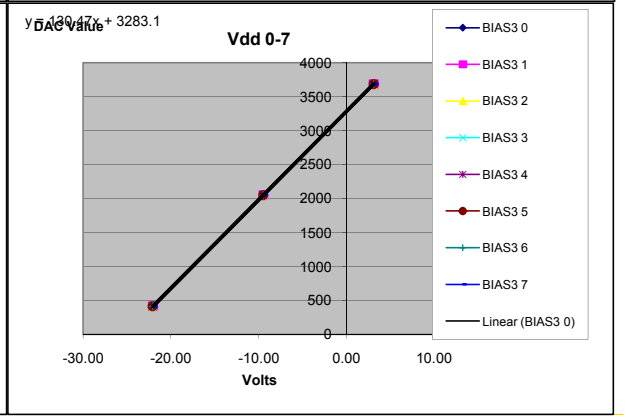
Checked for oscillations using a Agilent Oscilloscpe on AC.**OK**

average min & max voltages
(dac# -offset)/slope=voltage









Stage 8B. Telemetry System Tests - Table 7 (Bias Telemetry Tests)

DAC Value	410	3686	Bias Signals Set Volts		Resolved Values for Telemetry Channel	
	Telemetry Return Values					
Signal	10%	90%	10%	90%	Slope	Offset
Vru 0	-1764	421	-13.31	1.85	144.1293	154.36
Vru 1	-1766	420	-13.31	1.85	144.1953	153.24
Vru 2	-1764	420	-13.31	1.85	144.0633	153.48
Vru 3	-1763	420	-13.31	1.85	143.9974	153.60
Vru 4	-1770	420	-13.31	1.85	144.4591	152.75
Vru 5	-1767	420	-13.31	1.85	144.2612	153.12
Vru 6	-1767	420	-13.31	1.85	144.2612	153.12
Vru 7	-1770	420	-13.31	1.85	144.4591	152.75
Vrl 0	-1770	419	-13.31	1.85	144.3931	151.87
Vrl 1	-1771	420	-13.31	1.85	144.5251	152.63
Vrl 2	-1772	419	-13.31	1.85	144.5251	151.63
Vrl 3	-1769	419	-13.31	1.85	144.3272	151.99
Vrl 4	-1774	420	-13.31	1.85	144.7230	152.26
Vrl 5	-1770	420	-13.31	1.85	144.4591	152.75
Vrl 6	-1770	419	-13.31	1.85	144.3931	151.87
Vrl 7	-1771	419	-13.31	1.85	144.4591	151.75
Vog 0	-363	865	-1.76	4.24	204.6667	-2.79
Vog 1	-364	865	-1.76	4.24	204.8333	-3.49
Vog 2	-363	865	-1.76	4.24	204.6667	-2.79
Vog 3	-364	865	-1.76	4.24	204.8333	-3.49
Vog 4	-364	865	-1.76	4.24	204.8333	-3.49
Vog 5	-363	865	-1.76	4.24	204.6667	-2.79
Vog 6	-363	865	-1.76	4.24	204.6667	-2.79
Vog 7	-364	865	-1.76	4.24	204.8333	-3.49
Vdd 0	-1739	571	-22.02	3.09	91.9952	286.73
Vdd 1	-1747	572	-22.05	3.10	92.2068	286.16
Vdd 2	-1752	573	-22.08	3.10	92.3352	286.76
Vdd 3	-1738	572	-22.01	3.09	92.0319	287.62
Vdd 4	-1753	573	-22.13	3.11	92.1553	286.40
Vdd 5	-1745	573	-22.10	3.10	91.9841	287.85
Vdd 6	-1750	573	-22.09	3.11	92.1825	286.31
Vdd 7	-1754	573	-22.07	3.10	92.4513	286.40

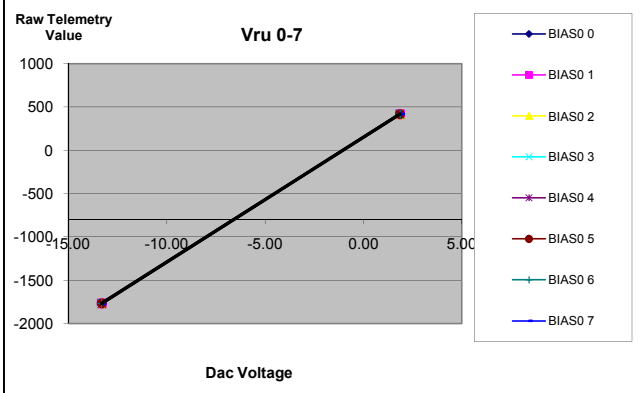
AVERAGE

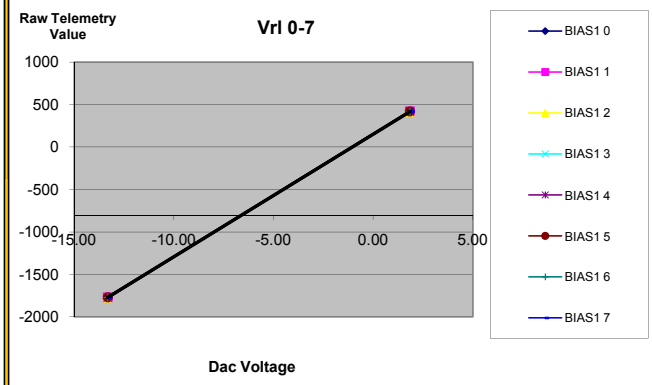
Vru	Slope		Offset
Mean	144.23	Mean	153.30
Stdev	0.1581739	Stdev	0.4906774

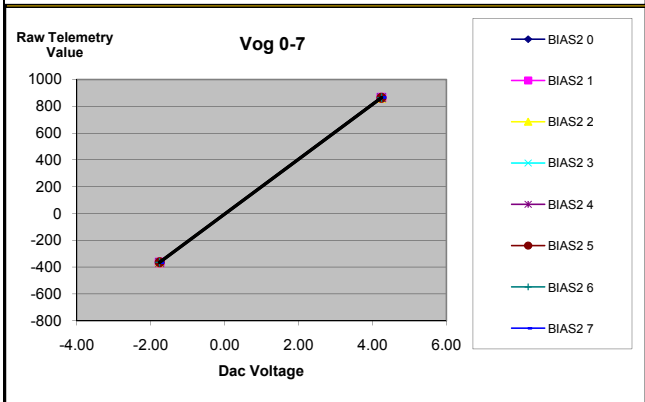
Vrl	Slope		Offset
Mean	144.48	Mean	152.10
Stdev	0.113055	Stdev	0.3853061

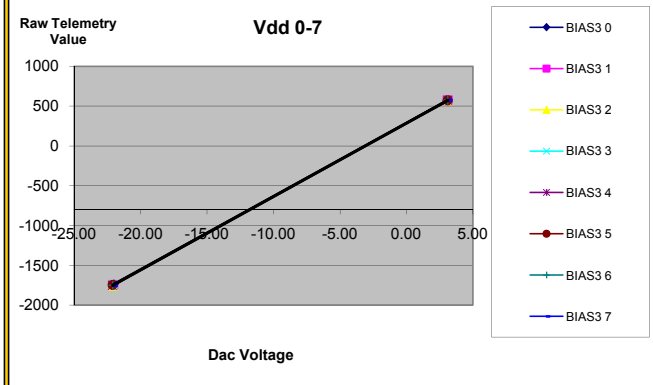
Vog	Slope		Offset
Mean	204.75	Mean	-3.14
Stdev	0.0833333	Stdev	0.3533333

Vdd	Slope		Offset
Mean	92.17	Mean	286.78
Stdev	0.1550382	Stdev	0.5861437









Stage 8C. Bias Voltage output enables testing - Table 8

Place a line through Bias Voltage name if enable/disable switch works

Vru 0	Vru 1	Vru 2	Vru 3	Vru 4	Vru 5
Vrl 0	Vrl 1	Vrl 2	Vrl 3	Vrl 4	Vrl 5
Vog 0	Vog 1	Vog 2	Vog 3	Vog 4	Vog 5
Vdd 0	Vdd 1	Vdd 2	Vdd 3	Vdd 4	Vdd 5

Stage 9. Vsub and Heater Control testing - Table 9

DAC Value	Vsub Measured Voltage Test Data 10%	50%	90%
Signal	volts	volts	volts
Vsub - rate	-1.26	3.74	8.74
Vsub - Limit	-1.26	3.74	8.74
Vsub0	0.00	0.00	0.00
	Vsub Enable Bit - pass		

DAC Value	Telemetery Readback Test Data 10%	50%	90%
Signal	dec	dec	dec
Vbias 0	154	266	448
Vbias 1	-28	692	1413
RTD1	219	NA	NA
RTD2	248	NA	NA
RTD3	277	NA	NA
RTD4	301	NA	NA
RTD5	323	NA	NA
RTD6	351	NA	NA
Reference 4096	836	NA	NA
eference buffere	836	NA	NA

Stage 10. Video Offset DAC Tests - Table 10.

	DAC Value 410				DAC Value 2048				DAC Value 3686			
ADC	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU
0	0.250	NA	NA	17159	1.250		NA	81100	2.250	NA	500ms	145044
1	0.250	NA	NA	17087	1.250		NA	81055	2.250	NA	500ms	145023
2	0.250	NA	NA	17036	1.250		NA	81086	2.250	NA	500ms	145135
3	0.250	NA	NA	17063	1.250		NA	81043	2.250	NA	500ms	145015
4	0.250	NA	NA	17125	1.250		NA	81160	2.250	NA	500ms	145204
5	0.250	NA	NA	17143	1.250		NA	81125	2.250	NA	500ms	145100
6	0.250	NA	NA	17233	1.250		NA	81226	2.250	NA	500ms	145214
7	0.250	NA	NA	17149	1.250		NA	81165	2.250	NA	500ms	145179
8	0.250	NA	NA	17150	1.250		NA	81199	2.250	NA	500ms	145246
9	0.250	NA	NA	16995	1.250		NA	81075	2.250	NA	500ms	145161
10	0.250	NA	NA	17065	1.250		NA	81053	2.250	NA	500ms	145039
11	0.250	NA	NA	17066	1.250		NA	81059	2.250	NA	500ms	145038

ADC	DC Volts		Data Set		
Channel	Slope	Offset	410	2048	3686
0	1638.000	0.500	0.250	1.250	2.250
1	1638.000	0.500	0.250	1.250	2.250
2	1638.000	0.500	0.250	1.250	2.250
3	1638.000	0.500	0.250	1.250	2.250
4	1638.000	0.500	0.250	1.250	2.250
5	1638.000	0.500	0.250	1.250	2.250
6	1638.000	0.500	0.250	1.250	2.250
7	1638.000	0.500	0.250	1.250	2.250
8	1638.000	0.500	0.250	1.250	2.250
9	1638.000	0.500	0.250	1.250	2.250
10	1638.000	0.500	0.250	1.250	2.250
11	1638.000	0.500	0.250	1.250	2.250

(dac# -offset)/slope=Voltage

ADC	ADU's		Data Set		
Channel	Slope	Offset	410	2048	3686
0	0.026	-29.55	17159	81100	145044
1	0.026	-27.54	17087	81055	145023
2	0.026	-25.68	17036	81086	145135
3	0.026	-26.90	17063	81043	145015
4	0.026	-27.98	17125	81160	145204
5	0.026	-28.93	17143	81125	145100
6	0.026	-31.14	17233	81226	145214
7	0.026	-28.81	17149	81165	145179
8	0.026	-28.61	17150	81199	145246
9	0.026	-24.38	16995	81075	145161
10	0.026	-26.85	17065	81053	145039
11	0.026	-26.94	17066	81059	145038

(dac# -offset)/slope=ADU

Notes and Observations

Checked for oscillations using a Agilent Oscilloscope on AC. OK

Stage 11. CDS Control Functions and Video Channel Performanc

TEST #1: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit is held static. The purpose of this test is to verify the correct operation of the ADC devices and measure the noise of the Offset voltage generators, ADC buffer amplifiers and ADC devices

Noise Test 1

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	81087	8.11E+04	81095.4	2.22533
CH 1	81042	8.11E+04	81050.8	2.3704
CH 2	81074	8.11E+04	81080.3	2.24482
CH 3	81033	8.10E+04	81040.7	2.28903
CH 4	81151	8.12E+04	81160.3	2.25326
CH 5	81113	8.11E+04	81120.9	2.31403
CH 6	81216	8.12E+04	81222.7	2.24596
CH 7	81157	8.12E+04	81164.9	2.36878
CH 8	81188	8.12E+04	81195.3	2.2209
CH 9	81066	81082	81074.2	2.13709
CH 10	81046	81062	81053.2	2.27728
CH 11	81044	81062	81053.5	2.23868

TEST #2: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the invert/non-invert and the DC Restore switches are held static.

Noise Test 2

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76339	7.64E+04	76349.4	2.83779
CH 1	76900	7.69E+04	76911.5	2.84354
CH 2	76625	7.66E+04	76634.2	2.81513
CH 3	76758	7.68E+04	76767.8	2.78441
CH 4	76508	7.65E+04	76518.6	2.69437
CH 5	76705	7.67E+04	76715.8	2.82351
CH 6	76936	7.70E+04	76945.7	2.78331
CH 7	77081	7.71E+04	77091.6	2.69307
CH 8	76782	7.68E+04	76792.1	2.73775
CH 9	76500	76520	76511.3	2.80293
CH 10	76564	76584	76572.9	2.80556
CH 11	76753	76775	76763.6	2.78126

TEST #3: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the DC Restore switch is held static.

Noise Test 3

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76336	7.64E+04	76347.6	3.04745
CH 1	76898	7.69E+04	76908.6	2.99937
CH 2	76623	7.66E+04	76632.8	3.00315
CH 3	76749	7.68E+04	76758.3	2.96397
CH 4	76507	7.65E+04	76516.5	2.8444
CH 5	76690	7.67E+04	76700.6	3.10695
CH 6	76923	7.69E+04	76934.8	3.08626
CH 7	77078	7.71E+04	77088	3.01254
CH 8	76782	7.68E+04	76793.9	3.04014
CH 9	76488	76512	76499.4	3.0661
CH 10	76570	76590	76579.3	2.96885
CH 11	76748	76770	76758.9	2.9849

TEST #4: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition.

Noise Test 4

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76327	7.63E+04	76338.8	3.15202
CH 1	76901	7.69E+04	76911.5	3.20655
CH 2	76625	7.66E+04	76636.3	3.06851
CH 3	76747	7.68E+04	76759.8	3.05222
CH 4	76540	7.66E+04	76549.9	2.99451
CH 5	76676	7.67E+04	76687.2	3.1866
CH 6	76932	7.70E+04	76944.7	3.17737
CH 7	77032	7.71E+04	77042.9	3.24133
CH 8	76825	7.68E+04	76836.3	3.05298
CH 9	76397	76420	76409.2	3.22744
CH 10	76589	76609	76599	3.03523
CH 11	76707	76729	76717.6	3.09881

TEST #5: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the circuitry set to high GAIN.

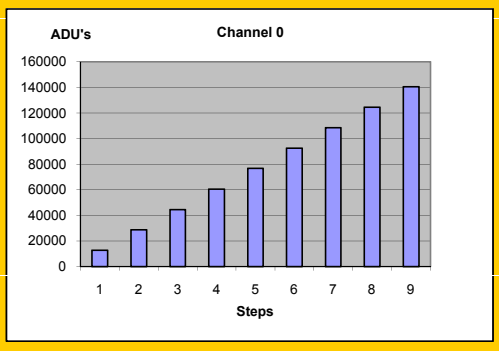
Noise Test 5

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76338	7.64E+04	76350.1	3.63382
CH 1	76912	7.69E+04	76924.9	3.69599
CH 2	76640	7.67E+04	76653.6	3.61947
CH 3	76753	7.68E+04	76765.5	3.6488
CH 4	76543	7.66E+04	76555.6	3.67185
CH 5	76674	7.67E+04	76686.4	3.69483
CH 6	76934	7.70E+04	76946.6	3.68116
CH 7	77031	7.71E+04	77044.1	3.67472
CH 8	76874	7.69E+04	76887.2	3.63878
CH 9	76397	76424	76409.6	3.77666
CH 10	76652	76676	76663.4	3.63846
CH 11	76702	76730	76717.5	3.63981

TEST #6A: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

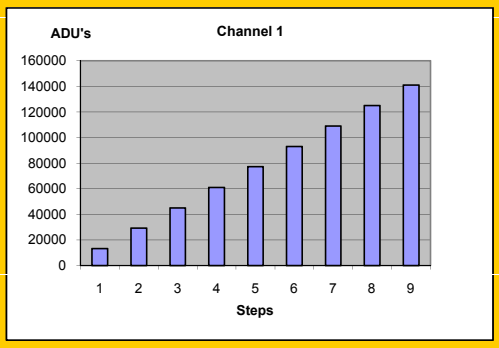
BrdTst6_006 / Channel 0					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12690	12712	12701.6	3.14253	10%
0x333	28655	28676	28666.1	3.13574	20%
0x4cc	44616	44638	44627.9	3.06395	30%
0x666	60619	60643	60632	3.10269	40%
0x800	76630	76652	76641.1	3.12325	50%
0x999	92597	92619	92609	3.07758	60%
0xb33	108602	108626	108614	3.25853	70%
0xccc	124569	124592	124579	3.16543	80%
0xe66	140570	140596	140583	3.13646	90%



TEST #6B: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

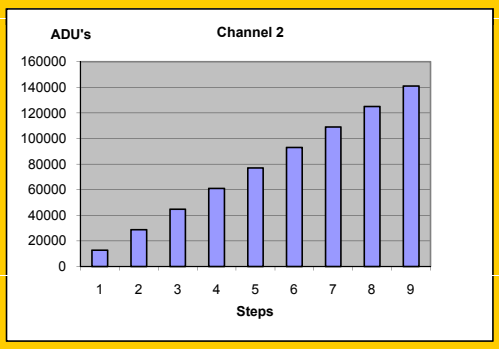
BrdTst6_006 / Channel 1					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13173	13197	13185	3.15053	10%
0x333	29142	29167	29155.4	2.95845	20%
0x4cc	45116	45138	45128.2	3.1265	30%
0x666	61125	61150	61137.4	3.08099	40%
0x800	77139	77160	77149.3	3.16282	50%
0x999	93110	93136	93122.6	3.16277	60%
0xb33	109121	109144	109133	3.16339	70%
0xccc	125097	125122	125109	3.34894	80%
0xe66	141106	141129	141117	3.21141	90%



TEST #6C: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

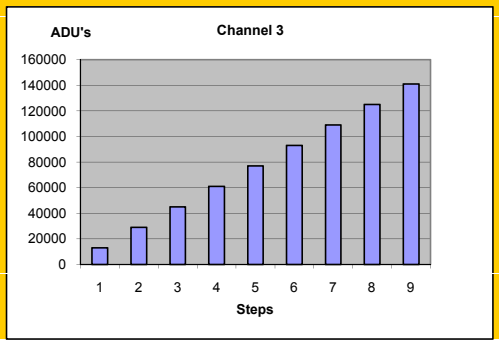
BrdTst6_006 / Channel 2					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12864	12885	12873.8	3.10975	10%
0x333	28854	28876	28865.1	3.18127	20%
0x4cc	44848	44870	44859.9	3.21959	30%
0x666	60881	60903	60891	3.19016	40%
0x800	76912	76936	76922.7	3.16891	50%
0x999	92906	92930	92916.8	2.99617	60%
0xb33	108936	108960	108948	3.0013	70%
0xccc	124936	124956	124946	3.04951	80%
0xe66	140966	140988	140978	3.01641	90%



TEST #6D: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

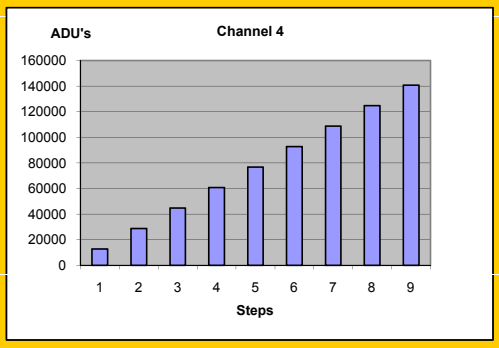
BrdTst6_006 / Channel 3					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13001	13026	13014.1	3.26137	10%
0x333	28980	29001	28989.5	3.1361	20%
0x4cc	44954	44977	44964.2	3.10792	30%
0x666	60967	60988	60977.7	3.16473	40%
0x800	76977	76999	76987.6	3.18325	50%
0x999	92952	92973	92962.9	2.96084	60%
0xb33	108967	108990	108978	3.01866	70%
0xccc	124942	124966	124955	3.21231	80%
0xe66	140957	140983	140970	3.18066	90%



TEST #6E: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

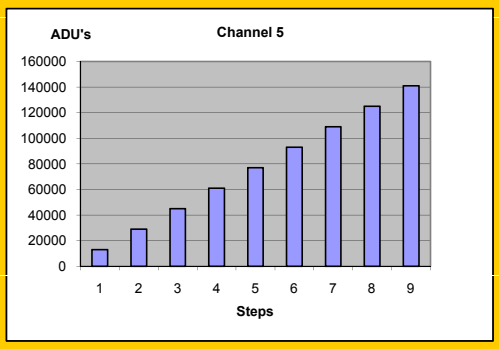
BrdTst6_006 / Channel 4					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12797	12818	12806.8	3.00814	10%
0x333	28788	28810	28797.7	3.15779	20%
0x4cc	44773	44795	44784.4	3.04177	30%
0x666	60804	60824	60814	3.05526	40%
0x800	76829	76852	76840.6	3.07508	50%
0x999	92822	92844	92832.4	3.10402	60%
0xb33	108853	108875	108864	3.0554	70%
0xccc	124843	124866	124855	3.02654	80%
0xe66	140874	140895	140884	3.10743	90%



TEST #6F: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

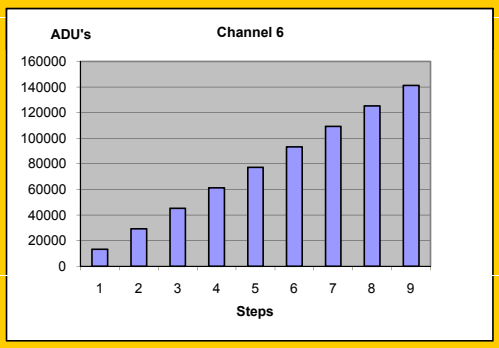
BrdTst6_006 / Channel 5					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12957	12980	12967.9	3.24153	10%
0x333	28931	28955	28942.5	3.19827	20%
0x4cc	44902	44926	44914.3	3.12175	30%
0x666	60917	60939	60928.5	3.03369	40%
0x800	76928	76950	76939.2	3.21621	50%
0x999	92900	92924	92913.1	3.19013	60%
0xb33	108916	108939	108928	3.15773	70%
0xccc	124892	124913	124902	3.04422	80%
0xe66	140906	140927	140916	3.13383	90%



TEST #6G: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

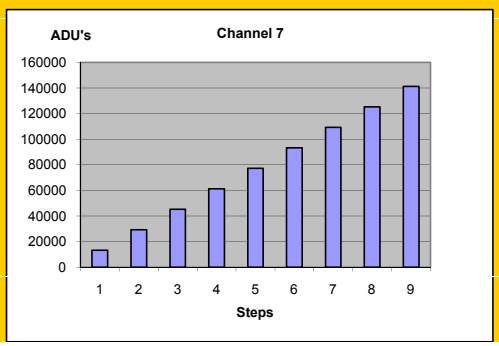
BrdTst6_006 / Channel 6					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13188	13212	13199.8	3.17634	10%
0x333	29164	29186	29175.8	3.17996	20%
0x4cc	45139	45163	45151.1	3.29645	30%
0x666	61154	61178	61167	3.21127	40%
0x800	77169	77194	77180.9	3.20585	50%
0x999	93146	93172	93159	3.1539	60%
0xb33	109163	109188	109175	3.2122	70%
0xccc	125144	125165	125154	3.05023	80%
0xe66	141156	141182	141169	3.09742	90%



TEST #6H: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

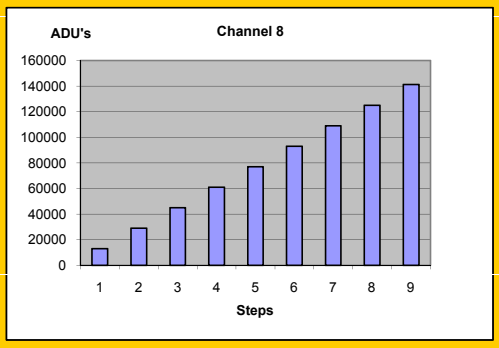
BrdTst6_006 / Channel 7					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13261	13284	13273.2	3.13427	10%
0x333	29245	29268	29257.5	3.24959	20%
0x4cc	45227	45250	45238.3	3.26162	30%
0x666	61251	61272	61261.6	3.13267	40%
0x800	77269	77291	77279.9	3.2499	50%
0x999	93249	93276	93261.7	3.19974	60%
0xb33	109275	109298	109287	3.13267	70%
0xccc	125258	125284	125271	3.12064	80%
0xe66	141286	141308	141296	3.18735	90%



TEST #6I: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

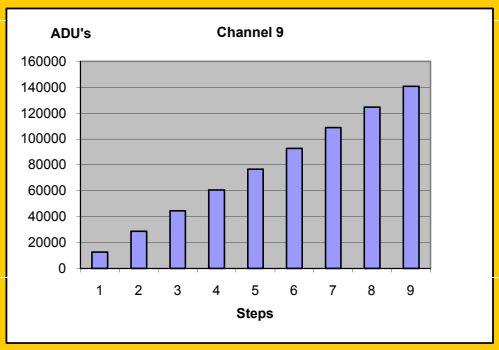
BrdTst6_006 / Channel 8					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13042	13065	13052.9	3.11851	10%
0x333	29035	29057	29045.3	3.04654	20%
0x4cc	45024	45045	45035.2	3.16556	30%
0x666	61057	61080	61067.7	3.08577	40%
0x800	77086	77106	77095.9	3.07029	50%
0x999	93078	93099	93088.7	3.09356	60%
0xb33	109111	109133	109122	2.95924	70%
0xccc	125103	125127	125115	3.17712	80%
0xe66	141133	141158	141147	3.16242	90%



TEST #6J: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

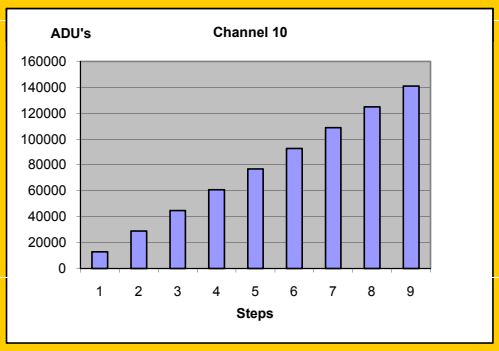
BrdTst6_006 / Channel 9					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12590	12614	12603.4	3.18491	10%
0x333	28594	28618	28607.4	3.30271	20%
0x4cc	44593	44618	44605.9	3.38404	30%
0x666	60636	60658	60647.6	3.25829	40%
0x800	76674	76696	76684.4	3.23228	50%
0x999	92674	92696	92685	3.22942	60%
0xb33	108717	108741	108729	3.26053	70%
0xccc	124717	124740	124729	3.32416	80%
0xe66	140759	140784	140771	3.14638	90%



TEST #6K: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

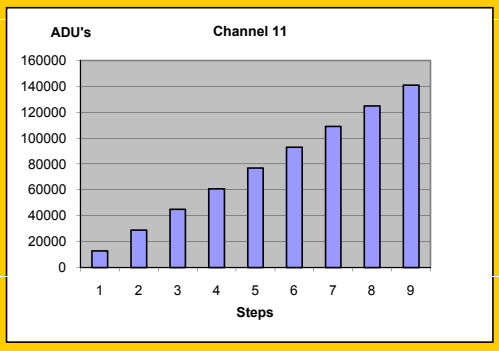
BrdTst6_006 / Channel 10					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12868	12893	12879.3	3.0713	10%
0x333	28844	28868	28856.3	3.09689	20%
0x4cc	44816	44842	44831.4	3.22459	30%
0x666	60837	60858	60848.2	3.06909	40%
0x800	76851	76874	76863.1	3.08365	50%
0x999	92830	92852	92841.9	3.12882	60%
0xb33	108848	108871	108859	3.16608	70%
0xccc	124825	124851	124837	3.14258	80%
0xe66	140841	140863	140852	3.03026	90%



TEST #6L: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

BrdTst6_006 / Channel 11					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12982	13005	12993.6	3.03145	10%
0x333	28960	28983	28970.2	3.16677	20%
0x4cc	44934	44958	44945.6	3.21878	30%
0x666	60952	60974	60962.5	2.87432	40%
0x800	76960	76983	76971.1	3.21637	50%
0x999	92934	92958	92947.8	2.99355	60%
0xb33	108952	108976	108964	2.92512	70%
0xccc	124933	124954	124944	3.17836	80%
0xe66	140947	140970	140959	3.12128	90%



Stage 13. Other Bit Tests. Table 11

Electronic Serial Number	0xDB8F9B		Board Serial Number	30
Firmware Version	0x193		Name Of Person Testing	S. Holm
Ident Register	0x502		Board passed Functional Tests	YES