DES 12 Channel Board - Functional Tests: CCD Acquisition Board Revision 1.0

Stage 1. Preparation of documentation and configuration settings - Table 1.

Board Part Number	11		Board Serial Number	0xDB6FB0
Date Of Tests	July 2010		Name Of Person Testing	S. Holm
Suggested Filename To Save	CCDACQ_12Ch_REPORT_BOARD12.xl		Sequence number: Test	

Stage 3. Power plane short test - Table 2.

Supply Name	Short test to ground: Impedance to ground	Test Point	
+1.2VD	78.90	TP43	~50 ohms
+1.8VD	2M	TPB12	> 1K ohm
+2.5VD	19K	TPB11	> 1K ohm
+3.3VD	6K	D13	> 1K ohm
+5VD	19K	D14	> 1K ohm
+5VA	4M	C267	> 1K ohm
-5VA	300K	C270	> 1K ohm
+15VA	500K	C288	> 1K ohm
-15VA	500K	C282	> 1K ohm
-28VA	2.6M	C307	> 1K ohm

Stage 4. Firmware programming tests - Table 3.

JTAG Order	Designator	Device	Load File	Check Sum or User Code
1	U122	XCF08PFS48C PROM	CcdAcqFpgaV41.mcs	0014ef670
2	U114	Spartan3 XC3S2000 FPGA	ccdacqfpgav41.bit	5102801

Stage 5. Power Consumption - Table 4.

Supply Name	Power Supply Consumption: Measured Voltage at test point	Measured Current on power supply	Test Point	
+1.2VD	1.20	N/A	TP43	
+1.8VD	1.80	N/A	TPB12	
+2.5VD	2.51	N/A	TPB11	
+3.3VD	3.30	0.082	D13	
+5VD	5.20	0.15	D14	
+5VA	5.05	0.56	C267	
-5VA	-5.00	0.43	C270	
+15VA	15.00	0.56	C288	
-15VA	-15.07	0.4	C282	
-28VA	-18.00	0.22	C307	
Vref 0+	10.07	N/A	R534	Vsub+ Reference(+10v)
Vref 0-	-2.51	N/A	R525	Vsub - Reference(-2.5v)
Vref Offset	2.50	N/A	R573	ADC Offset Reference(+2.5v)
Vclamp	1.88	N/A	VIA	ADC Clamp Voltage(+1.8v)
ADC Ref.	2.50	N/A	VIA	ADC Reference Voltage(+2.5v)
Vref 1+	2.50	N/A	R537	Vru and Vrl + Reference(+2.5v)
Vref 1-	-10.05	N/A	R535	Vru and Vrl - Reference(-10v)
Vref 2+	5.01	N/A	R563	Vog + Reference(+5v)
Vref 2-	-2.51	N/A	R555	Vog - Reference(-2.5v)
Vref 3+	2.50	N/A	R543	Vdd + Reference(+2.5v)
Vref 3-	-10.10	N/A	R571	Vdd - Reference(-10v)

Power Dissipation:
24.4 Watts

~27 watts +/- 5%

Stage 7. Basic Bus Transactions - **D**igital **Register** Tests - Table 5.

Register name	Put an X on any bit that has an error: 31-24	23-16	15-08	07-00	Function	Test name: Pattern	Walking 0's	Walking 1's
CDS Control			00000000	00000000	16 bit R/W			
Digital Output	00000000	00000000	00000000	00000000	32 bit R/W			
ADC Config.			0000	00000000	12 bit R/W			
Offset DAC			0000	00000000	12 bit R/W			
Bias DAC			0000	00000000	12 bit R/W			
Telemetry Config.				0000	4 bit R/W			
Auxilary Config.				00 00000000	10 bit R/W			
Redirect				0000	4 bit R/W			
Pixel Transfer				00000000	8 bit R/W			
Micro SEQ			00000000	00000000	16 bit R/W			
RAM Buffer			00000000	00000000	16 bit R/W			
LED Control				0000	4 bit R/W			
Control			00000000	00000000	16 bit R/W			
All Register Test	00000000	00000000	00000000	00000000	16 bit R/W	**Passed**	**Passed**	**Passed**

Stage 8. Bias Voltage settings and output enables testing - Table 8

DAC Value	410	Bias Voltage Test Data 2048	3686	50% rms Noise	10-90% Rise Time			
Signal	volts	volts	volts	uV	millisec.	Fanout Brd	Slope	Offset
Vru 0	-13.20	-5.67	1.86	<10	1	BIAS 3	217.53	3281.39
Vru 1	-13.20	-5.66	1.86	<10	1	BIAS 4	217.53	3280.67
Vru 2	-13.20	-5.66	1.86	<10	1	BIAS 5	217.53	3280.67
Vru 3	-13.22	-5.67	1.86	<10	1	BIAS 6	217.24	3281.21
Vru 4	-13.20	-5.67	1.86	<10	1	BIAS 7	217.53	3281.39
Vru 5	-13.21	-5.67	1.86	<10	1	BIAS 8	217.39	3281.30
Vru 6	-13.21	-5.67	1.86	NA	NA	BIAS 9	217.39	3281.30
Vru 7	-13.20	-5.67	1.86	NA	NA	BIAS 10	217.53	3281.39
Vrl 0	-13.20	-5.66	1.86	<10	1	BIAS 11	217.53	3280.67
Vrl 1	-13.20	-5.67	1.86	<10	1	BIAS 12	217.53	3281.39
Vrl 2	-13.22	-5.67	1.86	<10	1	BIAS 13	217.24	3281.21
Vrl 3	-13.19	-5.66	1.86	<10	1	BIAS 14	217.67	3280.76
Vrl 4	-13.19	-5.66	1.86	<10	1	BIAS 15	217.67	3280.76
Vrl 5	-13.21	-5.67	1.86	<10	1	BIAS 16	217.39	3281.30
Vrl 6	-13.22	-5.67	1.86	NA	NA	BIAS 17	217.24	3281.21
Vrl 7	-13.19	-5.67	1.86	NA	NA	BIAS 18	217.67	3281.49
Vog 0	-1.76	1.25	4.26	<10	1	BIAS 19	544.19	1367.77
Vog 1	-1.76	1.25	4.26	<10	1	BIAS 20	544.19	1367.77
Vog 2	-1.75	1.25	4.26	<10	1	BIAS 21	545.09	1364.82
Vog 3	-1.76	1.25	4.26	<10	1	BIAS 22	544.19	1367.77
Vog 4	-1.76	1.25	4.26	<10	1	BIAS 23	544.19	1367.77
Vog 5	-1.75	1.25	4.26	<10	1	BIAS 24	545.09	1364.82
Vog 6	-1.76	1.25	4.26	NA	NA	BIAS 25	544.19	1367.77
Vog 7	-1.75	1.25	4.26	NA	NA	BIAS 26	545.09	1364.82
Vdd 0	-22.13	-9.52	3.09	<10	20	BIAS 27	129.90	3284.62
Vdd 1	-22.18	-9.54	3.10	<10	20	BIAS 28	129.59	3284.28
Vdd 2	-22.17	-9.54	3.10	<10	20	BIAS 29	129.64	3284.33
Vdd 3	-22.11	-9.51	3.09	<10	20	BIAS 30	130.00	3284.30
Vdd 4	-22.07	-9.49	3.09	<10	20	BIAS 21	130.21	3283.66
Vdd 5	-22.13	-9.52	3.09	<10	20	BIAS 32	129.90	3284.62
Vdd 6	-22.16	-9.53	3.10	NA	NA	BIAS 33	129.69	3283.96
Vdd 7	-22.18	-9.54	3.10	NA	NA	BIAS 34	129.59	3284.28

Vru	Slope		Offset
Mean	217.46	Mean	3281.17
Stdev	0.1020343	Stdev	0.293491261
Average	217.45768	Average	3281.165934
	Dac #	Average voltage	
	0	-15.0	
	4095	3.7	

Vrl	Slope		Offset
Mean	217.49	Mean	3281.10
Stdev	0.1731034	Stdev	0.298715318
Average	217.49385	Average	3281.098649
	Dac #	Average voltage	
	0	-15.1	
	4095	3.7	

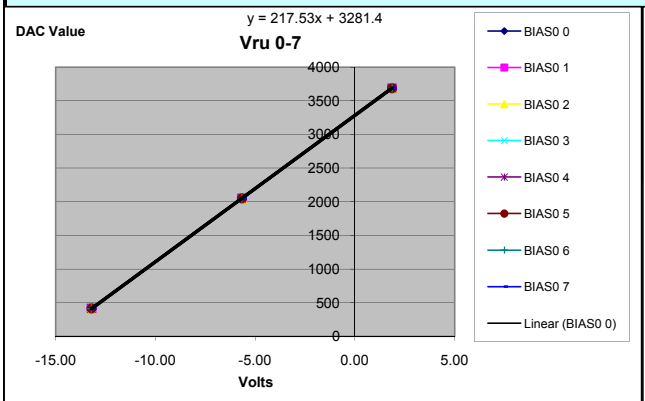
Vog	Slope		Offset
Mean	544.53	Mean	1366.66
Stdev	0.4381141	Stdev	1.427279463
Average	544.52541	Average	1366.661876
	Dac #	Average voltage	
	0	-2.5	
	4095	5.0	

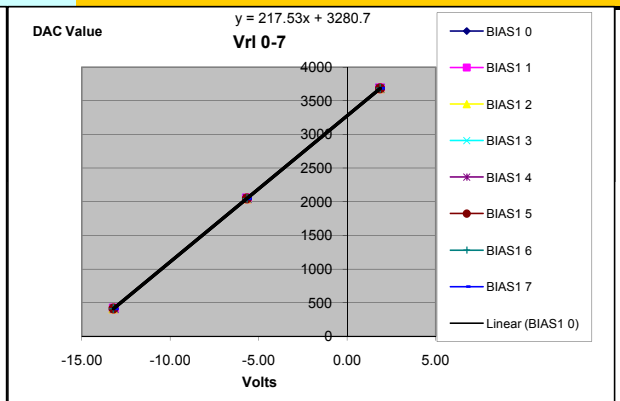
Vdd	Slope		Offset
Mean	129.81	Mean	3284.25
Stdev	0.209026	Stdev	0.298797101
Average	129.8136	Average	3284.254838
	Dac #	Average voltage	
	0	-25.3	
	4095	6.3	

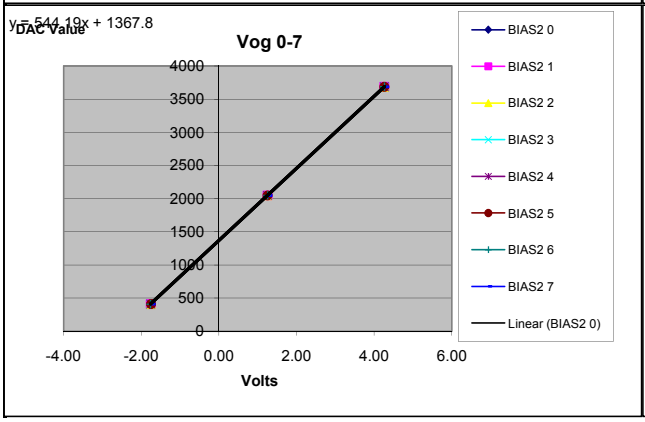
Notes and Observations

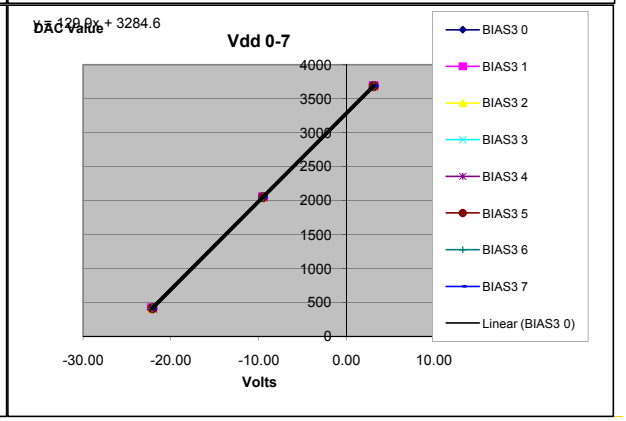
Checked for oscillations using a Agilent Oscilloscpe on AC.**OK**

average min & max voltages
(dac# -offset)/slope=voltage









Stage 8B. Telemetry System Tests - Table 7 (Bias Telemetry Tests)

DAC Value: 410 / 3686

Signal	Telemetry Return Values 10%	90%	Bias Signals Set Volts 10%	90%	Resolved Values for Telemetry Channel Slope	Offset
Vru 0	-1750	421	-13.20	1.86	144.1567	152.87
Vru 1	-1751	421	-13.20	1.86	144.2231	152.75
Vru 2	-1750	421	-13.20	1.86	144.1567	152.87
Vru 3	-1752	422	-13.22	1.86	144.1645	153.85
Vru 4	-1749	421	-13.20	1.86	144.0903	152.99
Vru 5	-1752	422	-13.21	1.86	144.2601	153.68
Vru 6	-1755	421	-13.21	1.86	144.3928	152.43
Vru 7	-1751	422	-13.20	1.86	144.2895	153.62
Vrl 0	-1741	423	-13.20	1.86	143.6919	155.73
Vrl 1	-1743	422	-13.20	1.86	143.7583	154.61
Vrl 2	-1747	423	-13.22	1.86	143.8992	155.35
Vrl 3	-1743	423	-13.19	1.86	143.9203	155.31
Vrl 4	-1747	423	-13.19	1.86	144.1860	154.81
Vrl 5	-1747	423	-13.21	1.86	143.9947	155.17
Vrl 6	-1745	423	-13.22	1.86	143.7666	155.59
Vrl 7	-1748	423	-13.19	1.86	144.2525	154.69
Vog 0	-364	869	-1.76	4.26	204.8173	-3.52
Vog 1	-364	869	-1.76	4.26	204.8173	-3.52
Vog 2	-364	870	-1.75	4.26	205.3245	-4.68
Vog 3	-364	870	-1.76	4.26	204.9834	-3.23
Vog 4	-363	870	-1.76	4.26	204.8173	-2.52
Vog 5	-363	870	-1.75	4.26	205.1581	-3.97
Vog 6	-364	869	-1.76	4.26	204.8173	-3.52
Vog 7	-362	869	-1.75	4.26	204.8253	-3.56
Vdd 0	-1765	572	-22.13	3.09	92.6646	285.67
Vdd 1	-1766	573	-22.18	3.10	92.5237	286.18
Vdd 2	-1766	572	-22.17	3.10	92.5208	285.19
Vdd 3	-1758	572	-22.11	3.09	92.4603	286.30
Vdd 4	-1755	571	-22.07	3.09	92.4483	285.33
Vdd 5	-1769	573	-22.13	3.09	92.8628	286.05
Vdd 6	-1762	573	-22.16	3.10	92.4386	286.44
Vdd 7	-1770	573	-22.18	3.10	92.6820	285.69

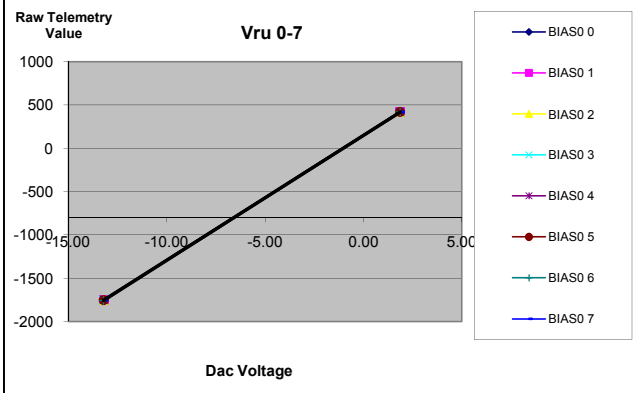
AVERAGE

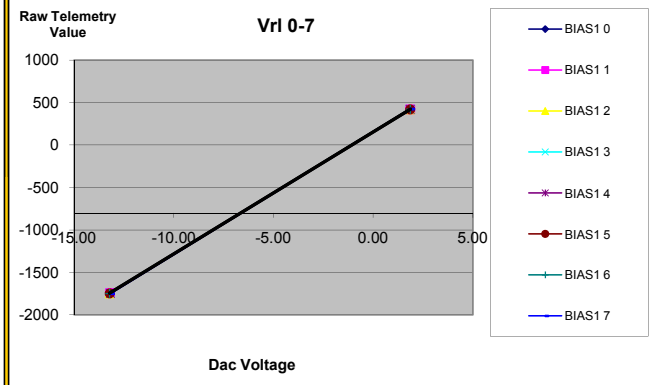
Vru	Slope		Offset
Mean	144.22	Mean	153.13
Stdev	0.0895501	Stdev	0.4820692

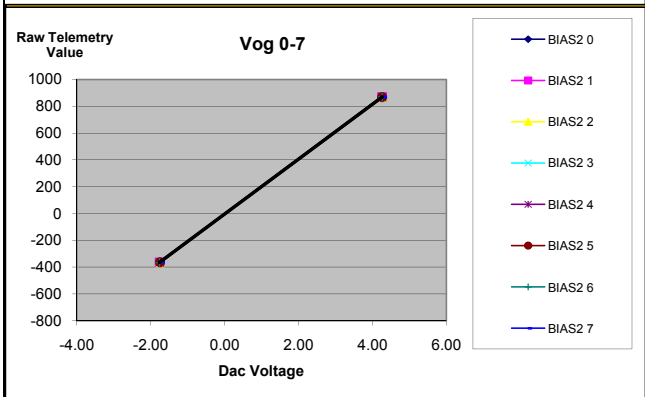
Vrl	Slope		Offset
Mean	143.93	Mean	155.16
Stdev	0.1895916	Stdev	0.390098

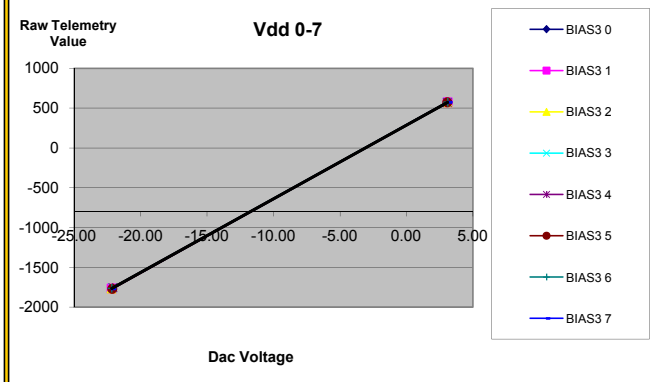
Vog	Slope		Offset
Mean	204.95	Mean	-3.57
Stdev	0.1838634	Stdev	0.5725015

Vdd	Slope		Offset
Mean	92.58	Mean	285.86
Stdev	0.1394872	Stdev	0.427821









Stage 8C. Bias Voltage output enables testing - Table 8

Place a line through Bias Voltage name if enable/disable switch works

Vru 0	Vru 1	Vru 2	Vru 3	Vru 4	Vru 5
Vrl 0	Vrl 1	Vrl 2	Vrl 3	Vrl 4	Vrl 5
Vog 0	Vog 1	Vog 2	Vog 3	Vog 4	Vog 5
Vdd 0	Vdd 1	Vdd 2	Vdd 3	Vdd 4	Vdd 5

Stage 9. Vsub and Heater Control testing - Table 9

DAC Value	Vsub Measured Voltage Test Data 10%	50%	90%
Signal	volts	volts	volts
Vsub - rate	-1.25	3.78	8.81
Vsub - Limit	-1.25	3.78	8.81
Vsub0	0.00	0.00	0.00
	Vsub Enable Bit - pass		

DAC Value	Telemetery Readback Test Data 10%	50%	90%
Signal	dec	dec	dec
Vbias 0	154	271	455
Vbias 1	-28	698	1423
RTD1	218	NA	NA
RTD2	249	NA	NA
RTD3	276	NA	NA
RTD4	303	NA	NA
RTD5	325	NA	NA
RTD6	350	NA	NA
Reference 4096	836	NA	NA
eference buffere	836	NA	NA

Stage 10. Video Offset DAC Tests - Table 10.

	DAC Value 410				DAC Value 2048				DAC Value 3686			
ADC	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU
0	0.250	NA	NA	16967	1.250		NA	81013	2.250	NA	500ms	145057
1	0.250	NA	NA	17035	1.250		NA	81013	2.250	NA	500ms	145007
2	0.250	NA	NA	17279	1.250		NA	81227	2.250	NA	500ms	145173
3	0.250	NA	NA	16971	1.250		NA	81024	2.250	NA	500ms	145078
4	0.250	NA	NA	17072	1.250		NA	81113	2.250	NA	500ms	145151
5	0.250	NA	NA	17109	1.250		NA	81102	2.250	NA	500ms	145086
6	0.250	NA	NA	17078	1.250		NA	81012	2.250	NA	500ms	144952
7	0.250	NA	NA	17026	1.250		NA	81065	2.250	NA	500ms	145107
8	0.250	NA	NA	16995	1.250		NA	81066	2.250	NA	500ms	145130
9	0.250	NA	NA	17078	1.250		NA	81146	2.250	NA	500ms	145214
10	0.250	NA	NA	17044	1.250		NA	81022	2.250	NA	500ms	144998
11	0.250	NA	NA	17025	1.250		NA	81083	2.250	NA	500ms	145136

ADC	DC Volts		Data Set		
Channel	Slope	Offset	410	2048	3686
0	1638.000	0.500	0.250	1.250	2.250
1	1638.000	0.500	0.250	1.250	2.250
2	1638.000	0.500	0.250	1.250	2.250
3	1638.000	0.500	0.250	1.250	2.250
4	1638.000	0.500	0.250	1.250	2.250
5	1638.000	0.500	0.250	1.250	2.250
6	1638.000	0.500	0.250	1.250	2.250
7	1638.000	0.500	0.250	1.250	2.250
8	1638.000	0.500	0.250	1.250	2.250
9	1638.000	0.500	0.250	1.250	2.250
10	1638.000	0.500	0.250	1.250	2.250
11	1638.000	0.500	0.250	1.250	2.250

(dac# -offset)/slope=Voltage

ADC	ADU's		Data Set		
Channel	Slope	Offset	410	2048	3686
0	0.026	-23.95	16967	81013	145057
1	0.026	-26.02	17035	81013	145007
2	0.026	-32.61	17279	81227	145173
3	0.026	-23.98	16971	81024	145078
4	0.026	-26.68	17072	81113	145151
5	0.026	-28.00	17109	81102	145086
6	0.026	-27.50	17078	81012	144952
7	0.026	-25.47	17026	81065	145107
8	0.026	-24.54	16995	81066	145130
9	0.026	-26.63	17078	81146	145214
10	0.026	-26.39	17044	81022	144998
11	0.026	-25.38	17025	81083	145136

(dac# -offset)/slope=ADU

Notes and Observations

Checked for oscillations using a Agilent Oscilloscope on AC. OK

Stage 11. CDS Control Functions and Video Channel Performanc

TEST #1: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit is held static. The purpose of this test is to verify the correct operation of the ADC devices and measure the noise of the Offset voltage generators, ADC buffer amplifiers and ADC devices

Noise Test 1

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	81007	8.10E+04	81015.3	2.287
CH 1	81012	8.10E+04	81020	2.35475
CH 2	81218	8.12E+04	81226.9	2.35938
CH 3	81017	8.10E+04	81026	2.26208
CH 4	81104	8.11E+04	81111.2	2.30225
CH 5	81088	8.11E+04	81097.5	2.3451
CH 6	81005	8.10E+04	81013.3	2.35199
CH 7	81061	8.11E+04	81069.4	2.44333
CH 8	81053	8.11E+04	81062.6	2.30523
CH 9	81139	81155	81146.7	2.31223
CH 10	81013	81028	81020.2	2.33413
CH 11	81073	81091	81082	2.35593

TEST #2: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the invert/non-invert and the DC Restore switches are held static.

Noise Test 2

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76640	7.67E+04	76649.5	2.832
CH 1	76798	7.68E+04	76810.8	2.90578
CH 2	76890	7.69E+04	76900.4	2.65955
CH 3	76959	7.70E+04	76969.5	2.86957
CH 4	76485	7.65E+04	76493.9	2.82729
CH 5	76915	7.69E+04	76926.9	2.9116
CH 6	76955	7.70E+04	76964.6	2.81865
CH 7	77039	7.71E+04	77049.6	2.8599
CH 8	76903	7.69E+04	76914.6	2.61665
CH 9	77307	77326	77316.7	2.77984
CH 10	76336	76356	76345.7	2.85649
CH 11	76918	76939	76927.7	2.9222

TEST #3: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the DC Restore switch is held static.

Noise Test 3

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76639	7.67E+04	76650.4	3.0467
CH 1	76805	7.68E+04	76816.1	3.0183
CH 2	76894	7.69E+04	76909.1	3.06496
CH 3	76954	7.70E+04	76968.8	3.18044
CH 4	76488	7.65E+04	76498.6	3.03338
CH 5	76913	7.69E+04	76924.2	3.08022
CH 6	76959	7.70E+04	76969.9	3.0834
CH 7	77047	7.71E+04	77057	3.10687
CH 8	76898	7.69E+04	76907.6	2.96699
CH 9	77306	77328	77316.2	3.02303
CH 10	76330	76354	76340.4	2.94436
CH 11	76910	76933	76920.6	2.97187

TEST #4: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition.

Noise Test 4

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76627	7.67E+04	76639.3	3.06778
CH 1	76806	7.68E+04	76817	3.13112
CH 2	76900	7.69E+04	76911.8	3.17511
CH 3	76956	7.70E+04	76967.8	3.19966
CH 4	76525	7.65E+04	76535.3	3.17652
CH 5	76899	7.69E+04	76910.5	3.16325
CH 6	76965	7.70E+04	76976	3.15386
CH 7	77014	7.70E+04	77025.5	3.21904
CH 8	76938	7.70E+04	76949.9	3.13978
CH 9	77224	77250	77236.8	3.341
CH 10	76348	76369	76358.4	3.15624
CH 11	76866	76894	76880.4	3.0927

TEST #5: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the circuitry set to high GAIN.

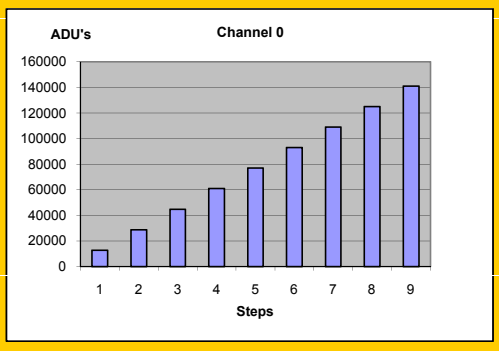
Noise Test 5

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76638	7.67E+04	76648.9	3.58065
CH 1	76819	7.68E+04	76832.4	3.6609
CH 2	76916	7.69E+04	76928.7	3.7516
CH 3	76961	7.70E+04	76975.5	3.65498
CH 4	76527	7.66E+04	76541.6	3.68834
CH 5	76897	7.69E+04	76910.5	3.73316
CH 6	76967	7.70E+04	76980.4	3.74654
CH 7	77015	7.70E+04	77029.1	3.6671
CH 8	76989	7.70E+04	77005.1	3.61114
CH 9	77222	77251	77238.4	3.92554
CH 10	76410	76436	76423.7	3.68042
CH 11	76867	76894	76882.5	3.64813

TEST #6A: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

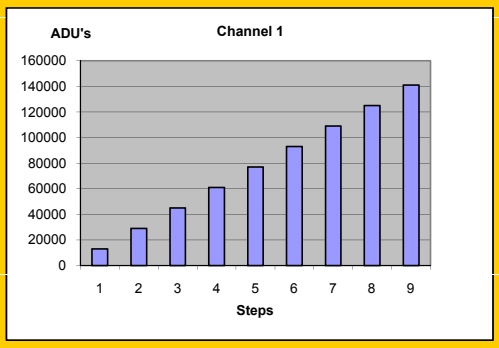
BrdTst6_006 / Channel 0					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12874	12898	12885.3	2.97517	10%
0x333	28866	28889	28878	3.19551	20%
0x4cc	44856	44879	44866.9	3.06268	30%
0x666	60885	60910	60898.5	2.98273	40%
0x800	76913	76937	76926.4	3.12023	50%
0x999	92908	92933	92920.5	3.15248	60%
0xb33	108940	108966	108952	3.19397	70%
0xccc	124930	124954	124943	3.36817	80%
0xe66	140965	140988	140977	3.1039	90%



TEST #6B: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

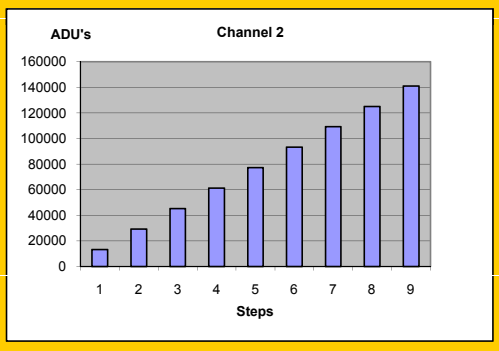
BrdTst6_006 / Channel 1					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13059	13080	13069.7	3.18848	10%
0x333	29035	29059	29046.3	3.20976	20%
0x4cc	45008	45030	45018.5	3.17056	30%
0x666	61021	61045	61033.2	3.17495	40%
0x800	77034	77057	77046.8	3.1782	50%
0x999	93011	93034	93022.5	3.11539	60%
0xb33	109026	109049	109038	3.23496	70%
0xccc	124998	125023	125010	3.23376	80%
0xe66	141018	141040	141029	3.06461	90%



TEST #6C: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

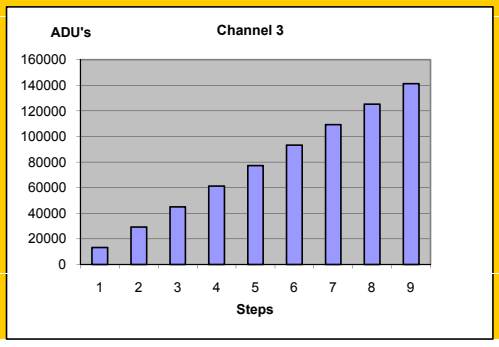
BrdTst6_006 / Channel 2					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13229	13255	13242.9	3.11864	10%
0x333	29197	29221	29209.2	3.18173	20%
0x4cc	45165	45186	45175.1	3.01048	30%
0x666	61168	61194	61180.3	3.20571	40%
0x800	77173	77194	77183.4	3.0764	50%
0x999	93140	93163	93152.4	3.16892	60%
0xb33	109148	109172	109158	3.11724	70%
0xccc	125111	125137	125124	3.2974	80%
0xe66	141118	141144	141133	3.14375	90%



TEST #6D: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

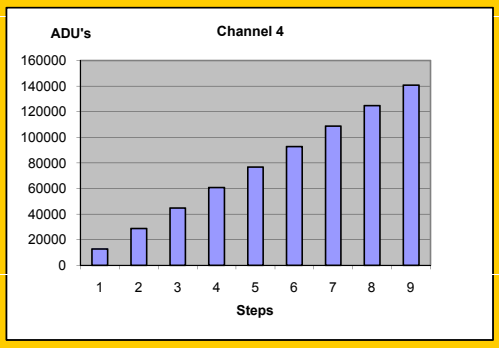
BrdTst6_006 / Channel 3					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13135	13158	13146.7	3.24189	10%
0x333	29128	29153	29140.2	3.23376	20%
0x4cc	45117	45142	45130.1	3.22954	30%
0x666	61150	61174	61161.6	3.25051	40%
0x800	77184	77205	77195.1	3.17743	50%
0x999	93176	93200	93186.9	3.08173	60%
0xb33	109206	109232	109219	3.0804	70%
0xccc	125197	125223	125211	3.37731	80%
0xe66	141235	141256	141246	3.23562	90%



TEST #6E: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

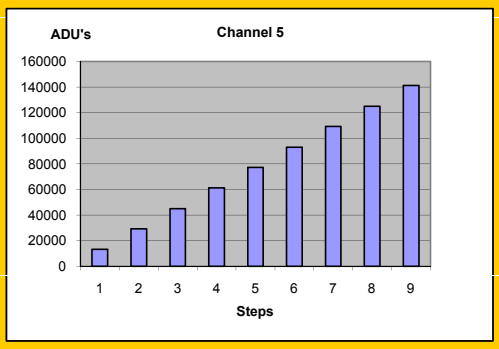
BrdTst6_006 / Channel 4					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12768	12790	12778.6	3.06896	10%
0x333	28754	28781	28768.3	3.17478	20%
0x4cc	44746	44768	44756.9	3.21981	30%
0x666	60774	60796	60784.6	3.06826	40%
0x800	76802	76827	76813.3	3.14274	50%
0x999	92793	92818	92804.7	3.19004	60%
0xb33	108824	108845	108834	2.96109	70%
0xccc	124810	124835	124824	3.41539	80%
0xe66	140844	140866	140855	3.21803	90%



TEST #6F: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

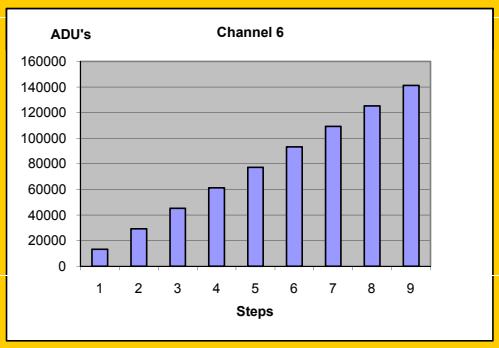
BrdTst6_006 / Channel 5					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13162	13185	13172.8	3.05286	10%
0x333	29140	29165	29150.4	3.1889	20%
0x4cc	45113	45135	45123.5	3.20867	30%
0x666	61128	61152	61138.9	3.26122	40%
0x800	77138	77164	77150.5	3.21434	50%
0x999	93118	93140	93128	3.1304	60%
0xb33	109134	109157	109145	3.27595	70%
0xccc	125104	125129	125119	3.33214	80%
0xe66	141127	141151	141138	3.08366	90%



TEST #6G: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

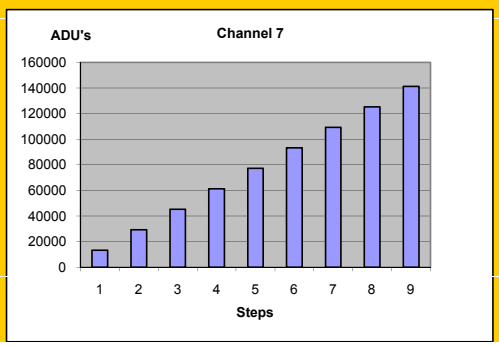
BrdTst6_006 / Channel 6					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13268	13290	13278.6	3.16069	10%
0x333	29231	29253	29242.5	3.1781	20%
0x4cc	45194	45219	45206.2	3.16247	30%
0x666	61196	61220	61208.3	3.26482	40%
0x800	77199	77221	77210.4	3.12814	50%
0x999	93164	93189	93176.8	3.19864	60%
0xb33	109166	109191	109178	3.22993	70%
0xccc	125129	125155	125143	3.49165	80%
0xe66	141136	141160	141148	3.19381	90%



TEST #6H: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

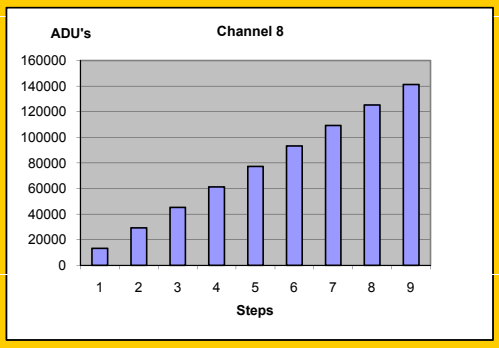
BrdTst6_006 / Channel 7					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13189	13211	13201.2	3.0842	10%
0x333	29181	29204	29192.8	3.1599	20%
0x4cc	45169	45194	45181.8	3.19209	30%
0x666	61200	61223	61211.1	3.23468	40%
0x800	77222	77248	77234.5	3.2078	50%
0x999	93215	93240	93226.5	3.23905	60%
0xb33	109245	109268	109257	3.2177	70%
0xccc	125235	125259	125246	3.35398	80%
0xe66	141268	141293	141280	3.2731	90%



TEST #6I: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

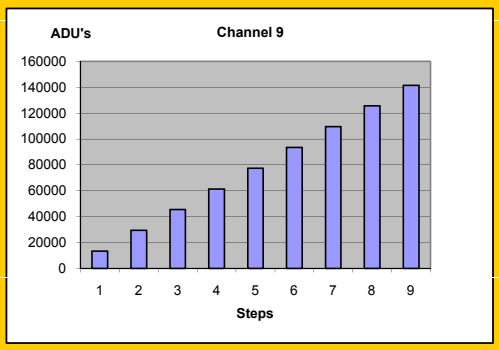
BrdTst6_006 / Channel 8					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13140	13160	13150.2	3.08188	10%
0x333	29133	29156	29145.8	3.07099	20%
0x4cc	45129	45151	45140.2	3.06551	30%
0x666	61163	61185	61174.4	3.17431	40%
0x800	77200	77222	77211	3.145	50%
0x999	93197	93221	93209.6	3.09845	60%
0xb33	109235	109257	109245	3.10891	70%
0xccc	125227	125254	125241	3.27542	80%
0xe66	141268	141290	141279	3.12267	90%



TEST #6J: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

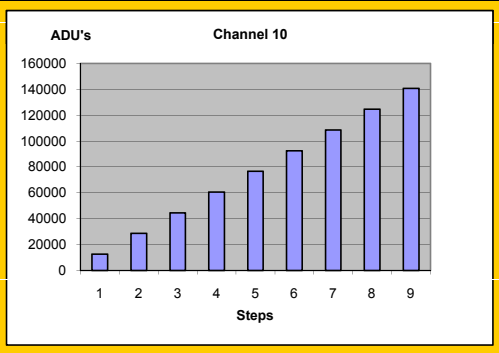
BrdTst6_006 / Channel 9					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13423	13445	13433.8	3.2609	10%
0x333	29422	29446	29433.9	3.25772	20%
0x4cc	45418	45441	45428.1	3.1313	30%
0x666	61450	61477	61464	3.38248	40%
0x800	77480	77505	77493.7	3.32854	50%
0x999	93483	93506	93493.9	3.28804	60%
0xb33	109518	109543	109531	3.38841	70%
0xccc	125512	125538	125526	3.44458	80%
0xe66	141554	141578	141567	3.26418	90%



TEST #6K: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

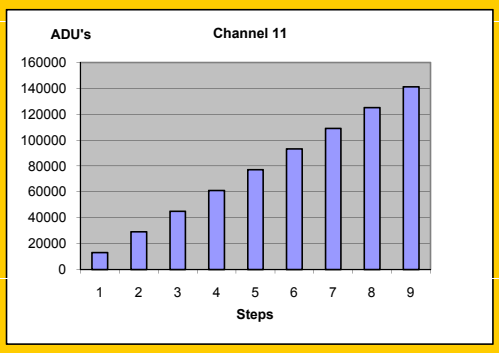
BrdTst6_006 / Channel 10					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12634	12657	12645.7	3.1526	10%
0x333	28610	28633	28621.8	3.08592	20%
0x4cc	44583	44606	44594.2	3.09231	30%
0x666	60598	60621	60609	3.18514	40%
0x800	76610	76633	76621.6	3.11358	50%
0x999	92587	92610	92597.9	3.20909	60%
0xb33	108601	108625	108613	3.19955	70%
0xccc	124576	124600	124587	3.3421	80%
0xe66	140592	140616	140605	3.1918	90%



TEST #6L: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

BrdTst6_006 / Channel 11					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13069	13094	13081.7	3.26231	10%
0x333	29064	29088	29076.7	3.04424	20%
0x4cc	45057	45084	45070.4	3.21759	30%
0x666	61093	61116	61102.9	3.19455	40%
0x800	77118	77141	77129.6	3.13459	50%
0x999	93113	93137	93125.3	3.1827	60%
0xb33	109147	109168	109158	3.07493	70%
0xccc	125138	125164	125151	3.47783	80%
0xe66	141174	141200	141188	3.20743	90%



Stage 13. Other Bit Tests. Table 11

Electronic Serial Number	0xDB6FB0		Board Serial Number	11
Firmware Version	0x193		Name Of Person Testing	S. Holm
Ident Register	0x502		Board passed Functional Tests	YES