DES 12 Channel Board - Functional Tests: CCD Acquisition Board Revision 1.0

Stage 1. Preparation of documentation and configuration settings - Table 1.

Board Part Number	27		Board Serial Number	0xDB6FA0
Date Of Tests	May 2010		Name Of Person Testing	S. Holm
Suggested Filename To Save	CCDACQ_12Ch_REPORT_BOARD27.xl		Sequence number: Test	

Stage 3. Power plane short test - Table 2.

Supply Name	Short test to ground: Impedance to ground	Test Point	
+1.2VD	41.60	TP43	~50 ohms
+1.8VD	350k	TPB12	> 1K ohm
+2.5VD	15k	TPB11	> 1K ohm
+3.3VD	5k	D13	> 1K ohm
+5VD	82k	D14	> 1K ohm
+5VA	1.8M	C267	> 1K ohm
-5VA	500k	C270	> 1K ohm
+15VA	2M	C288	> 1K ohm
-15VA	1.9M	C282	> 1K ohm
-28VA	1.7M	C307	> 1K ohm

Stage 4. Firmware programming tests - Table 3.

JTAG Order	Designator	Device	Load File	Check Sum or User Code
1	U122	XCF08PFS48C PROM	CcdAcqFpgaV41.mcs	0014ef670
2	U114	Spartan3 XC3S2000 FPGA	ccdacqfpgav41.bit	5102801

Stage 5. Power Consumption - Table 4.

Supply Name	Power Supply Consumption: Measured Voltage at test point	Measured Current on power supply	Test Point	
+1.2VD	1.21	N/A	TP43	
+1.8VD	1.80	N/A	TPB12	
+2.5VD	2.51	N/A	TPB11	
+3.3VD	3.27	0.102	D13	
+5VD	5.20	0.15	D14	
+5VA	4.74	0.569	C267	
-5VA	-4.97	0.437	C270	
+15VA	14.97	0.558	C288	
-15VA	-15.07	0.411	C282	
-28VA	-27.81	0.197	C307	
Vref 0+	10.05	N/A	R534	Vsub+ Reference(+10v)
Vref 0-	-2.51	N/A	R525	Vsub - Reference(-2.5v)
Vref Offset	2.50	N/A	R573	ADC Offset Reference(+2.5v)
Vclamp	1.88	N/A	VIA	ADC Clamp Voltage(+1.8v)
ADC Ref.	2.50	N/A	VIA	ADC Reference Voltage(+2.5v)
Vref 1+	2.50	N/A	R537	Vru and Vrl + Reference(+2.5v)
Vref 1-	-10.09	N/A	R535	Vru and Vrl - Reference(-10v)
Vref 2+	5.00	N/A	R563	Vog + Reference(+5v)
Vref 2-	-2.51	N/A	R555	Vog - Reference(-2.5v)
Vref 3+	2.50	N/A	R543	Vdd + Reference(+2.5v)
Vref 3-	-10.10	N/A	R571	Vdd - Reference(-10v)

Power Dissipation:
26.0 Watts

~27 watts +/- 5%

Stage 7. Basic Bus Transactions - **D**igital **Register** Tests - Table 5.

Register name	Put an X on any bit that has an error: 31-24	23-16	15-08	07-00	Function	Test name: Pattern	Walking 0's	Walking 1's
CDS Control			00000000	00000000	16 bit R/W			
Digital Output	00000000	00000000	00000000	00000000	32 bit R/W			
ADC Config.			0000	00000000	12 bit R/W			
Offset DAC			0000	00000000	12 bit R/W			
Bias DAC			0000	00000000	12 bit R/W			
Telemetry Config.				0000	4 bit R/W			
Auxilary Config.			00	00000000	10 bit R/W			
Redirect				0000	4 bit R/W			
Pixel Transfer				00000000	8 bit R/W			
Micro SEQ			00000000	00000000	16 bit R/W			
RAM Buffer			00000000	00000000	16 bit R/W			
LED Control				0000	4 bit R/W			
Control			00000000	00000000	16 bit R/W			
All Register Test	00000000	00000000	00000000	00000000	16 bit R/W	**Passed**	**Passed**	**Passed**

Stage 8. Bias Voltage settings and output enables testing - Table 8

DAC Value	410	Bias Voltage Test Data 2048	3686	50% rms Noise	10-90% Rise Time			
Signal	volts	volts	volts	uV	millisec.	Fanout Brd	Slope	Offset
Vru 0	-13.26	-5.70	1.86	<10	1	BIAS 3	216.67	3283.00
Vru 1	-13.26	-5.70	1.86	<10	1	BIAS 4	216.67	3283.00
Vru 2	-13.26	-5.70	1.86	<10	1	BIAS 5	216.67	3283.00
Vru 3	-13.26	-5.70	1.86	<10	1	BIAS 6	216.67	3283.00
Vru 4	-13.26	-5.70	1.86	<10	1	BIAS 7	216.67	3283.00
Vru 5	-13.26	-5.70	1.86	<10	1	BIAS 8	216.67	3283.00
Vru 6	-13.26	-5.70	1.86	NA	NA	BIAS 9	216.67	3283.00
Vru 7	-13.26	-5.70	1.86	NA	NA	BIAS 10	216.67	3283.00
Vrl 0	-13.26	-5.70	1.86	<10	1	BIAS 11	216.67	3283.00
Vrl 1	-13.26	-5.70	1.86	<10	1	BIAS 12	216.67	3283.00
Vrl 2	-13.26	-5.70	1.86	<10	1	BIAS 13	216.67	3283.00
Vrl 3	-13.26	-5.70	1.86	<10	1	BIAS 14	216.67	3283.00
Vrl 4	-13.26	-5.70	1.86	<10	1	BIAS 15	216.67	3283.00
Vrl 5	-13.26	-5.70	1.86	<10	1	BIAS 16	216.67	3283.00
Vrl 6	-13.26	-5.70	1.86	NA	NA	BIAS 17	216.67	3283.00
Vrl 7	-13.26	-5.70	1.86	NA	NA	BIAS 18	216.67	3283.00
Vog 0	-1.76	1.24	4.25	<10	1	BIAS 19	545.09	1370.27
Vog 1	-1.76	1.24	4.25	<10	1	BIAS 20	545.09	1370.27
Vog 2	-1.76	1.24	4.25	<10	1	BIAS 21	545.09	1370.27
Vog 3	-1.76	1.24	4.25	<10	1	BIAS 22	545.09	1370.27
Vog 4	-1.76	1.24	4.25	<10	1	BIAS 23	545.09	1370.27
Vog 5	-1.76	1.24	4.25	<10	1	BIAS 24	545.09	1370.27
Vog 6	-1.76	1.24	4.25	NA	NA	BIAS 25	545.09	1370.27
Vog 7	-1.76	1.24	4.25	NA	NA	BIAS 26	545.09	1370.27
Vdd 0	-22.15	-9.53	3.10	<10	20	BIAS 27	129.74	3284.01
Vdd 1	-22.15	-9.53	3.10	<10	20	BIAS 28	129.74	3284.01
Vdd 2	-22.17	-9.54	3.10	<10	20	BIAS 29	129.64	3284.33
Vdd 3	-22.12	-9.51	3.10	<10	20	BIAS 30	129.90	3283.32
Vdd 4	-22.21	-9.55	3.11	<10	20	BIAS 21	129.38	3283.62
Vdd 5	-22.11	-9.51	3.09	<10	20	BIAS 32	130.00	3284.30
Vdd 6	-22.14	-9.53	3.09	NA	NA	BIAS 33	129.85	3284.99
Vdd 7	-22.21	-9.55	3.11	NA	NA	BIAS 34	129.38	3283.62

Vru	Slope		Offset
Mean	216.67	Mean	3283.00
Stdev	0	Stdev	0
Average	216.66667	Average	3283
	Dac #	Average voltage	
	0	-15.0	
	4095	3.8	

Vrl	Slope		Offset
Mean	216.67	Mean	3283.00
Stdev	0	Stdev	0
Average	216.66667	Average	3283
	Dac #	Average voltage	
	0	-15.2	
	4095	3.8	

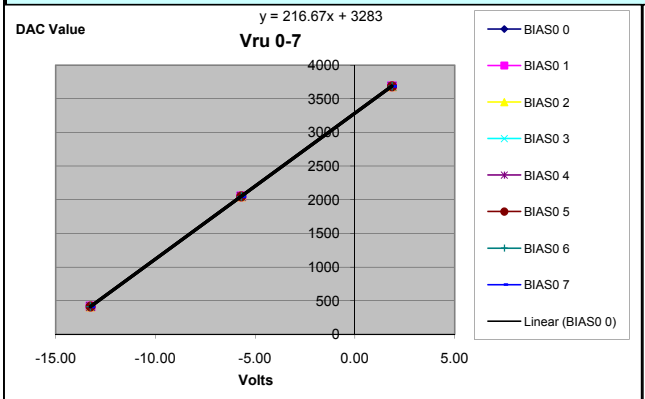
Vog	Slope		Offset
Mean	545.09	Mean	1370.27
Stdev	1.137E-13	Stdev	2.27374E-13
Average	545.09101	Average	1370.270176
	Dac #	Average voltage	
	0	-2.5	
	4095	5.0	

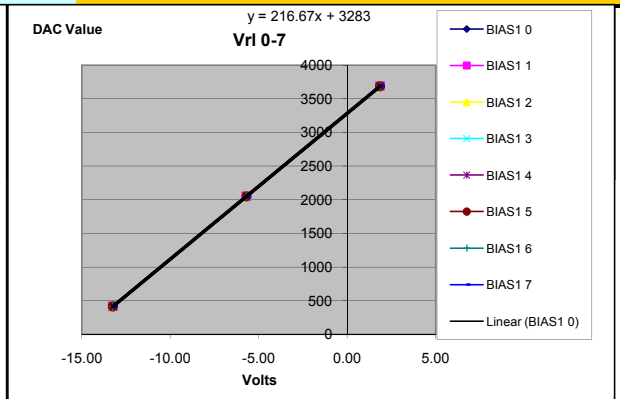
Vdd	Slope		Offset
Mean	129.70	Mean	3284.03
Stdev	0.2112042	Stdev	0.492600052
Average	129.70439	Average	3284.025817
	Dac #	Average voltage	
	0	-25.3	
	4095	6.3	

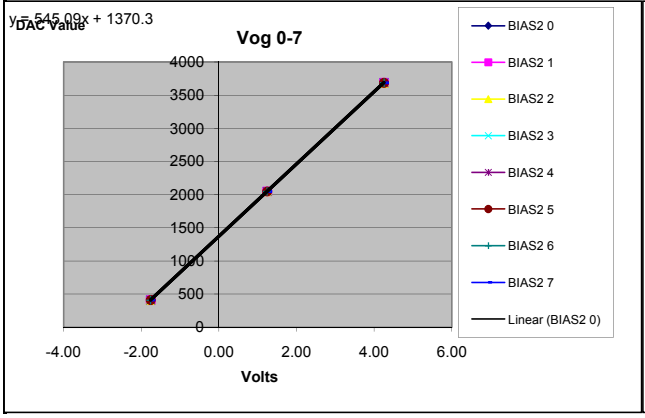
Notes and Observations

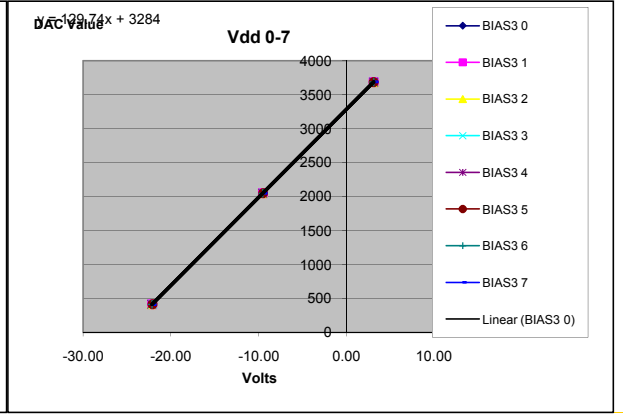
Checked for oscillations using a Agilent Oscilloscpe on AC.**OK**

average min & max voltages
(dac# -offset)/slope=voltage









Stage 8B. Telemetry System Tests - Table 7 (Bias Telemetry Tests)

DAC Value	410	3686	Bias Signals Set Volts		Resolved Values for Telemetry Channel	
	Telemetry Return Values					
Signal	10%	90%	10%	90%	Slope	Offset
Vru 0	-1764	421	-13.26	1.86	144.5106	152.21
Vru 1	-1766	421	-13.26	1.86	144.6429	151.96
Vru 2	-1764	421	-13.26	1.86	144.5106	152.21
Vru 3	-1763	421	-13.26	1.86	144.4444	152.33
Vru 4	-1763	421	-13.26	1.86	144.4444	152.33
Vru 5	-1764	421	-13.26	1.86	144.5106	152.21
Vru 6	-1767	421	-13.26	1.86	144.7090	151.84
Vru 7	-1765	420	-13.26	1.86	144.5106	151.21
Vrl 0	-1762	421	-13.26	1.86	144.3783	152.46
Vrl 1	-1764	421	-13.26	1.86	144.5106	152.21
Vrl 2	-1761	422	-13.26	1.86	144.3783	153.46
Vrl 3	-1761	421	-13.26	1.86	144.3122	152.58
Vrl 4	-1761	421	-13.26	1.86	144.3122	152.58
Vrl 5	-1761	421	-13.26	1.86	144.3122	152.58
Vrl 6	-1761	421	-13.26	1.86	144.3122	152.58
Vrl 7	-1761	421	-13.26	1.86	144.3122	152.58
Vog 0	-363	867	-1.76	4.25	204.6589	-2.80
Vog 1	-363	867	-1.76	4.25	204.6589	-2.80
Vog 2	-363	867	-1.76	4.25	204.6589	-2.80
Vog 3	-363	867	-1.76	4.25	204.6589	-2.80
Vog 4	-363	867	-1.76	4.25	204.6589	-2.80
Vog 5	-363	867	-1.76	4.25	204.6589	-2.80
Vog 6	-363	867	-1.76	4.25	204.6589	-2.80
Vog 7	-363	867	-1.76	4.25	204.6589	-2.80
Vdd 0	-1759	573	-22.15	3.10	92.3564	286.70
Vdd 1	-1761	573	-22.15	3.10	92.4356	286.45
Vdd 2	-1760	573	-22.17	3.10	92.3229	286.80
Vdd 3	-1755	572	-22.12	3.10	92.2680	285.97
Vdd 4	-1760	573	-22.21	3.11	92.1406	286.44
Vdd 5	-1752	572	-22.11	3.09	92.2222	287.03
Vdd 6	-1754	572	-22.14	3.09	92.1918	287.13
Vdd 7	-1763	574	-22.21	3.11	92.2986	286.95

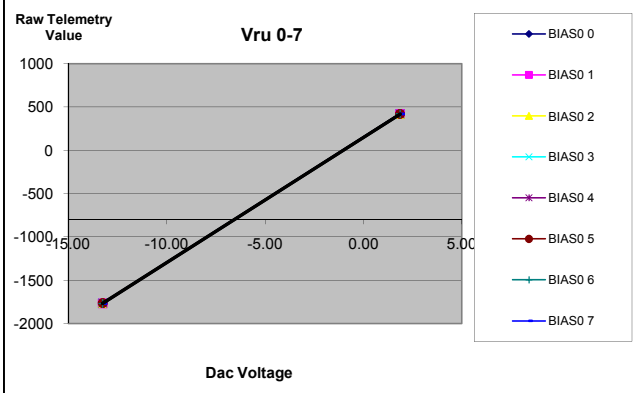
AVERAGE

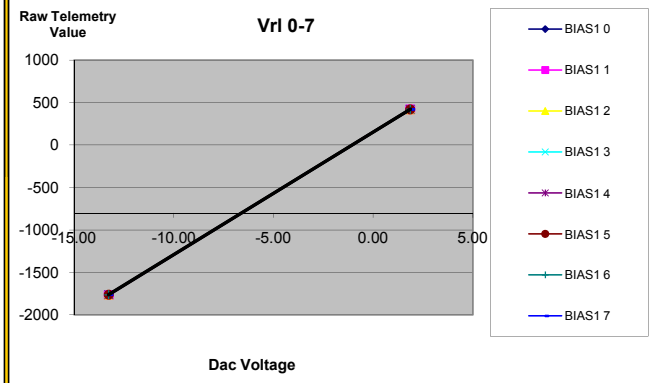
Vru	Slope		Offset
Mean	144.54	Mean	152.04
Stdev	0.0871003	Stdev	0.3522618

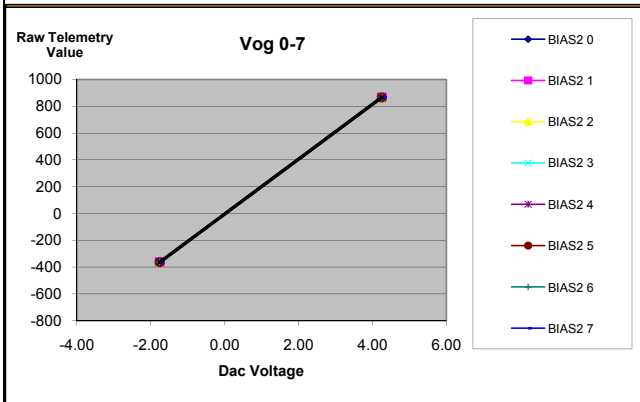
Vrl	Slope		Offset
Mean	144.35	Mean	152.63
Stdev	0.0656188	Stdev	0.3357659

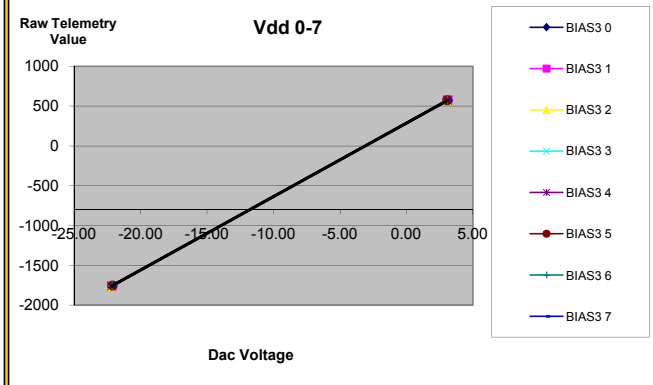
Vog	Slope		Offset
Mean	204.66	Mean	-2.80
Stdev	0	Stdev	0

Vdd	Slope		Offset
Mean	92.28	Mean	286.68
Stdev	0.0886981	Stdev	0.3584093









Stage 8C. Bias Voltage output enables testing - Table 8

Place a line through Bias Voltage name if enable/disable switch works

Vru 0	Vru 1	Vru 2	Vru 3	Vru 4	Vru 5
Vrl 0	Vrl 1	Vrl 2	Vrl 3	Vrl 4	Vrl 5
Vog 0	Vog 1	Vog 2	Vog 3	Vog 4	Vog 5
Vdd 0	Vdd 1	Vdd 2	Vdd 3	Vdd 4	Vdd 5

Stage 9. Vsub and Heater Control testing - Table 9

DAC Value	Vsub Measured Voltage Test Data 10%	50%	90%
Signal	volts	volts	volts
Vsub - rate	-1.25	3.76	8.79
Vsub - Limit	-1.25	3.76	8.79
Vsub0	0.00	0.00	0.00
	Vsub Enable Bit - pass		

DAC Value	Telemetery Readback Test Data 10%	50%	90%
Signal	dec	dec	dec
Vbias 0	154	272	451
Vbias 1	-28	696	1420
RTD1	219	NA	NA
RTD2	249	NA	NA
RTD3	274	NA	NA
RTD4	301	NA	NA
RTD5	326	NA	NA
RTD6	351	NA	NA
Reference 4096	836	NA	NA
eference buffere	836	NA	NA

Stage 10. Video Offset DAC Tests - Table 10.

	DAC Value 410				DAC Value 2048				DAC Value 3686			
ADC	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU
0	0.250	NA	NA	17016	1.250		NA	81026	2.250	NA	500ms	145027
1	0.250	NA	NA	17159	1.250		NA	81106	2.250	NA	500ms	145063
2	0.250	NA	NA	17039	1.250		NA	81104	2.250	NA	500ms	145171
3	0.250	NA	NA	17039	1.250		NA	81059	2.250	NA	500ms	145074
4	0.250	NA	NA	17026	1.250		NA	81076	2.250	NA	500ms	145137
5	0.250	NA	NA	16903	1.250		NA	81038	2.250	NA	500ms	145181
6	0.250	NA	NA	16930	1.250		NA	81029	2.250	NA	500ms	145126
7	0.250	NA	NA	16994	1.250		NA	81088	2.250	NA	500ms	145177
8	0.250	NA	NA	16958	1.250		NA	81115	2.250	NA	500ms	145271
9	0.250	NA	NA	16974	1.250		NA	81036	2.250	NA	500ms	145099
10	0.250	NA	NA	17196	1.250		NA	81199	2.250	NA	500ms	145196
11	0.250	NA	NA	17105	1.250		NA	81162	2.250	NA	500ms	145219

ADC	DC Volts		Data Set		
Channel	Slope	Offset	410	2048	3686
0	1638.000	0.500	0.250	1.250	2.250
1	1638.000	0.500	0.250	1.250	2.250
2	1638.000	0.500	0.250	1.250	2.250
3	1638.000	0.500	0.250	1.250	2.250
4	1638.000	0.500	0.250	1.250	2.250
5	1638.000	0.500	0.250	1.250	2.250
6	1638.000	0.500	0.250	1.250	2.250
7	1638.000	0.500	0.250	1.250	2.250
8	1638.000	0.500	0.250	1.250	2.250
9	1638.000	0.500	0.250	1.250	2.250
10	1638.000	0.500	0.250	1.250	2.250
11	1638.000	0.500	0.250	1.250	2.250

(dac# -offset)/slope=Voltage

ADC	ADU's		Data Set		
Channel	Slope	Offset	410	2048	3686
0	0.026	-25.50	17016	81026	145027
1	0.026	-29.45	17159	81106	145063
2	0.026	-25.63	17039	81104	145171
3	0.026	-25.99	17039	81059	145074
4	0.026	-25.33	17026	81076	145137
5	0.026	-21.64	16903	81038	145181
6	0.026	-22.65	16930	81029	145126
7	0.026	-24.34	16994	81088	145177
8	0.026	-22.96	16958	81115	145271
9	0.026	-24.00	16974	81036	145099
10	0.026	-30.14	17196	81199	145196
11	0.026	-27.39	17105	81162	145219

(dac# -offset)/slope=ADU

Notes and Observations

Checked for oscillations using a Agilent Oscilloscope on AC. OK

Stage 11. CDS Control Functions and Video Channel Performanc

TEST #1: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit is held static. The purpose of this test is to verify the correct operation of the ADC devices and measure the noise of the Offset voltage generators, ADC buffer amplifiers and ADC devices

Noise Test 1

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	81018	81035	81027.3	2.18552
CH 1	81101	81118	81110.3	2.39002
CH 2	81097	81114	81105.6	2.40449
CH 3	81052	81070	81061	2.48027
CH 4	81074	81089	81081.7	2.28051
CH 5	81033	81049	81040.1	2.31463
CH 6	81020	81037	81028.6	2.32864
CH 7	81080	81099	81089	2.36894
CH 8	81108	81125	81116.5	2.27333
CH 9	81029	81047	81036.7	2.39251
CH 10	81186	81205	81196.2	2.33841
CH 11	81155	81173	81165	2.455

TEST #2: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the invert/non-invert and the DC Restore switches are held static.

Noise Test 2

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76442	76460	76451.2	2.69246
CH 1	76805	76824	76814.6	2.85049
CH 2	76720	76740	76729.7	2.94683
CH 3	76913	76936	76925.4	2.90181
CH 4	76653	76673	76663	2.71679
CH 5	76884	76906	76895.5	2.81754
CH 6	76896	76916	76906.1	2.83881
CH 7	77021	77040	77030.5	2.8087
CH 8	76617	76639	76627.8	2.63065
CH 9	76764	76785	76775.7	2.83932
CH 10	76860	76884	76871.1	2.87753
CH 11	77120	77140	77130	2.87569

TEST #3: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the DC Restore switch is held static.

Noise Test 3

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76439	76463	76452	2.93265
CH 1	76790	76814	76802.1	3.12551
CH 2	76715	76740	76727.8	3.12568
CH 3	76915	76938	76926.7	3.08473
CH 4	76646	76668	76657.5	2.88372
CH 5	76885	76906	76895	2.99522
CH 6	76882	76905	76893.9	3.04342
CH 7	77029	77052	77039.6	3.10021
CH 8	76612	76634	76623.3	2.92146
CH 9	76760	76782	76772	3.03791
CH 10	76865	76890	76875.5	3.13645
CH 11	77127	77149	77138.1	3.10193

TEST #4: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition.

Noise Test 4

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76432	76454	76443.4	3.12167
CH 1	76795	76818	76806	3.23261
CH 2	76720	76742	76730.9	3.15177
CH 3	76915	76937	76925.6	3.18911
CH 4	76684	76705	76694.2	3.03218
CH 5	76871	76893	76882.1	2.99115
CH 6	76890	76910	76900	3.16297
CH 7	76998	77021	77009.1	3.1758
CH 8	76656	76676	76665.5	3.10976
CH 9	76678	76702	76689	3.05675
CH 10	76882	76905	76894	3.19198
CH 11	77085	77109	77097.3	3.21526

TEST #5: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the circuitry set to high GAIN.

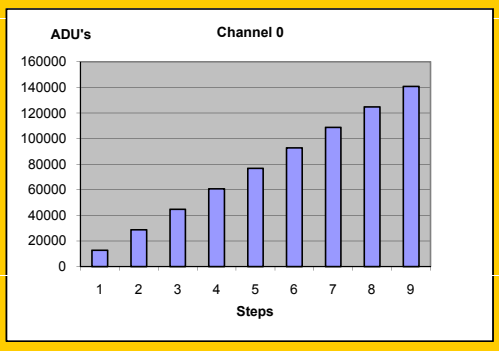
Noise Test 5

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76440	76468	76453.6	3.53808
CH 1	76804	76829	76817.6	3.60675
CH 2	76732	76758	76745.2	3.69473
CH 3	76917	76946	76930.5	3.73471
CH 4	76687	76711	76698.7	3.60715
CH 5	76867	76894	76882.2	3.5328
CH 6	76889	76916	76903.1	3.66657
CH 7	76998	77026	77011.4	3.74763
CH 8	76704	76733	76718.6	3.5367
CH 9	76677	76703	76689.7	3.55946
CH 10	76944	76970	76958	3.73975
CH 11	77085	77111	77098.1	3.67536

TEST #6A: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

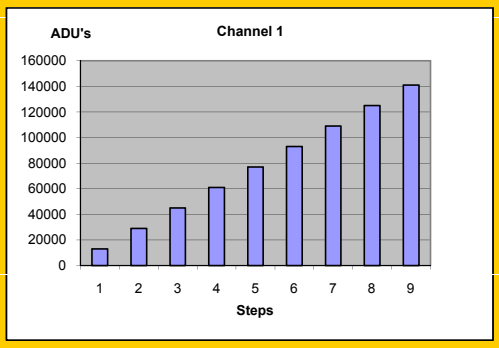
BrdTst6_006 / Channel 0					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12727	12749	12737.3	3.09205	10%
0x333	28709	28732	28721	3.13915	20%
0x4cc	44690	44713	44701.9	3.18721	30%
0x666	60711	60737	60723.7	3.18535	40%
0x800	76727	76750	76738.9	2.92634	50%
0x999	92709	92730	92719.7	3.1563	60%
0xb33	108731	108752	108741	3.08518	70%
0xccc	124713	124736	124724	3.20406	80%
0xe66	140736	140760	140746	3.22504	90%



TEST #6B: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

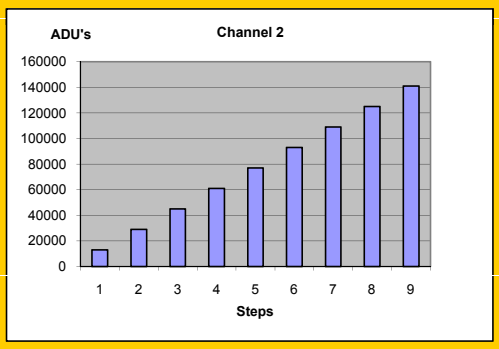
BrdTst6_006 / Channel 1					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13094	13117	13106.5	3.17196	10%
0x333	29062	29086	29076.8	3.196	20%
0x4cc	45030	45053	45041.5	3.10021	30%
0x666	61040	61062	61050.7	3.20381	40%
0x800	77039	77062	77051.6	3.22241	50%
0x999	93009	93032	93019.4	3.1853	60%
0xb33	109015	109038	109027	3.04478	70%
0xccc	124982	125006	124995	3.31162	80%
0xe66	140991	141016	141003	3.28793	90%



TEST #6C: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

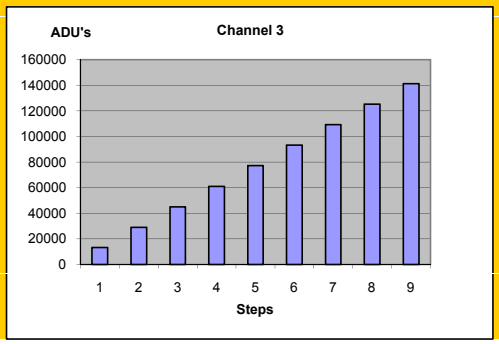
BrdTst6_006 / Channel 2					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12943	12966	12955	3.17764	10%
0x333	28941	28965	28950.8	3.17672	20%
0x4cc	44933	44956	44944.6	3.22341	30%
0x666	60969	60992	60979.7	3.0575	40%
0x800	76997	77020	77009.2	3.20246	50%
0x999	92995	93018	93007.4	3.18422	60%
0xb33	109032	109056	109042	3.1897	70%
0xccc	125027	125049	125037	3.26601	80%
0xe66	141063	141085	141073	3.27669	90%



TEST #6D: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

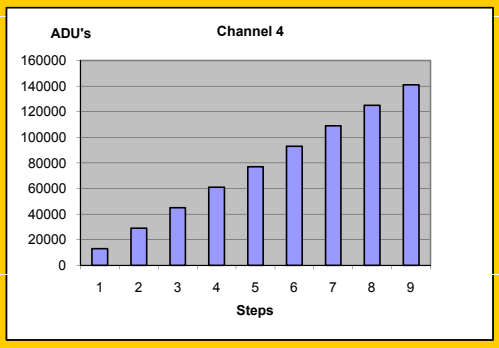
BrdTst6_006 / Channel 3					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13134	13155	13143.8	3.18333	10%
0x333	29118	29142	29129.3	3.19318	20%
0x4cc	45099	45124	45111.9	3.26029	30%
0x666	61124	61146	61136.4	3.10978	40%
0x800	77141	77167	77154.5	3.2331	50%
0x999	93126	93150	93138.4	3.34773	60%
0xb33	109151	109173	109162	3.22766	70%
0xccc	125132	125156	125145	3.24512	80%
0xe66	141156	141181	141170	3.35263	90%



TEST #6E: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

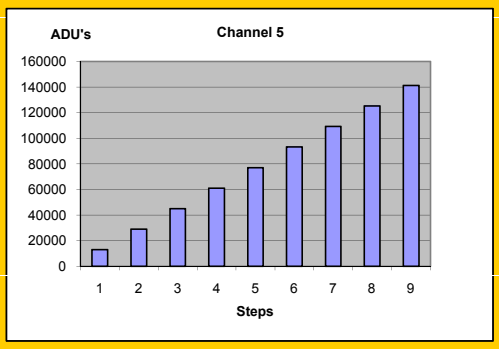
BrdTst6_006 / Channel 4					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12927	12951	12937.4	3.07604	10%
0x333	28918	28942	28930.7	2.99222	20%
0x4cc	44915	44936	44925	3.13428	30%
0x666	60947	60971	60957.9	3.20205	40%
0x800	76978	77000	76989.1	3.08348	50%
0x999	92971	92993	92982.7	3.11386	60%
0xb33	109004	109028	109014	3.00714	70%
0xccc	125000	125022	125011	3.09593	80%
0xe66	141033	141055	141044	3.1835	90%



TEST #6F: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

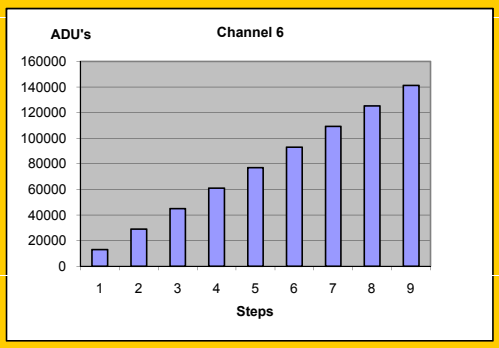
BrdTst6_006 / Channel 5					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12989	13012	13000.9	3.0963	10%
0x333	29003	29028	29016.1	3.15772	20%
0x4cc	45015	45038	45027.4	3.13392	30%
0x666	61069	61093	61081.8	3.16963	40%
0x800	77124	77148	77135.9	3.19089	50%
0x999	93136	93159	93147.6	3.16297	60%
0xb33	109190	109216	109202	3.24222	70%
0xccc	125204	125226	125215	3.14525	80%
0xe66	141256	141280	141269	3.23939	90%



TEST #6G: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

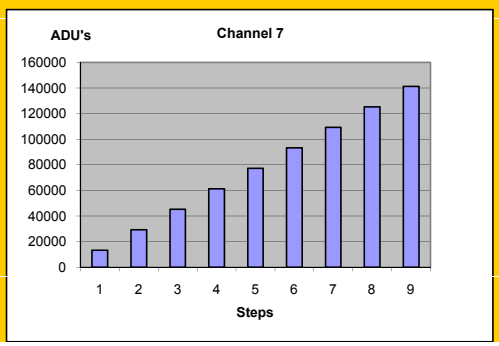
BrdTst6_006 / Channel 6					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13032	13054	13042.8	2.96955	10%
0x333	29033	29056	29043.8	3.02522	20%
0x4cc	45039	45061	45049.6	3.09594	30%
0x666	61077	61103	61091.5	3.11619	40%
0x800	77120	77144	77132.4	3.16704	50%
0x999	93124	93146	93136.2	3.12414	60%
0xb33	109165	109188	109176	3.11841	70%
0xccc	125172	125196	125184	3.09985	80%
0xe66	141212	141235	141224	3.15519	90%



TEST #6H: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

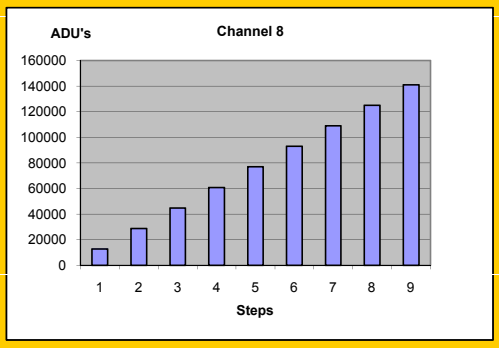
BrdTst6_006 / Channel 7					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13138	13160	13148	3.25061	10%
0x333	29139	29164	29152.5	3.21186	20%
0x4cc	45141	45164	45152.5	3.11721	30%
0x666	61184	61206	61195.9	3.23372	40%
0x800	77221	77246	77234.9	3.1867	50%
0x999	93222	93246	93234.4	3.16609	60%
0xb33	109268	109290	109279	3.17484	70%
0xccc	125268	125291	125280	3.22102	80%
0xe66	141310	141336	141323	3.28997	90%



TEST #6I: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

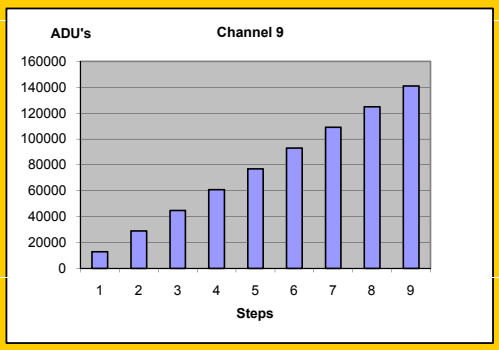
BrdTst6_006 / Channel 8					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12767	12789	12777.3	3.12161	10%
0x333	28786	28810	28798.4	3.1254	20%
0x4cc	44799	44822	44811.8	3.17824	30%
0x666	60858	60883	60871	3.05214	40%
0x800	76916	76940	76928	3.18441	50%
0x999	92936	92957	92947.2	3.1442	60%
0xb33	108995	109018	109005	3.15328	70%
0xccc	125009	125033	125022	3.23859	80%
0xe66	141070	141093	141081	3.23404	90%



TEST #6J: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

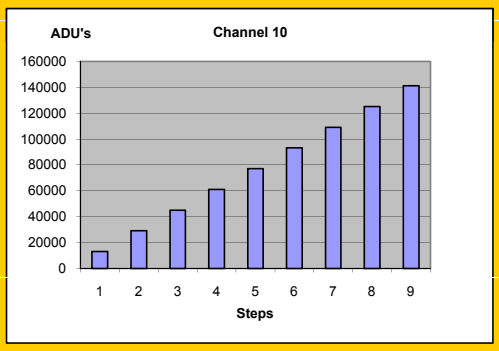
BrdTst6_006 / Channel 9					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12872	12897	12884.5	3.29819	10%
0x333	28870	28893	28881.1	3.07909	20%
0x4cc	44866	44888	44876.5	3.17184	30%
0x666	60899	60923	60911.4	3.25771	40%
0x800	76934	76957	76945.3	3.06887	50%
0x999	92929	92953	92939.6	3.19156	60%
0xb33	108965	108989	108976	3.22208	70%
0xccc	124961	124985	124972	3.30487	80%
0xe66	140998	141022	141010	3.14429	90%



TEST #6K: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

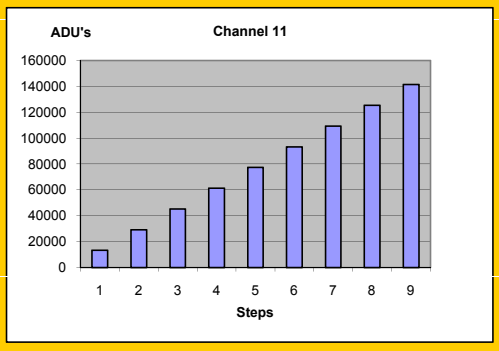
BrdTst6_006 / Channel 10					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13162	13186	13173.9	3.1507	10%
0x333	29137	29161	29150.1	3.11704	20%
0x4cc	45124	45147	45135.4	3.12293	30%
0x666	61136	61161	61150.7	3.20778	40%
0x800	77159	77182	77170.5	3.15305	50%
0x999	93141	93164	93152.8	3.11459	60%
0xb33	109155	109179	109168	3.21676	70%
0xccc	125142	125167	125154	3.32448	80%
0xe66	141158	141181	141169	3.25623	90%



TEST #6L: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

BrdTst6_006 / Channel 11					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13300	13323	13312.3	3.21004	10%
0x333	29296	29318	29306.4	3.24359	20%
0x4cc	45288	45312	45299.2	3.28057	30%
0x666	61321	61345	61332	3.14232	40%
0x800	77351	77375	77363.8	3.27342	50%
0x999	93345	93367	93355.6	3.2294	60%
0xb33	109377	109400	109389	3.19489	70%
0xccc	125372	125394	125383	3.20803	80%
0xe66	141405	141428	141416	3.19453	90%



Stage 13. Other Bit Tests. Table 11

Electronic Serial Number	0xDB6FA0		Board Serial Number	27
Firmware Version	0x193		Name Of Person Testing	S. Holm
Ident Register	0x502		Board passed Functional Tests	YES