DES 12 Channel Board - Functional Tests: CCD Acquisition Board Revision 1.0

Stage 1. Preparation of documentation and configuration settings - Table 1.

Board Part Number	#	Board Serial Number	2
Date Of Tests	November , 2009	Name Of Person Testing	S. Holm
Suggested Filename To Save	CCDACQ_12Ch_REPORT_BOARD#.xls	Sequence number: Test	

Stage 3. Power plane short test - Table 2.

Supply Name	Short test to ground: Impedance to ground	Test Point	
+1.2VD	80.00	TP43	~60 ohms
+1.8VD	1M	TPB12	> 1K ohm
+2.5VD	16k	TPB11	> 1K ohm
+3.3VD	23k	D13	> 1K ohm
+5VD	400k	D14	> 1K ohm
+5VA	1.1M	C267	> 1K ohm
-5VA	35k	C270	> 1K ohm *Found a short on this rail and fixed.
+15VA	1M	C288	> 1K ohm
-15VA	2M	C282	> 1K ohm
-28VA	500k	C307	> 1K ohm

Stage 4. Firmware programming tests - Table 3.

JTAG Order	Designator	Device	Load File	Check Sum or User Code
1	U122	XCF08PFS48C PROM	CcdAcqFpgaV41.mcs	0014ef670
2	U114	Spartan3 XC3S2000 FPGA	ccdacqfpgav41.bit	5102801

Stage 5. Power Consumption - Table 4.

Supply Name	Power Supply Consumption: Measured Voltage at test point	Measured Current on power supply	Test Point	
+1.2VD	1.20	N/A	TP43	
+1.8VD	1.80	N/A	TPB12	
+2.5VD	2.50	N/A	TPB11	
+3.3VD	3.30	0.1	D13	
+5VD	5.00	0.13	D14	
+5VA	5.00	0.55	C267	
-5VA	-5.00	0.44	C270	
+15VA	15.00	0.56	C288	
-15VA	-15.00	0.4	C282	
-28VA	-28.00	0.2	C307	
Vref 0+	10.00	N/A	R534	Vsub+ Reference(+10v)
Vref 0-	-2.50	N/A	R525	Vsub - Reference(-2.5v)
Vref Offset	2.50	N/A	R573	ADC Offset Reference(+2.5v)
Vclamp	1.80	N/A	VIA	ADC Clamp Voltage(+1.8v)
ADC Ref.	2.50	N/A	VIA	ADC Reference Voltage(+2.5v)
Vref 1+	2.50	N/A	R537	Vru and Vrl + Reference(+2.5v)
Vref 1-	-10.00	N/A	R535	Vru and Vrl - Reference(-10v)
Vref 2+	5.00	N/A	R563	Vog + Reference(+5v)
Vref 2-	-2.50	N/A	R555	Vog - Reference(-2.5v)
Vref 3+	2.50	N/A	R543	Vdd + Reference(+2.5v)
Vref 3-	-10.00	N/A	R571	Vdd - Reference(-10v)

Power Dissipation:
25.9 Watts

~27 watts +/- 5%

Stage 7. Basic Bus Transactions - **D**igital **Register** Tests - Table 5.

Register name	Put an X on any bit that has an error: 31-24	23-16	15-08	07-00	Function	Test name: Pattern	Walking 0's	Walking 1's
CDS Control			00000000	00000000	16 bit R/W			
Digital Output	00000000	00000000	00000000	00000000	32 bit R/W			
ADC Config.			0000	00000000	12 bit R/W			
Offset DAC			0000	00000000	12 bit R/W			
Bias DAC			0000	00000000	12 bit R/W			
Telemetry Config.				0000	4 bit R/W			
Auxilary Config.				00 00000000	10 bit R/W			
Redirect				0000	4 bit R/W			
Pixel Transfer				00000000	8 bit R/W			
Micro SEQ			00000000	00000000	16 bit R/W			
RAM Buffer			00000000	00000000	16 bit R/W			
LED Control				0000	4 bit R/W			
Control			00000000	00000000	16 bit R/W			
All Register Test	00000000	00000000	00000000	00000000	16 bit R/W	**YES**	**Passed**	**ALL**

Stage 8. Bias Voltage settings and output enables testing - Table 8

DAC Value	Bias Voltage Test Data 410	2048	3686	50% rms Noise	10-90% Rise Time	Fanout Brd	Slope	Offset
Signal	volts	volts	volts	uV	millisec.			
Vru 0	-13.12	-5.62	1.87	<10	1	BIAS 3	218.55	3276.96
Vru 1	-13.13	-5.62	1.87	<10	1	BIAS 4	218.40	3276.86
Vru 2	-13.12	-5.63	1.87	<10	1	BIAS 5	218.55	3277.68
Vru 3	-13.09	-5.61	1.87	<10	1	BIAS 6	218.98	3276.50
Vru 4	-13.10	-5.61	1.87	<10	1	BIAS 7	218.84	3276.41
Vru 5	-13.10	-5.61	1.87	<10	1	BIAS 8	218.84	3276.41
Vru 6	-13.10	-5.62	1.87	NA	NA	BIAS 9	218.84	3277.14
Vru 7	-13.10	-5.61	1.87	NA	NA	BIAS 10	218.84	3276.41
Vrl 0	-13.12	-5.62	1.87	<10	1	BIAS 11	218.55	3276.96
Vrl 1	-13.12	-5.62	1.87	<10	1	BIAS 12	218.55	3276.96
Vrl 2	-13.09	-5.61	1.87	<10	1	BIAS 13	218.98	3276.50
Vrl 3	-13.13	-5.63	1.87	<10	1	BIAS 14	218.40	3277.59
Vrl 4	-13.10	-5.61	1.87	<10	1	BIAS 15	218.84	3276.41
Vrl 5	-13.09	-5.61	1.87	<10	1	BIAS 16	218.98	3276.50
Vrl 6	-13.11	-5.62	1.87	NA	NA	BIAS 17	218.69	3277.05
Vrl 7	-13.11	-5.62	1.87	NA	NA	BIAS 18	218.69	3277.05
Vog 0	-1.75	1.25	4.24	<10	1	BIAS 19	546.91	1366.18
Vog 1	-1.75	1.25	4.24	<10	1	BIAS 20	546.91	1366.18
Vog 2	-1.75	1.25	4.24	<10	1	BIAS 21	546.91	1366.18
Vog 3	-1.75	1.25	4.24	<10	1	BIAS 22	546.91	1366.18
Vog 4	-1.75	1.25	4.24	<10	1	BIAS 23	546.91	1366.18
Vog 5	-1.75	1.25	4.24	<10	1	BIAS 24	546.91	1366.18
Vog 6	-1.75	1.25	4.24	NA	NA	BIAS 25	546.91	1366.18
Vog 7	-1.75	1.25	4.24	NA	NA	BIAS 26	546.91	1366.18
Vdd 0	-21.90	-9.40	3.10	<10	40	BIAS 27	131.04	3279.78
Vdd 1	-21.94	-9.41	3.11	<10	40	BIAS 28	130.78	3279.06
Vdd 2	-21.95	-9.42	3.11	<10	40	BIAS 29	130.73	3279.44
Vdd 3	-21.87	-9.38	3.10	<10	40	BIAS 30	131.20	3279.07
Vdd 4	-21.94	-9.41	3.12	<10	40	BIAS 21	130.73	3278.13
Vdd 5	-21.92	-9.41	3.11	<10	40	BIAS 32	130.88	3279.17
Vdd 6	-21.96	-9.42	3.12	NA	NA	BIAS 33	130.62	3278.46
Vdd 7	-21.96	-9.43	3.11	NA	NA	BIAS 34	130.67	3279.82

Vru	Slope		Offset
Mean	218.73	Mean	3276.80
Stdev	0.189658	Stdev	0.42902354
Average	218.72822	Average	3276.79575
	Dac #	Average voltage	
	0	-14.0	
	4095	3.7	

Vrl	Slope		Offset
Mean	218.71	Mean	3276.88
Stdev	0.1991193	Stdev	0.368214194
Average	218.71001	Average	3276.875542
	Dac #	Average voltage	
	0	-15.0	
	4095	3.7	

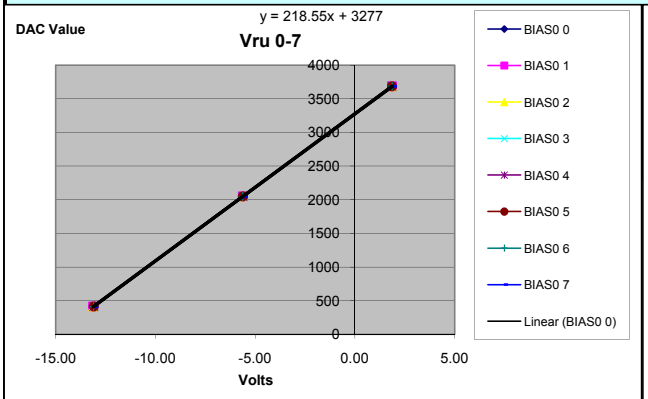
Vog	Slope		Offset
Mean	546.91	Mean	1366.18
Stdev	0	Stdev	0
Average	546.91101	Average	1366.184273
	Dac #	Average voltage	
	0	-2.5	
	4095	5.0	

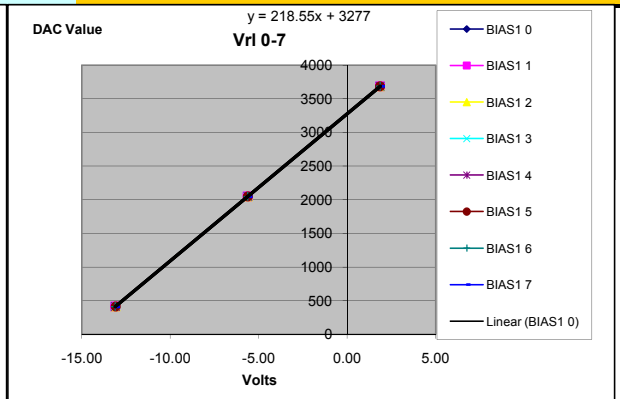
Vdd	Slope		Offset
Mean	130.83	Mean	3279.12
Stdev	0.1849483	Stdev	0.552556143
Average	130.83093	Average	3279.116793
	Dac #	Average voltage	
	0	-25.1	
	4095	6.2	

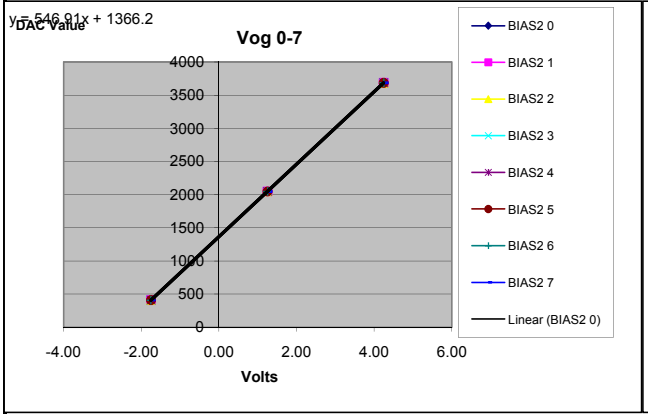
Notes and Observations

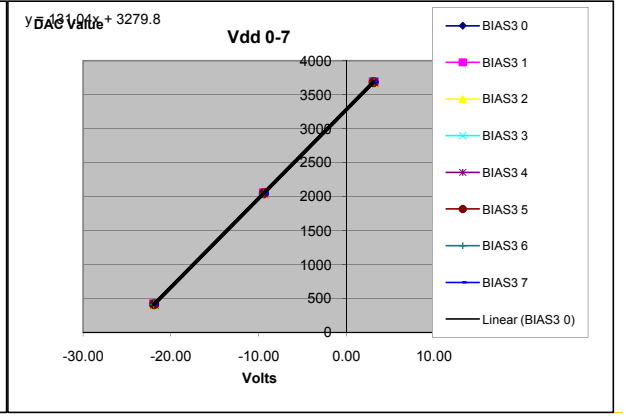
Checked for oscillations using a Agilent Oscilloscpe on AC. OK

average min & max voltages
(dac# -offset)/slope=voltage









Stage 8B. Telemetry System Tests - Table 7 (Bias Telemetry Tests)

DAC Value	410	3686	Bias Signals		Resolved Values for	
	Telemetry Return Values		Set Volts		Telemetry Channel	
Signal	10%	90%	10%	90%	Slope	Offset
Vru 0	-1732	420	-13.12	1.87	143.5624	151.54
Vru 1	-1732	421	-13.13	1.87	143.5333	152.59
Vru 2	-1733	423	-13.12	1.87	143.8292	154.04
Vru 3	-1726	423	-13.09	1.87	143.6497	154.38
Vru 4	-1730	423	-13.10	1.87	143.8210	154.05
Vru 5	-1728	423	-13.10	1.87	143.6874	154.30
Vru 6	-1729	423	-13.10	1.87	143.7542	154.18
Vru 7	-1730	423	-13.10	1.87	143.8210	154.05
Vrl 0	-1733	424	-13.12	1.87	143.8959	154.91
Vrl 1	-1732	424	-13.12	1.87	143.8292	155.04
Vrl 2	-1729	424	-13.09	1.87	143.9171	154.88
Vrl 3	-1734	425	-13.13	1.87	143.9333	155.84
Vrl 4	-1731	424	-13.10	1.87	143.9546	154.80
Vrl 5	-1729	424	-13.09	1.87	143.9171	154.88
Vrl 6	-1730	424	-13.11	1.87	143.7917	155.11
Vrl 7	-1727	424	-13.11	1.87	143.5915	155.48
Vog 0	-362	867	-1.75	4.24	205.1753	-2.94
Vog 1	-362	867	-1.75	4.24	205.1753	-2.94
Vog 2	-362	867	-1.75	4.24	205.1753	-2.94
Vog 3	-362	867	-1.75	4.24	205.1753	-2.94
Vog 4	-362	867	-1.75	4.24	205.1753	-2.94
Vog 5	-361	867	-1.75	4.24	205.0083	-2.24
Vog 6	-362	867	-1.75	4.24	205.1753	-2.94
Vog 7	-361	867	-1.75	4.24	205.0083	-2.24
Vdd 0	-1688	572	-21.90	3.10	90.4000	291.76
Vdd 1	-1691	574	-21.94	3.11	90.4192	292.80
Vdd 2	-1696	573	-21.95	3.11	90.5427	291.41
Vdd 3	-1686	573	-21.87	3.10	90.4686	292.55
Vdd 4	-1691	574	-21.94	3.12	90.3831	292.00
Vdd 5	-1688	573	-21.92	3.11	90.3316	292.07
Vdd 6	-1692	574	-21.96	3.12	90.3509	292.11
Vdd 7	-1696	574	-21.96	3.11	90.5465	292.40

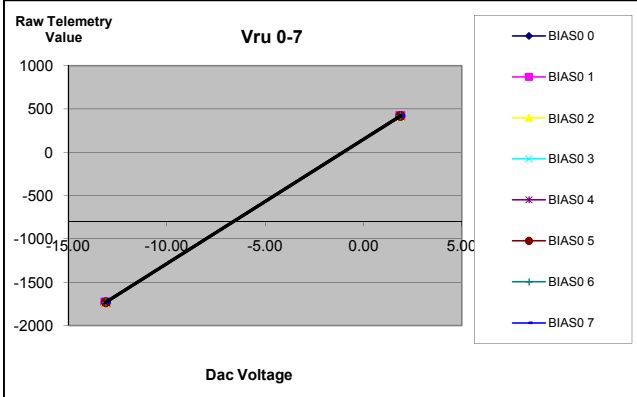
AVERAGE

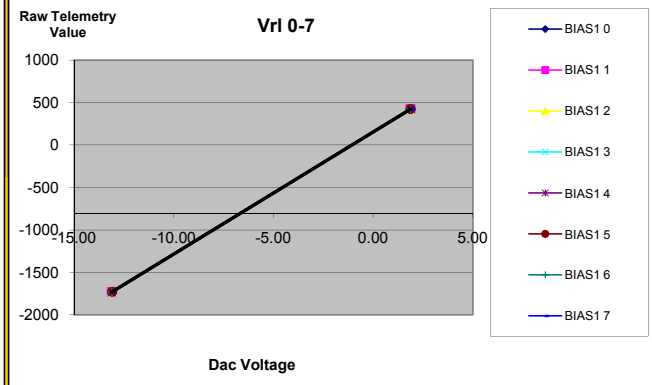
Vru	Slope		Offset
Mean	143.71	Mean	153.64
Stdev	0.1106145	Stdev	0.9546283

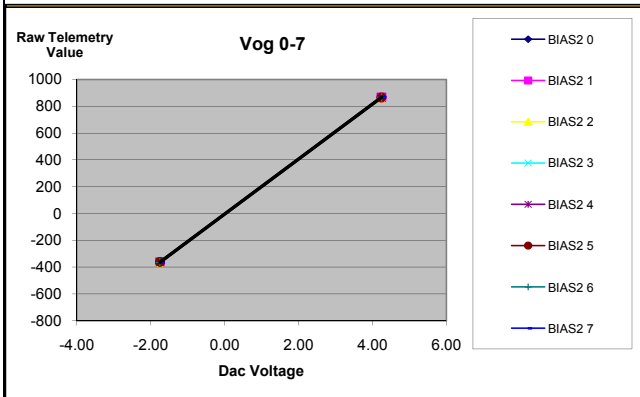
Vrl	Slope		Offset
Mean	143.85	Mean	155.12
Stdev	0.1115548	Stdev	0.3401674

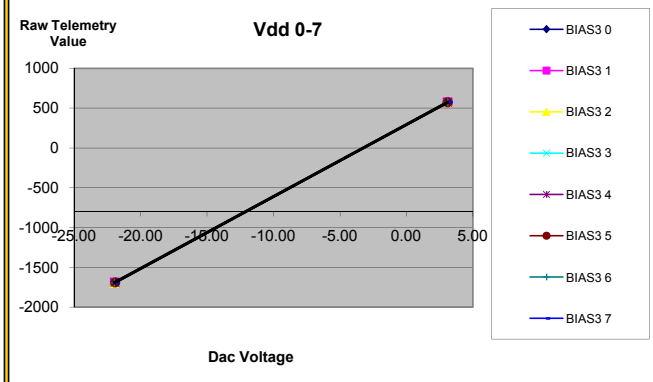
Vog	Slope		Offset
Mean	205.13	Mean	-2.77
Stdev	0.0722893	Stdev	0.3065065

Vdd	Slope		Offset
Mean	90.43	Mean	292.14
Stdev	0.0765782	Stdev	0.4128123









Stage 8C. Bias Voltage output enables testing - Table 8

Place a line through Bias Voltage name if enable/disable switch works

~~Vru 0~~	~~Vru 1~~	~~Vru 2~~	~~Vru 3~~	~~Vru 4~~	~~Vru 5~~
~~Vrl 0~~	~~Vrl 1~~	~~Vrl 2~~	~~Vrl 3~~	~~Vrl 4~~	~~Vrl 5~~
~~Vog 0~~	~~Vog 1~~	~~Vog 2~~	~~Vog 3~~	~~Vog 4~~	~~Vog 5~~
~~Vdd 0~~	~~Vdd 1~~	~~Vdd 2~~	~~Vdd 3~~	~~Vdd 4~~	~~Vdd 5~~

Stage 9. Vsub and Heater Control testing - Table 9

DAC Value	Vsub Measured Voltage Test Data		
	10%	50%	90%
Signal	volts	volts	volts
Vsub - rate	-1.25	3.75	8.75

Vsub - Limit	-1.25	3.75	8.75
Vsub0	0.00	3.75	8.75
	Vsub Enable Bit - pass		

DAC	Telemetery Readback Test Data		
Value	10%	50%	90%
Signal	dec	dec	dec
Vbias 0	73.00	363.00	725.00
Vbias 1	-21.00	694.00	1408.00
RTD1	220.00	NA	NA
RTD2	248.00	NA	NA
RTD3	275.00	NA	NA
RTD4	301.00	NA	NA
RTD5	324.00	NA	NA
RTD6	351.00	NA	NA
Reference 4096	836.00	NA	NA
eference buffere	837.00	NA	NA

Stage 10. Video Offset DAC Tests - Table 10.

	DAC Value 410				DAC Value 2048				DAC Value 3686			
ADC	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU
0	0.250	NA	NA	56276	1.250		NA	120389	2.250	NA	400ms	184512
1	0.250	NA	NA	56437	1.250		NA	120541	2.250	NA	400ms	184647
2	0.250	NA	NA	56386	1.250		NA	120374	2.250	NA	400ms	184366
3	0.250	NA	NA	56432	1.250		NA	120428	2.250	NA	400ms	184407
4	0.250	NA	NA	56419	1.250		NA	120501	2.250	NA	400ms	184582
5	0.250	NA	NA	56420	1.250		NA	120565	2.250	NA	400ms	184700
6	0.250	NA	NA	56392	1.250		NA	120492	2.250	NA	400ms	184593
7	0.250	NA	NA	56502	1.250		NA	120525	2.250	NA	400ms	184537
8	0.250	NA	NA	56306	1.250		NA	120338	2.250	NA	400ms	184365
9	0.250	NA	NA	56438	1.250		NA	120453	2.250	NA	400ms	184474
10	0.250	NA	NA	56282	1.250		NA	120315	2.250	NA	400ms	184348
11	0.250	NA	NA	56452	1.250		NA	120445	2.250	NA	400ms	184451

ADC	DC Volts		Data Set		
Channel	Slope	Offset	410	2048	3686
0	1638.000	0.500	0.250	1.250	2.250
1	1638.000	0.500	0.250	1.250	2.250
2	1638.000	0.500	0.250	1.250	2.250
3	1638.000	0.500	0.250	1.250	2.250
4	1638.000	0.500	0.250	1.250	2.250
5	1638.000	0.500	0.250	1.250	2.250
6	1638.000	0.500	0.250	1.250	2.250
7	1638.000	0.500	0.250	1.250	2.250
8	1638.000	0.500	0.250	1.250	2.250
9	1638.000	0.500	0.250	1.250	2.250
10	1638.000	0.500	0.250	1.250	2.250
11	1638.000	0.500	0.250	1.250	2.250

(dac# -offset)/slope=Voltage

ADC	ADU's		Data Set		
Channel	Slope	Offset	410	2048	3686
0	0.026	-1027.62	56276	120389	184512
1	0.026	-1032.06	56437	120541	184647
2	0.026	-1033.34	56386	120374	184366
3	0.026	-1034.66	56432	120428	184407
4	0.026	-1032.14	56419	120501	184582
5	0.026	-1030.89	56420	120565	184700
6	0.026	-1031.02	56392	120492	184593
7	0.026	-1035.75	56502	120525	184537
8	0.026	-1030.44	56306	120338	184365
9	0.026	-1034.03	56438	120453	184474
10	0.026	-1029.73	56282	120315	184348
11	0.026	-1034.77	56452	120445	184451

(dac# -offset)/slope=ADU

Notes and Observations

Checked for oscillations using a Agilent Oscilloscope on AC. OK

Stage 11. CDS Control Functions and Video Channel Performanc

TEST #1: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit is held static. The purpose of this test is to verify the correct operation of the ADC devices and measure the noise of the Offset voltage generators, ADC buffer amplifiers and ADC devices

Noise Test 1

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	104371	104392	104381	2.87556
CH 1	104524	104545	104535	3.15092
CH 2	104378	104400	104388	3.07943
CH 3	104429	104450	104439	2.9933
CH 4	104484	104503	104493	2.87948
CH 5	104528	104549	104538	3.05993
CH 6	104476	104499	104488	2.88794
CH 7	104524	104546	104535	2.94981
CH 8	104339	104361	104351	2.76165
CH 9	104457	104479	104469	3.05854
CH 10	104316	104336	104325	2.86226
CH 11	104456	104477	104466	2.93233

TEST #2: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the invert/non-invert and the DC Restore switches are held static.

Noise Test 2

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	99630	99656	99642	3.40787
CH 1	100341	100365	100352	3.49682
CH 2	99864	99886	99875.2	3.19267
CH 3	100184	100208	100196	3.47433
CH 4	99793	99815	99803.4	3.27874
CH 5	100360	100384	100372	3.47644
CH 6	100118	100143	100131	3.21267
CH 7	100336	100360	100348	3.4019
CH 8	99881	99904	99892.6	3.08601
CH 9	100503	100527	100514	3.31008
CH 10	99845	99869	99857.5	3.24117
CH 11	100319	100344	100330	3.22087

TEST #3: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the DC Restore switch is held static.

Noise Test 3

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	99624	99652	99637.5	3.63718
CH 1	100332	100360	100347	3.66101
CH 2	99860	99884	99872.7	3.40198
CH 3	100188	100216	100203	3.69959
CH 4	99774	99800	99787.6	3.46364
CH 5	100357	100382	100369	3.63735
CH 6	100112	100137	100124	3.53427
CH 7	100332	100356	100343	3.61045
CH 8	99882	99904	99892.9	3.2479
CH 9	101001	101024	101012	3.25528
CH 10	99850	99873	99861	3.45524
CH 11	100320	100345	100332	3.45755

TEST #4: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition.

Noise Test 4

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	99621	99647	99633.2	3.80407
CH 1	100338	100364	100351	3.75498
CH 2	99863	99888	99875.7	3.43366
CH 3	100189	100216	100202	3.87193
CH 4	99812	99837	99824.8	3.61426
CH 5	100345	100372	100358	3.61541
CH 6	100122	100147	100134	3.47813
CH 7	100285	100312	100299	3.6355
CH 8	99923	99948	99935.1	3.45207
CH 9	101063	101088	101076	3.5257
CH 10	99867	99892	99878.3	3.34217
CH 11	100274	100303	100289	3.72569

TEST #5: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the circuitry set to high GAIN.

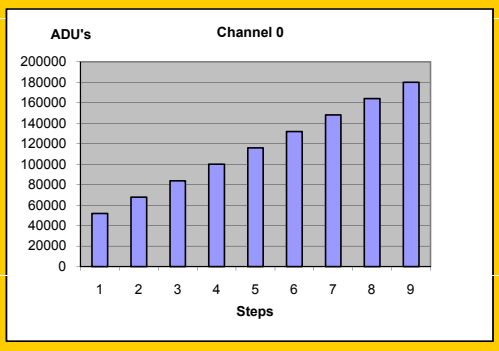
Noise Test 5

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	99620	99644	99632.3	3.80508
CH 1	100338	100362	100350	3.75435
CH 2	99860	99887	99874.6	3.5012
CH 3	100188	100220	100203	3.82165
CH 4	99812	99838	99824.9	3.58664
CH 5	100346	100371	100357	3.607
CH 6	100121	100147	100134	3.49585
CH 7	100282	100312	100297	3.68469
CH 8	99923	99947	99934.6	3.4377
CH 9	101062	101088	101076	3.55043
CH 10	99867	99890	99878	3.32508
CH 11	100276	100302	100289	3.68651

TEST #6A: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

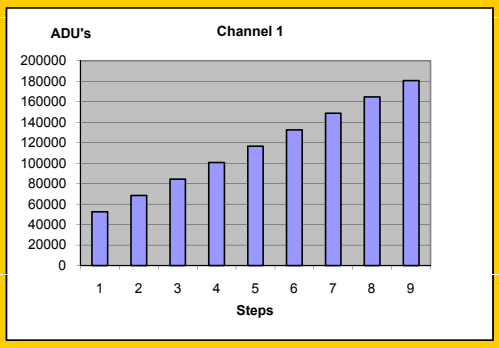
BrdTst6_006 / Channel 0					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	51838	51865	51852.6	3.73242	10%
0x333	67848	67876	67861.4	3.73806	20%
0x4cc	83859	83887	83872.8	3.69774	30%
0x666	99905	99931	99918.4	3.71102	40%
0x800	115954	115982	115967	3.75597	50%
0x999	131965	131994	131978	3.80709	60%
0xb33	148014	148041	148028	3.72504	70%
0xccc	164031	164059	164044	3.87332	80%
0xe66	180080	180106	180092	3.8339	90%



TEST #6B: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

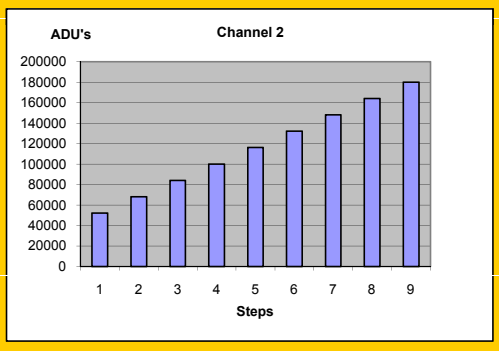
BrdTst6_006 / Channel 1					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	52464	52490	52477	3.94691	10%
0x333	68466	68496	68482.2	3.7664	20%
0x4cc	84474	84500	84487.7	3.881	30%
0x666	100517	100546	100531	3.85659	40%
0x800	116560	116592	116576	3.67751	50%
0x999	132571	132598	132584	3.7756	60%
0xb33	148617	148643	148629	3.59447	70%
0xccc	164624	164651	164638	3.71637	80%
0xe66	180670	180697	180684	3.80353	90%



TEST #6C: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

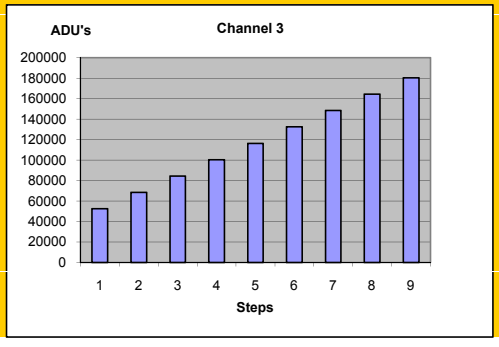
BrdTst6_006 / Channel 2					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	52141	52167	52153.3	3.70536	10%
0x333	68119	68146	68130.6	3.55413	20%
0x4cc	84096	84122	84108.3	3.78026	30%
0x666	100111	100137	100124	3.73201	40%
0x800	116127	116152	116140	3.67519	50%
0x999	132106	132132	132119	3.65652	60%
0xb33	148124	148151	148138	3.76403	70%
0xccc	164105	164134	164119	3.79393	80%
0xe66	180123	180150	180137	3.74328	90%



TEST #6D: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

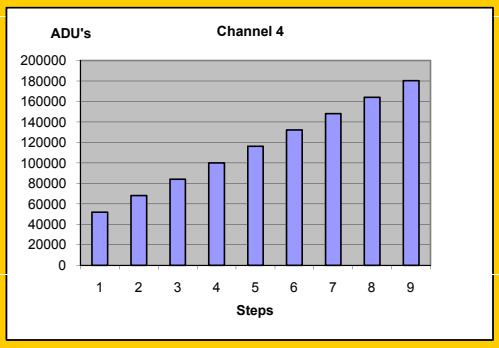
BrdTst6_006 / Channel 3					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	52416	52448	52432.2	3.86568	10%
0x333	68395	68424	68409	3.89448	20%
0x4cc	84372	84400	84385.3	3.62164	30%
0x666	100387	100413	100400	3.6726	40%
0x800	116405	116431	116418	3.61788	50%
0x999	132379	132407	132393	3.75365	60%
0xb33	148399	148424	148412	3.81636	70%
0xccc	164379	164405	164391	3.6997	80%
0xe66	180393	180423	180408	3.7526	90%



TEST #6E: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

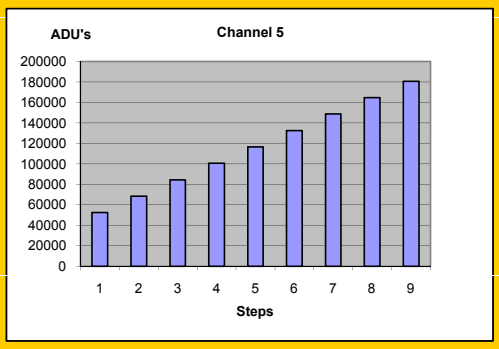
BrdTst6_006 / Channel 4					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	52013	52044	52030.6	3.56773	10%
0x333	68018	68045	68031.1	3.59005	20%
0x4cc	84018	84047	84033.4	3.52145	30%
0x666	100060	100083	100071	3.53608	40%
0x800	116098	116123	116111	3.58533	50%
0x999	132102	132128	132115	3.47008	60%
0xb33	148145	148170	148156	3.65149	70%
0xccc	164146	164175	164161	3.64956	80%
0xe66	180190	180214	180202	3.55539	90%



TEST #6F: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

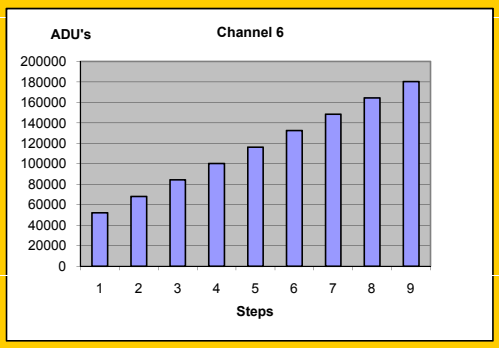
BrdTst6_006 / Channel 5					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	52464	52492	52479.1	3.86758	10%
0x333	68480	68506	68493.7	3.73208	20%
0x4cc	84497	84521	84508.9	3.62265	30%
0x666	100549	100576	100562	3.88713	40%
0x800	116596	116626	116611	3.65217	50%
0x999	132613	132642	132629	3.70003	60%
0xb33	148671	148698	148684	3.71825	70%
0xccc	164689	164715	164703	3.71665	80%
0xe66	180741	180770	180757	3.59801	90%



TEST #6G: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

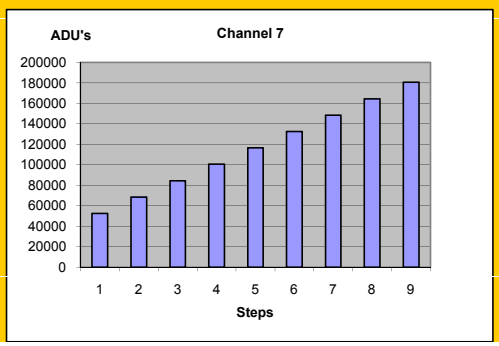
BrdTst6_006 / Channel 6					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	52258	52284	52271.6	3.73172	10%
0x333	68262	68289	68275.4	3.67675	20%
0x4cc	84274	84300	84288	3.65435	30%
0x666	100316	100341	100329	3.68086	40%
0x800	116356	116381	116369	3.53368	50%
0x999	132364	132389	132375	3.55839	60%
0xb33	148403	148435	148420	3.58838	70%
0xccc	164421	164448	164435	3.71809	80%
0xe66	180465	180492	180478	3.5699	90%



TEST #6H: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

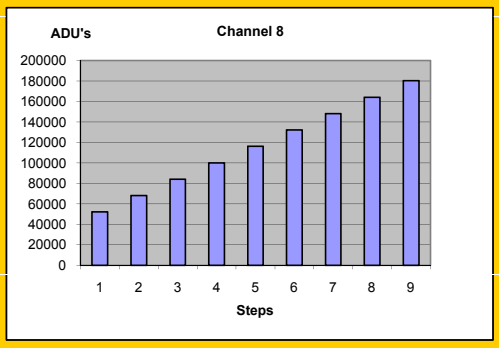
BrdTst6_006 / Channel 7					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	52496	52520	52507.9	3.64814	10%
0x333	68476	68504	68489.5	3.69105	20%
0x4cc	84464	84493	84478.1	3.69285	30%
0x666	100486	100513	100498	3.60269	40%
0x800	116507	116534	116519	3.54141	50%
0x999	132491	132518	132505	3.60137	60%
0xb33	148515	148540	148528	3.66323	70%
0xccc	164507	164533	164519	3.88768	80%
0xe66	180529	180558	180541	3.69945	90%



TEST #6I: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

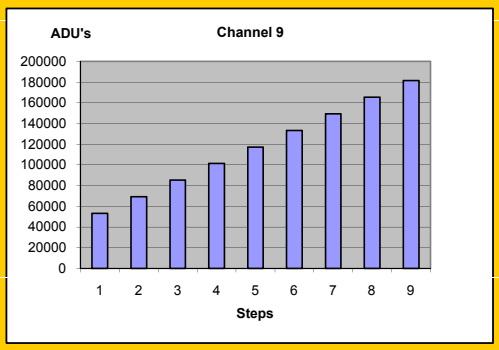
BrdTst6_006 / Channel 8					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	52151	52177	52165.2	3.63752	10%
0x333	68140	68166	68154.1	3.52731	20%
0x4cc	84128	84154	84141	3.60435	30%
0x666	100156	100183	100168	3.5467	40%
0x800	116181	116208	116195	3.67524	50%
0x999	132172	132199	132184	3.54921	60%
0xb33	148202	148231	148214	3.60775	70%
0xccc	164189	164216	164203	3.53249	80%
0xe66	180219	180245	180232	3.52399	90%



TEST #6J: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

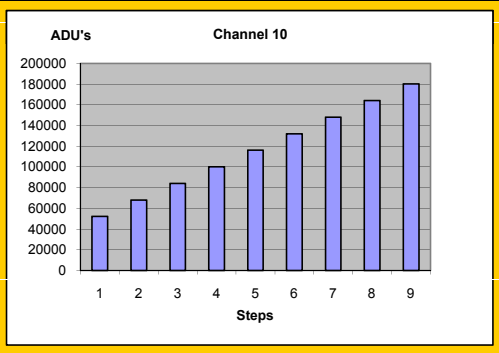
BrdTst6_006 / Channel 9					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	53280	53307	53294.3	3.76686	10%
0x333	69266	69292	69278.7	3.62828	20%
0x4cc	85250	85276	85263.1	3.60605	30%
0x666	101273	101298	101286	3.6231	40%
0x800	117298	117321	117310	3.57945	50%
0x999	133280	133306	133294	3.68628	60%
0xb33	149302	149331	149319	3.62301	70%
0xccc	165292	165317	165305	3.5813	80%
0xe66	181318	181342	181331	3.68847	90%



TEST #6K: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

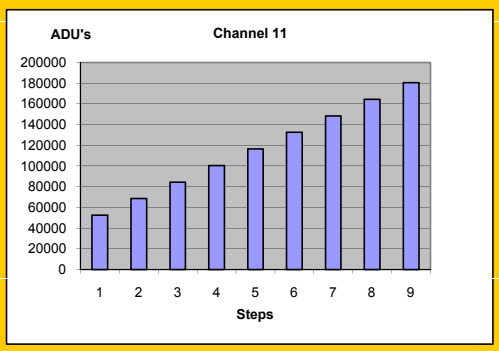
BrdTst6_006 / Channel 10					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	52092	52118	52105.1	3.61256	10%
0x333	68080	68107	68093	3.63786	20%
0x4cc	84067	84095	84081	3.68708	30%
0x666	100094	100120	100108	3.58064	40%
0x800	116121	116146	116135	3.48289	50%
0x999	132111	132138	132125	3.54418	60%
0xb33	148142	148166	148154	3.53856	70%
0xccc	164133	164158	164146	3.50022	80%
0xe66	180162	180186	180175	3.54423	90%



TEST #6L: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

BrdTst6_006 / Channel 11					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	52507	52534	52520.3	3.6532	10%
0x333	68488	68512	68499.4	3.54012	20%
0x4cc	84466	84492	84478.8	3.7496	30%
0x666	100484	100508	100497	3.4582	40%
0x800	116505	116528	116517	3.38041	50%
0x999	132483	132506	132495	3.51815	60%
0xb33	148503	148529	148516	3.44556	70%
0xccc	164485	164513	164498	3.6513	80%
0xe66	180503	180531	180517	3.59869	90%



Stage 13. Other Bit Tests. Table 11

Electronic Serial Number	0xDB9128		Board Serial Number	2
Firmware Version	0x191		Name Of Person Testing	S. Holm
Ident Register	0x502		Board passed Functional Tests	YES