DES 12 Channel Board - Functional Tests: CCD Acquisition Board Revision 1.0

Stage 1. Preparation of documentation and configuration settings - Table 1.

Board Part Number	16		Board Serial Number	0xDB6FA9
Date Of Tests	May 2010		Name Of Person Testing	S. Holm
Suggested Filename To Save	CCDACQ_12Ch_REPORT_BOARD16.xl		Sequence number: Test	

Stage 3. Power plane short test - Table 2.

Supply Name	Short test to ground: Impedance to ground	Test Point	
+1.2VD	56.80	TP43	~50 ohms
+1.8VD	2M	TPB12	> 1K ohm
+2.5VD	17K	TPB11	> 1K ohm
+3.3VD	6K	D13	> 1K ohm
+5VD	18K	D14	> 1K ohm
+5VA	4M	C267	> 1K ohm
-5VA	300k	C270	> 1K ohm
+15VA	500K	C288	> 1K ohm
-15VA	500K	C282	> 1K ohm
-28VA	300K	C307	> 1K ohm

Stage 4. Firmware programming tests - Table 3.

JTAG Order	Designator	Device	Load File	Check Sum or User Code
1	U122	XCF08PFS48C PROM	CcdAcqFpgaV41.mcs	0014ef670
2	U114	Spartan3 XC3S2000 FPGA	ccdacqfpgav41.bit	5102801

Stage 5. Power Consumption - Table 4.

Supply Name	Power Supply Consumption: Measured Voltage at test point	Measured Current on power supply	Test Point	
+1.2VD	1.20	N/A	TP43	
+1.8VD	1.80	N/A	TPB12	
+2.5VD	2.51	N/A	TPB11	
+3.3VD	3.27	0.257	D13	
+5VD	5.20	0.151	D14	
+5VA	5.03	0.545	C267	
-5VA	-5.02	0.434	C270	
+15VA	15.12	0.567	C288	
-15VA	-15.04	0.417	C282	
-28VA	-28.03	0.196	C307	
Vref 0+	10.04	N/A	R534	Vsub+ Reference(+10v)
Vref 0-	-2.49	N/A	R525	Vsub - Reference(-2.5v)
Vref Offset	2.50	N/A	R573	ADC Offset Reference(+2.5v)
Vclamp	1.87	N/A	VIA	ADC Clamp Voltage(+1.8v)
ADC Ref.	2.50	N/A	VIA	ADC Reference Voltage(+2.5v)
Vref 1+	2.50	N/A	R537	Vru and Vrl + Reference(+2.5v)
Vref 1-	-10.02	N/A	R535	Vru and Vrl - Reference(-10v)
Vref 2+	4.99	N/A	R563	Vog + Reference(+5v)
Vref 2-	-2.50	N/A	R555	Vog - Reference(-2.5v)
Vref 3+	2.50	N/A	R543	Vdd + Reference(+2.5v)
Vref 3-	-10.02	N/A	R571	Vdd - Reference(-10v)

Power Dissipation:
26.9 Watts

~27 watts +/- 5%

Stage 7. Basic Bus Transactions - **D**igital **Register** Tests - Table 5.

Register name	Put an X on any bit that has an error: 31-24	23-16	15-08	07-00	Function	Test name: Pattern	Walking 0's	Walking 1's
CDS Control			00000000	00000000	16 bit R/W			
Digital Output	00000000	00000000	00000000	00000000	32 bit R/W			
ADC Config.			0000	00000000	12 bit R/W			
Offset DAC			0000	00000000	12 bit R/W			
Bias DAC			0000	00000000	12 bit R/W			
Telemetry Config.				0000	4 bit R/W			
Auxilary Config.			00	00000000	10 bit R/W			
Redirect				0000	4 bit R/W			
Pixel Transfer				00000000	8 bit R/W			
Micro SEQ			00000000	00000000	16 bit R/W			
RAM Buffer			00000000	00000000	16 bit R/W			
LED Control				0000	4 bit R/W			
Control			00000000	00000000	16 bit R/W			
All Register Test	00000000	00000000	00000000	00000000	16 bit R/W	**Passed**	**Passed**	**Passed**

Stage 8. Bias Voltage settings and output enables testing - Table 8

DAC Value	410	Bias Voltage Test Data 2048	3686	50% rms Noise	10-90% Rise Time			
Signal	volts	volts	volts	uV	millisec.	Fanout Brd	Slope	Offset
Vru 0	-13.15	-5.64	1.87	<10	2	BIAS 3	218.11	3278.14
Vru 1	-13.15	-5.64	1.87	<10	2	BIAS 4	218.11	3278.14
Vru 2	-13.15	-5.64	1.87	<10	2	BIAS 5	218.11	3278.14
Vru 3	-13.15	-5.64	1.87	<10	2	BIAS 6	218.11	3278.14
Vru 4	-13.15	-5.64	1.87	<10	2	BIAS 7	218.11	3278.14
Vru 5	-13.15	-5.64	1.87	<10	2	BIAS 8	218.11	3278.14
Vru 6	-13.15	-5.64	1.87	NA	NA	BIAS 9	218.11	3278.14
Vru 7	-13.15	-5.64	1.87	NA	NA	BIAS 10	218.11	3278.14
Vrl 0	-13.15	-5.64	1.87	<10	2	BIAS 11	218.11	3278.14
Vrl 1	-13.15	-5.64	1.87	<10	2	BIAS 12	218.11	3278.14
Vrl 2	-13.15	-5.64	1.87	<10	2	BIAS 13	218.11	3278.14
Vrl 3	-13.15	-5.64	1.87	<10	2	BIAS 14	218.11	3278.14
Vrl 4	-13.15	-5.64	1.87	<10	2	BIAS 15	218.11	3278.14
Vrl 5	-13.15	-5.64	1.87	<10	2	BIAS 16	218.11	3278.14
Vrl 6	-13.15	-5.64	1.87	NA	NA	BIAS 17	218.11	3278.14
Vrl 7	-13.15	-5.64	1.87	NA	NA	BIAS 18	218.11	3278.14
Vog 0	-1.75	1.25	4.24	<10	2	BIAS 19	546.91	1366.18
Vog 1	-1.75	1.25	4.24	<10	2	BIAS 20	546.91	1366.18
Vog 2	-1.75	1.25	4.24	<10	2	BIAS 21	546.91	1366.18
Vog 3	-1.75	1.25	4.24	<10	2	BIAS 22	546.91	1366.18
Vog 4	-1.75	1.25	4.24	<10	2	BIAS 23	546.91	1366.18
Vog 5	-1.75	1.25	4.24	<10	2	BIAS 24	546.91	1366.18
Vog 6	-1.75	1.25	4.24	NA	NA	BIAS 25	546.91	1366.18
Vog 7	-1.75	1.25	4.24	NA	NA	BIAS 26	546.91	1366.18
Vdd 0	-21.91	-9.40	3.11	<10	20	BIAS 27	130.94	3278.79
Vdd 1	-21.89	-9.39	3.11	<10	20	BIAS 28	131.04	3278.47
Vdd 2	-21.93	-9.41	3.11	<10	20	BIAS 29	130.83	3279.12
Vdd 3	-21.99	-9.44	3.12	<10	20	BIAS 30	130.47	3279.16
Vdd 4	-21.91	-9.41	3.11	<10	20	BIAS 21	130.94	3279.23
Vdd 5	-21.93	-9.41	3.11	<10	20	BIAS 32	130.83	3279.12
Vdd 6	-22.01	-9.44	3.12	NA	NA	BIAS 33	130.36	3279.05
Vdd 7	-21.86	-9.38	3.10	NA	NA	BIAS 34	131.25	3279.13

Vru	Slope		Offset
Mean	218.11	Mean	3278.14
Stdev	2.842E-14	Stdev	0
Average	218.10919	Average	3278.135819
	Dac #	Average voltage	
	0	-15.0	
	4095	3.7	

Vrl	Slope		Offset
Mean	218.11	Mean	3278.14
Stdev	2.842E-14	Stdev	0
Average	218.10919	Average	3278.135819
	Dac #	Average voltage	
	0	-15.0	
	4095	3.7	

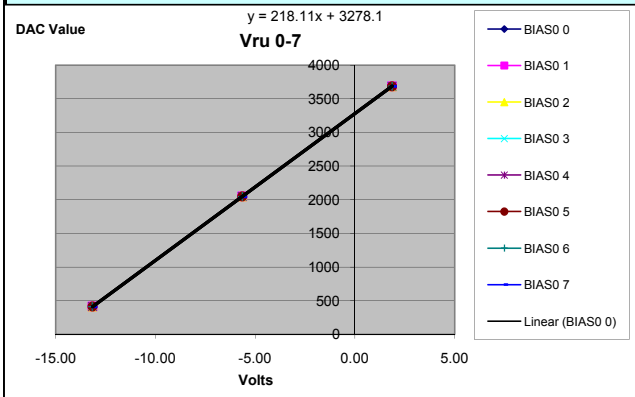
Vog	Slope		Offset
Mean	546.91	Mean	1366.18
Stdev	0	Stdev	0
Average	546.91101	Average	1366.184273
	Dac #	Average voltage	
	0	-2.5	
	4095	5.0	

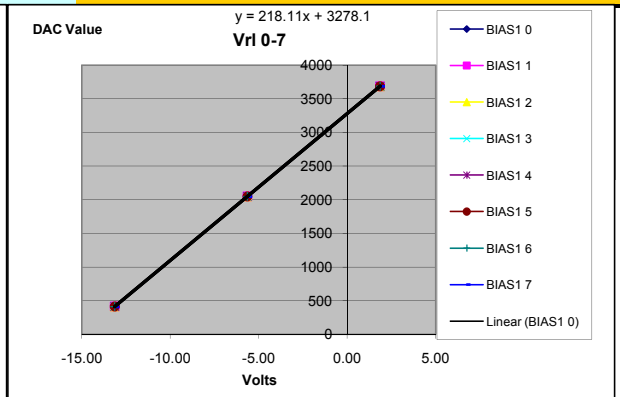
Vdd	Slope		Offset
Mean	130.83	Mean	3279.01
Stdev	0.2725108	Stdev	0.237918189
Average	130.83123	Average	3279.007403
	Dac #	Average voltage	
	0	-25.1	
	4095	6.2	

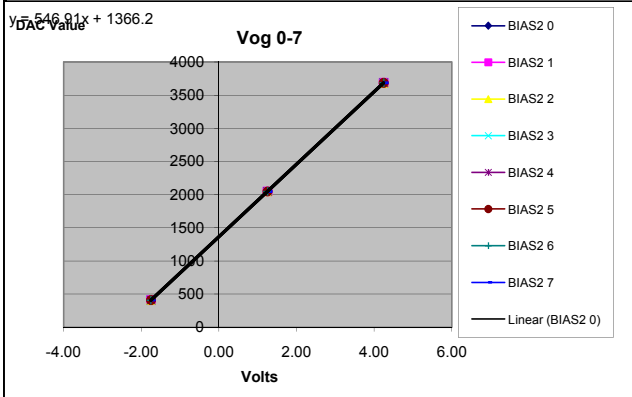
Notes and Observations

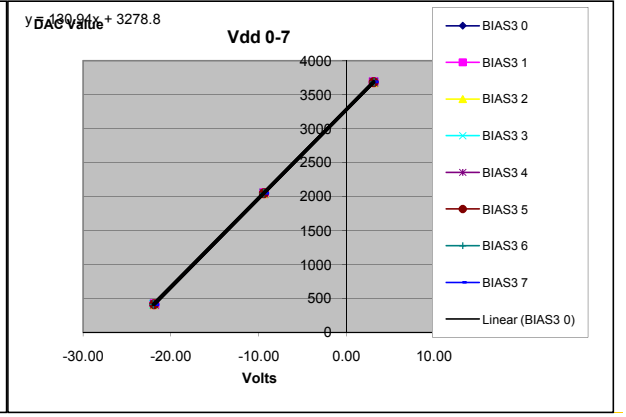
Checked for oscillations using a Agilent Oscilloscpe on AC.**OK**

average min & max voltages
(dac# -offset)/slope=voltage









Stage 8B. Telemetry System Tests - Table 7 (Bias Telemetry Tests)

DAC Value: 410 / 3686

Signal	Telemetry Return Values 10%	90%	Bias Signals Set Volts 10%	90%	Resolved Values for Telemetry Channel Slope	Offset
Vru 0	-1758	422	-13.15	1.87	145.1398	150.59
Vru 1	-1761	422	-13.15	1.87	145.3395	150.22
Vru 2	-1760	422	-13.15	1.87	145.2730	150.34
Vru 3	-1754	422	-13.15	1.87	144.8735	151.09
Vru 4	-1759	422	-13.15	1.87	145.2064	150.46
Vru 5	-1760	422	-13.15	1.87	145.2730	150.34
Vru 6	-1760	422	-13.15	1.87	145.2730	150.34
Vru 7	-1760	422	-13.15	1.87	145.2730	150.34
Vrl 0	-1760	422	-13.15	1.87	145.2730	150.34
Vrl 1	-1760	422	-13.15	1.87	145.2730	150.34
Vrl 2	-1759	422	-13.15	1.87	145.2064	150.46
Vrl 3	-1763	423	-13.15	1.87	145.5393	150.84
Vrl 4	-1763	423	-13.15	1.87	145.5393	150.84
Vrl 5	-1765	423	-13.15	1.87	145.6724	150.59
Vrl 6	-1766	422	-13.15	1.87	145.6724	149.59
Vrl 7	-1762	422	-13.15	1.87	145.4061	150.09
Vog 0	-362	866	-1.75	4.24	205.0083	-3.24
Vog 1	-362	866	-1.75	4.24	205.0083	-3.24
Vog 2	-362	866	-1.75	4.24	205.0083	-3.24
Vog 3	-362	866	-1.75	4.24	205.0083	-3.24
Vog 4	-361	867	-1.75	4.24	205.0083	-2.24
Vog 5	-362	866	-1.75	4.24	205.0083	-3.24
Vog 6	-361	867	-1.75	4.24	205.0083	-2.24
Vog 7	-362	866	-1.75	4.24	205.0083	-3.24
Vdd 0	-1743	574	-21.91	3.11	92.6059	286.00
Vdd 1	-1747	574	-21.89	3.11	92.8400	285.27
Vdd 2	-1746	575	-21.93	3.11	92.6917	286.73
Vdd 3	-1752	574	-21.99	3.12	92.6324	284.99
Vdd 4	-1744	574	-21.91	3.11	92.6459	285.87
Vdd 5	-1743	574	-21.93	3.11	92.5319	286.23
Vdd 6	-1751	575	-22.01	3.12	92.5587	286.22
Vdd 7	-1737	574	-21.86	3.10	92.5881	286.98

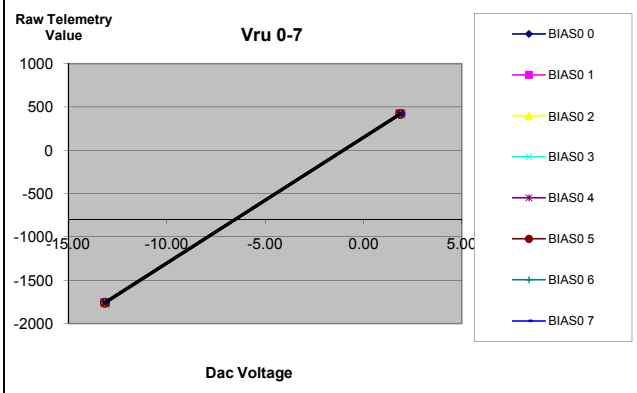
AVERAGE

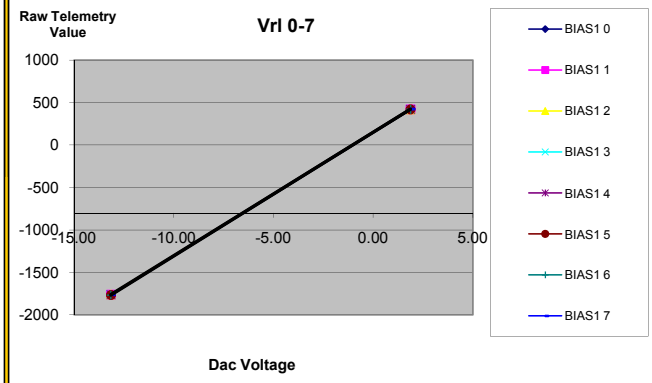
Vru	Slope		Offset
Mean	145.21	Mean	150.46
Stdev	0.1372538	Stdev	0.2566647

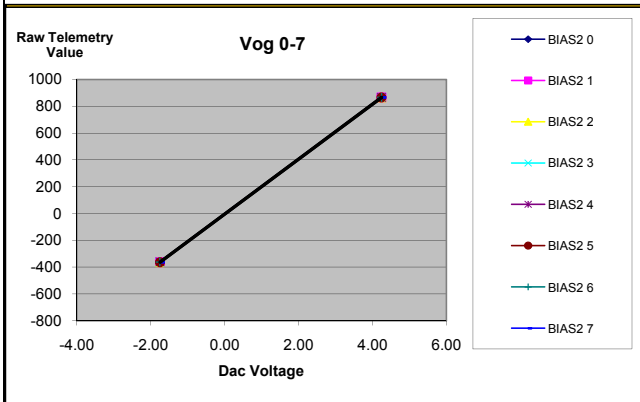
Vrl	Slope		Offset
Mean	145.45	Mean	150.39
Stdev	0.1727741	Stdev	0.3848623

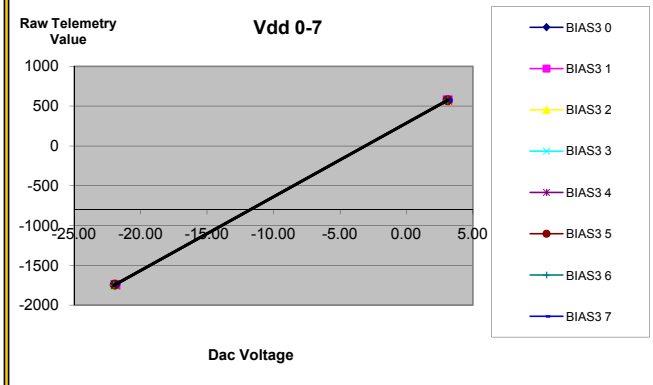
Vog	Slope		Offset
Mean	205.01	Mean	-2.99
Stdev	2.842E-14	Stdev	0.4330127

Vdd	Slope		Offset
Mean	92.64	Mean	286.03
Stdev	0.0900146	Stdev	0.6278518









Stage 8C. Bias Voltage output enables testing - Table 8

Place a line through Bias Voltage name if enable/disable switch works

Vru 0	Vru 1	Vru 2	Vru 3	Vru 4	Vru 5
Vrl 0	Vrl 1	Vrl 2	Vrl 3	Vrl 4	Vrl 5
Vog 0	Vog 1	Vog 2	Vog 3	Vog 4	Vog 5
Vdd 0	Vdd 1	Vdd 2	Vdd 3	Vdd 4	Vdd 5

Stage 9. Vsub and Heater Control testing - Table 9

DAC Value	Vsub Measured Voltage Test Data 10%	50%	90%
Signal	volts	volts	volts
Vsub - rate	-1.24	3.77	8.79
Vsub - Limit	-1.24	3.77	8.79
Vsub0	0.00	0.00	0.00
	Vsub Enable Bit - pass		

DAC Value	Telemetery Readback Test Data 10%	50%	90%
Signal	dec	dec	dec
Vbias 0	153	216	466
Vbias 1	-29	696	1422
RTD1	220	NA	NA
RTD2	248	NA	NA
RTD3	275	NA	NA
RTD4	301	NA	NA
RTD5	325	NA	NA
RTD6	352	NA	NA
Reference 4096	837	NA	NA
eference buffere	837	NA	NA

Stage 10. Video Offset DAC Tests - Table 10.

	DAC Value 410				DAC Value 2048				DAC Value 3686			
ADC	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU	DC Volts	RMS Noise	Rise Time	ADU
0	0.250	NA	NA	17087	1.250		NA	81121	2.250	NA	500ms	145151
1	0.250	NA	NA	16997	1.250		NA	81062	2.250	NA	500ms	145127
2	0.250	NA	NA	16939	1.250		NA	81057	2.250	NA	500ms	145176
3	0.250	NA	NA	16963	1.250		NA	81041	2.250	NA	500ms	145122
4	0.250	NA	NA	16954	1.250		NA	81056	2.250	NA	500ms	145149
5	0.250	NA	NA	17110	1.250		NA	81183	2.250	NA	500ms	145264
6	0.250	NA	NA	16892	1.250		NA	80987	2.250	NA	500ms	145079
7	0.250	NA	NA	17123	1.250		NA	81164	2.250	NA	500ms	145201
8	0.250	NA	NA	17121	1.250		NA	81191	2.250	NA	500ms	145263
9	0.250	NA	NA	16963	1.250		NA	81073	2.250	NA	500ms	145184
10	0.250	NA	NA	17200	1.250		NA	81190	2.250	NA	500ms	145182
11	0.250	NA	NA	16963	1.250		NA	81085	2.250	NA	500ms	145212

ADC	DC Volts		Data Set		
Channel	Slope	Offset	410	2048	3686
0	1638.000	0.500	0.250	1.250	2.250
1	1638.000	0.500	0.250	1.250	2.250
2	1638.000	0.500	0.250	1.250	2.250
3	1638.000	0.500	0.250	1.250	2.250
4	1638.000	0.500	0.250	1.250	2.250
5	1638.000	0.500	0.250	1.250	2.250
6	1638.000	0.500	0.250	1.250	2.250
7	1638.000	0.500	0.250	1.250	2.250
8	1638.000	0.500	0.250	1.250	2.250
9	1638.000	0.500	0.250	1.250	2.250
10	1638.000	0.500	0.250	1.250	2.250
11	1638.000	0.500	0.250	1.250	2.250

(dac# -offset)/slope=Voltage

ADC	ADU's		Data Set		
Channel	Slope	Offset	410	2048	3686
0	0.026	-27.12	17087	81121	145151
1	0.026	-24.58	16997	81062	145127
2	0.026	-22.73	16939	81057	145176
3	0.026	-23.60	16963	81041	145122
4	0.026	-23.29	16954	81056	145149
5	0.026	-27.35	17110	81183	145264
6	0.026	-21.71	16892	80987	145079
7	0.026	-27.99	17123	81164	145201
8	0.026	-27.70	17121	81191	145263
9	0.026	-23.39	16963	81073	145184
10	0.026	-30.27	17200	81190	145182
11	0.026	-23.28	16963	81085	145212

(dac# -offset)/slope=ADU

Notes and Observations

Checked for oscillations using a Agilent Oscilloscope on AC. OK

Stage 11. CDS Control Functions and Video Channel Performanc

TEST #1: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit is held static. The purpose of this test is to verify the correct operation of the ADC devices and measure the noise of the Offset voltage generators, ADC buffer amplifiers and ADC devices

Noise Test 1

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	81116	81131	81122.9	2.12221
CH 1	81055	81073	81063.7	2.36419
CH 2	81054	81069	81061.7	2.31293
CH 3	81039	81057	81047.6	2.35459
CH 4	81046	81063	81054.4	2.29193
CH 5	81178	81195	81187.5	2.07507
CH 6	80977	80994	80985.6	2.31308
CH 7	81158	81174	81166.7	2.38226
CH 8	81185	81202	81193.8	2.2451
CH 9	81067	81084	81075.4	2.28502
CH 10	81184	81200	81192.2	2.3202
CH 11	81084	81099	81091.8	2.18615

TEST #2: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the invert/non-invert and the DC Restore switches are held static.

Noise Test 2

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76220	76244	76233.8	2.79084
CH 1	76727	76747	76736.3	2.8986
CH 2	76351	76372	76360.7	2.78618
CH 3	76631	76652	76642.3	2.75634
CH 4	76354	76376	76363.4	2.75925
CH 5	76912	76932	76921.5	2.86551
CH 6	76539	76558	76549	2.83486
CH 7	76971	76991	76980.5	2.70184
CH 8	76702	76723	76711.9	2.77071
CH 9	76835	76858	76846.5	2.81526
CH 10	76551	76572	76561.3	2.8536
CH 11	76874	76892	76882	2.6911

TEST #3: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition while the DC Restore switch is held static.

Noise Test 3

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76218	76239	76229.4	3.0435
CH 1	76720	76744	76732.7	3.05702
CH 2	76348	76369	76357.8	3.00863
CH 3	76621	76643	76631.4	2.97071
CH 4	76353	76377	76363.1	3.03615
CH 5	76904	76927	76915.8	3.02449
CH 6	76530	76553	76542.6	3.06243
CH 7	76967	76989	76977.8	2.91569
CH 8	76699	76721	76709.5	2.90936
CH 9	76824	76845	76835.5	2.80604
CH 10	76553	76575	76563	3.01775
CH 11	76869	76891	76879	3.00149

TEST #4: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition.

Noise Test 4

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76212	76233	76222.6	3.20735
CH 1	76724	76748	76736.3	3.17577
CH 2	76351	76373	76362.4	3.1882
CH 3	76620	76642	76631.2	3.07451
CH 4	76392	76414	76402	3.08304
CH 5	76895	76916	76905.8	3.15116
CH 6	76537	76559	76548.4	3.23263
CH 7	76936	76959	76947.9	2.98126
CH 8	76738	76764	76750.9	3.10746
CH 9	76744	76770	76757.2	3.29509
CH 10	76572	76596	76582.4	3.07754
CH 11	76832	76854	76840.8	3.15296

TEST #5: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the circuitry set to high GAIN.

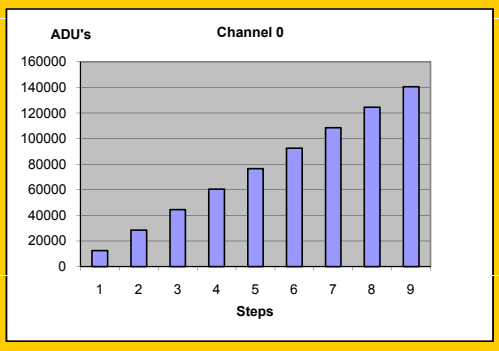
Noise Test 5

	Min Pix Value	Max Pix	Mean Pix	Std. Dev.
CH 0	76218	76249	76233	3.66493
CH 1	76735	76763	76748.2	3.69374
CH 2	76367	76393	76379.8	3.63438
CH 3	76627	76653	76639.2	3.66998
CH 4	76395	76420	76407.2	3.64534
CH 5	76892	76917	76904.1	3.64513
CH 6	76537	76565	76550.1	3.75713
CH 7	76936	76965	76950.2	3.61956
CH 8	76790	76814	76801.9	3.60559
CH 9	76743	76771	76756.7	3.79244
CH 10	76628	76655	76642.3	3.67513
CH 11	76828	76854	76840.1	3.58798

TEST #6A: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

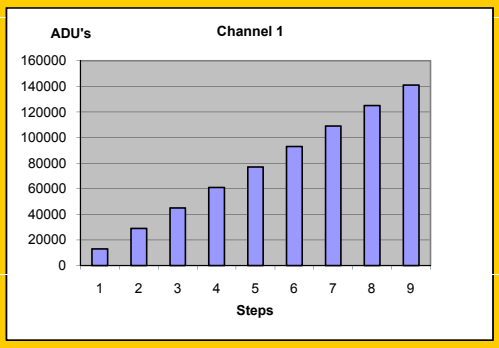
BrdTst6_006 / Channel 0					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12484	12507	12495.5	3.16673	10%
0x333	28475	28496	28485.1	3.20573	20%
0x4cc	44459	44481	44469.7	3.17461	30%
0x666	60486	60510	60498.5	2.99633	40%
0x800	76510	76536	76522.5	3.24111	50%
0x999	92498	92524	92512	3.21104	60%
0xb33	108530	108552	108541	3.09573	70%
0xccc	124517	124542	124530	3.04262	80%
0xe66	140549	140571	140560	3.20392	90%



TEST #6B: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

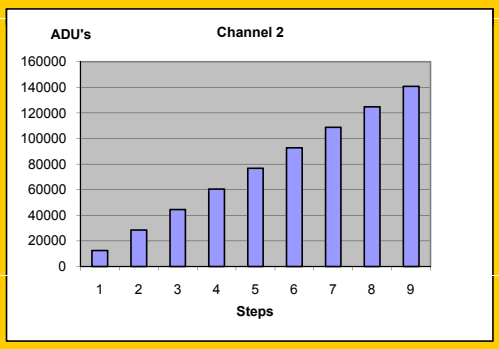
BrdTst6_006 / Channel 1					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12904	12925	12914.2	3.16319	10%
0x333	28899	28922	28910	3.12874	20%
0x4cc	44895	44920	44907.6	3.16692	30%
0x666	60930	60955	60942	3.15663	40%
0x800	76963	76986	76974.6	3.13216	50%
0x999	92959	92981	92970.6	3.16455	60%
0xb33	108994	109017	109006	3.146	70%
0xccc	124995	125018	125006	3.16662	80%
0xe66	141027	141052	141040	3.17971	90%



TEST #6C: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

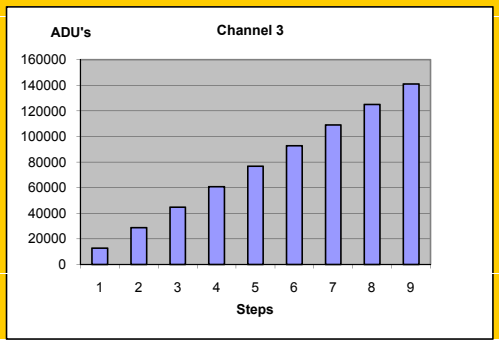
BrdTst6_006 / Channel 2					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12530	12552	12539.7	3.17548	10%
0x333	28539	28565	28551.6	3.2462	20%
0x4cc	44549	44572	44560.4	3.09104	30%
0x666	60597	60622	60610.6	3.11485	40%
0x800	76643	76667	76655.1	3.14621	50%
0x999	92651	92675	92664.1	3.16568	60%
0xb33	108703	108728	108714	3.16103	70%
0xccc	124714	124737	124726	3.28527	80%
0xe66	140764	140789	140777	3.19771	90%



TEST #6D: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

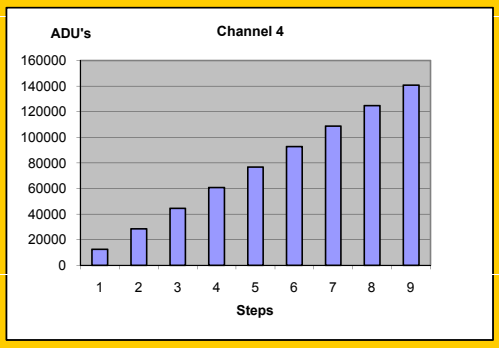
BrdTst6_006 / Channel 3					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12786	12808	12797.6	3.24327	10%
0x333	28785	28806	28796.6	3.17902	20%
0x4cc	44786	44810	44798.8	3.16864	30%
0x666	60825	60846	60835.6	3.04346	40%
0x800	76861	76886	76874.5	3.17275	50%
0x999	92864	92886	92874.9	3.12949	60%
0xb33	108901	108924	108912	3.1386	70%
0xccc	124906	124930	124917	3.27428	80%
0xe66	140942	140967	140955	3.16339	90%



TEST #6E: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

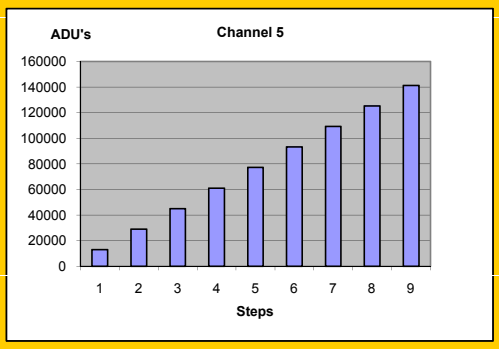
BrdTst6_006 / Channel 4					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12594	12616	12605.8	3.15448	10%
0x333	28600	28621	28610.8	2.98644	20%
0x4cc	44600	44624	44610.8	3.12892	30%
0x666	60645	60667	60656.4	3.04839	40%
0x800	76688	76708	76698.5	3.14705	50%
0x999	92690	92718	92703.1	3.01102	60%
0xb33	108736	108758	108748	3.11311	70%
0xccc	124738	124764	124751	3.19183	80%
0xe66	140787	140808	140797	3.12272	90%



TEST #6F: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

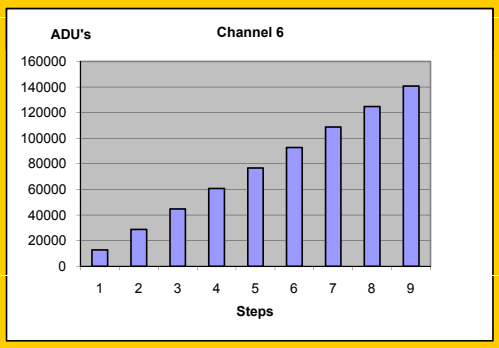
BrdTst6_006 / Channel 5					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13073	13098	13083.5	3.21513	10%
0x333	29070	29092	29081	3.13796	20%
0x4cc	45068	45092	45080.1	3.1419	30%
0x666	61105	61128	61117	3.17497	40%
0x800	77141	77165	77154.2	3.22116	50%
0x999	93143	93166	93156	3.02716	60%
0xb33	109181	109207	109194	3.24505	70%
0xccc	125184	125206	125196	3.1826	80%
0xe66	141222	141245	141234	3.13971	90%



TEST #6G: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

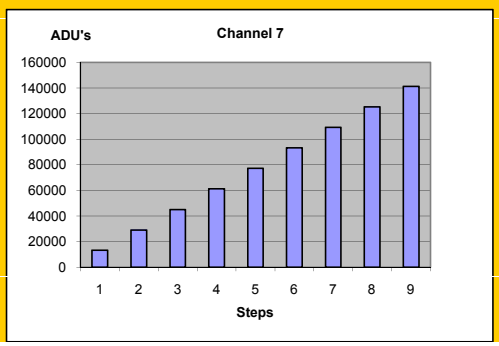
BrdTst6_006 / Channel 6					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12692	12715	12703	3.14324	10%
0x333	28696	28719	28707.5	2.98268	20%
0x4cc	44696	44719	44708.8	3.08059	30%
0x666	60741	60765	60752.7	3.21784	40%
0x800	76778	76803	76791.2	3.11198	50%
0x999	92781	92804	92793.8	3.17004	60%
0xb33	108826	108849	108838	3.06543	70%
0xccc	124831	124852	124842	3.13725	80%
0xe66	140874	140897	140886	3.20452	90%



TEST #6H: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

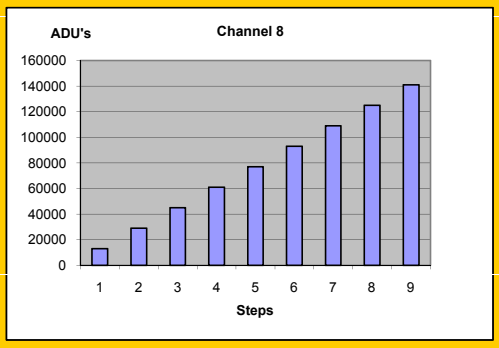
BrdTst6_006 / Channel 7					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	13131	13153	13140.9	3.06754	10%
0x333	29121	29145	29131.3	3.16005	20%
0x4cc	45112	45136	45122.6	3.04127	30%
0x666	61138	61160	61149.9	3.24073	40%
0x800	77166	77188	77177.2	3.17338	50%
0x999	93157	93182	93169.2	3.11913	60%
0xb33	109187	109211	109198	3.19206	70%
0xccc	125179	125203	125191	3.13319	80%
0xe66	141208	141232	141220	3.18094	90%



TEST #6I: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

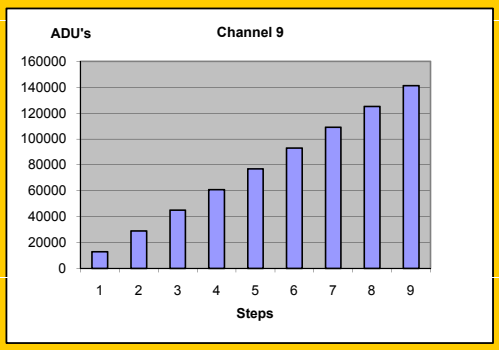
BrdTst6_006 / Channel 8					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12949	12970	12959.5	2.90336	10%
0x333	28948	28972	28959.4	3.13823	20%
0x4cc	44945	44966	44955.4	3.11816	30%
0x666	60984	61006	60994.4	2.96171	40%
0x800	77015	77039	77026.8	3.0797	50%
0x999	93013	93034	93023.6	3.06946	60%
0xb33	109050	109074	109062	2.98312	70%
0xccc	125051	125073	125061	3.00101	80%
0xe66	141089	141113	141101	3.17155	90%



TEST #6J: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

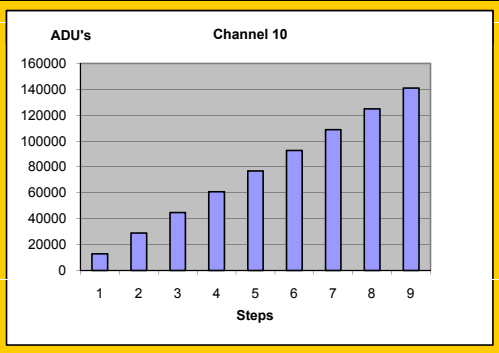
BrdTst6_006 / Channel 9					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12892	12916	12903.9	3.21444	10%
0x333	28902	28924	28914	3.03093	20%
0x4cc	44909	44933	44921.5	3.15918	30%
0x666	60957	60981	60969.5	3.20421	40%
0x800	77002	77025	77013.8	3.17681	50%
0x999	93014	93036	93024.2	3.13871	60%
0xb33	109064	109085	109074	3.12023	70%
0xccc	125074	125097	125085	3.20751	80%
0xe66	141121	141144	141133	3.18179	90%



TEST #6K: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

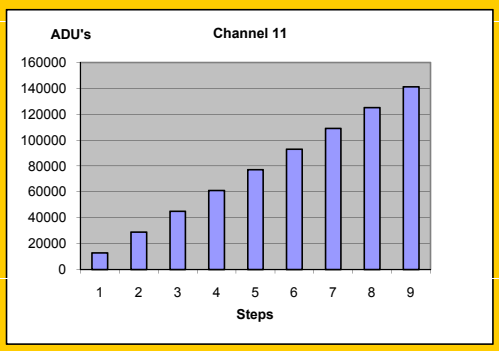
BrdTst6_006 / Channel 10					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12858	12882	12870.4	3.18674	10%
0x333	28841	28862	28850.7	3.17713	20%
0x4cc	44815	44839	44827.6	3.19571	30%
0x666	60836	60859	60847.1	3.16929	40%
0x800	76848	76870	76859	3.17595	50%
0x999	92826	92850	92838.3	3.24315	60%
0xb33	108844	108868	108857	3.25323	70%
0xccc	124826	124850	124838	3.28463	80%
0xe66	140846	140869	140858	3.23934	90%



TEST #6L: ccdBrdTest_Setup01.mod

This setup aquires data from the ADC channels while the CDS circuit performs a nornal acquisition with the ADC Offset Voltage stepped from 10% to 90%.

BrdTst6_006 / Channel 11					
OFFSET DAC VALUE	Min Pix Value	Max Pix Value	Mean Pix Value	Std. Dev.	Remarks
0x19a	12973	12996	12984.8	3.22789	10%
0x333	28985	29012	28997.7	3.25003	20%
0x4cc	44995	45018	45007	3.25681	30%
0x666	61045	61071	61058.2	3.09037	40%
0x800	77093	77116	77104.7	3.21362	50%
0x999	93105	93130	93117.4	3.21695	60%
0xb33	109159	109182	109170	3.31612	70%
0xccc	125170	125194	125182	3.16615	80%
0xe66	141222	141245	141233	3.09844	90%



Stage 13. Other Bit Tests. Table 11

Electronic Serial Number	0xDB6FA9		Board Serial Number	16
Firmware Version	0x193		Name Of Person Testing	S. Holm
Ident Register	0x502		Board passed Functional Tests	YES