

SEE PAGE 2 FOR REVISION BLOCK

CLK & BIAS BOARD  
Bias and FastBias Outputs

CURRENT LIMIT  
RESISTORS

PROTECTION DIODES

Interface Card  
Clock Outputs

CLK & BIAS BOARD  
Clock Outputs

2

2

3

3

4

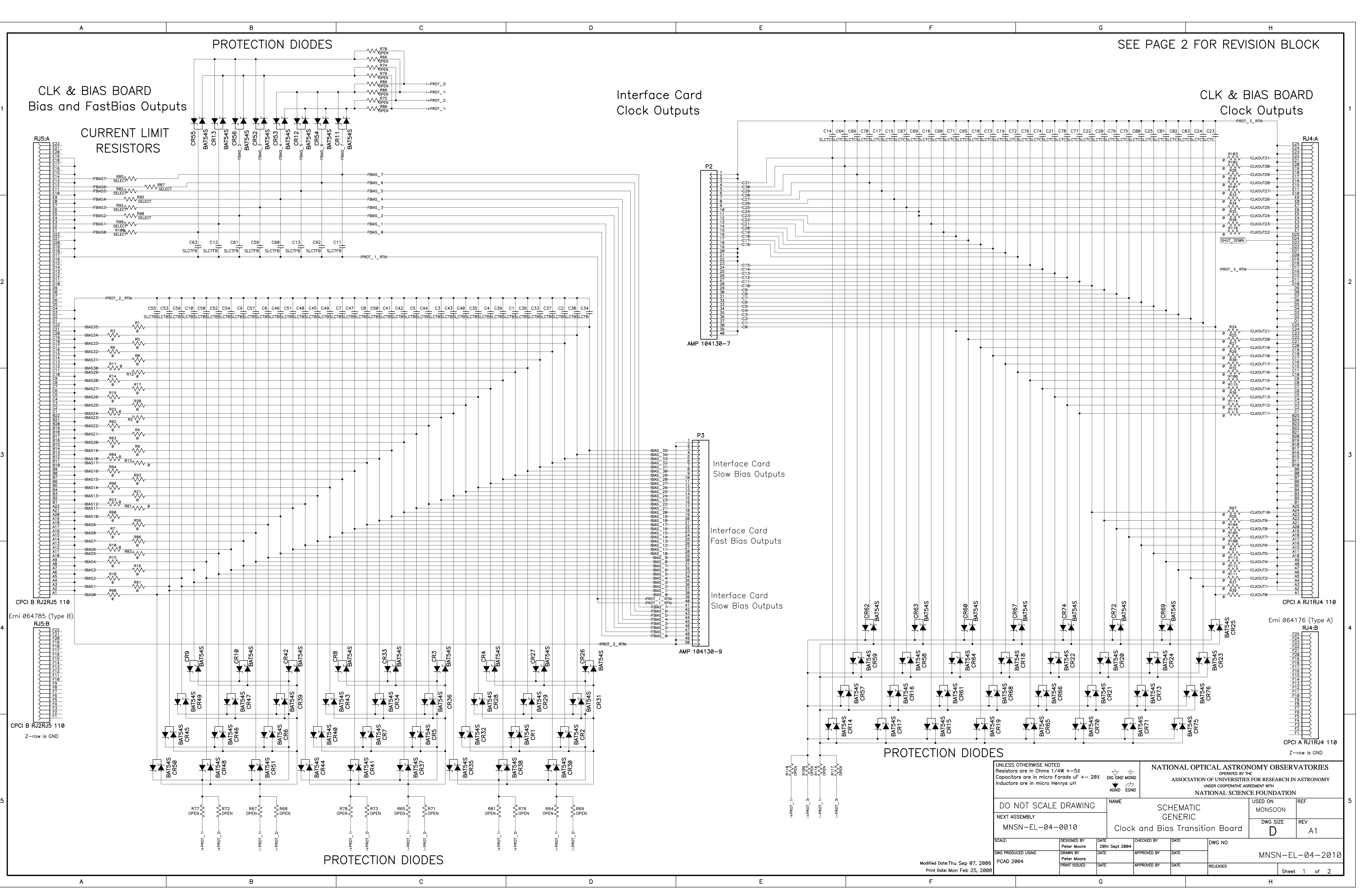
4

5

5

5

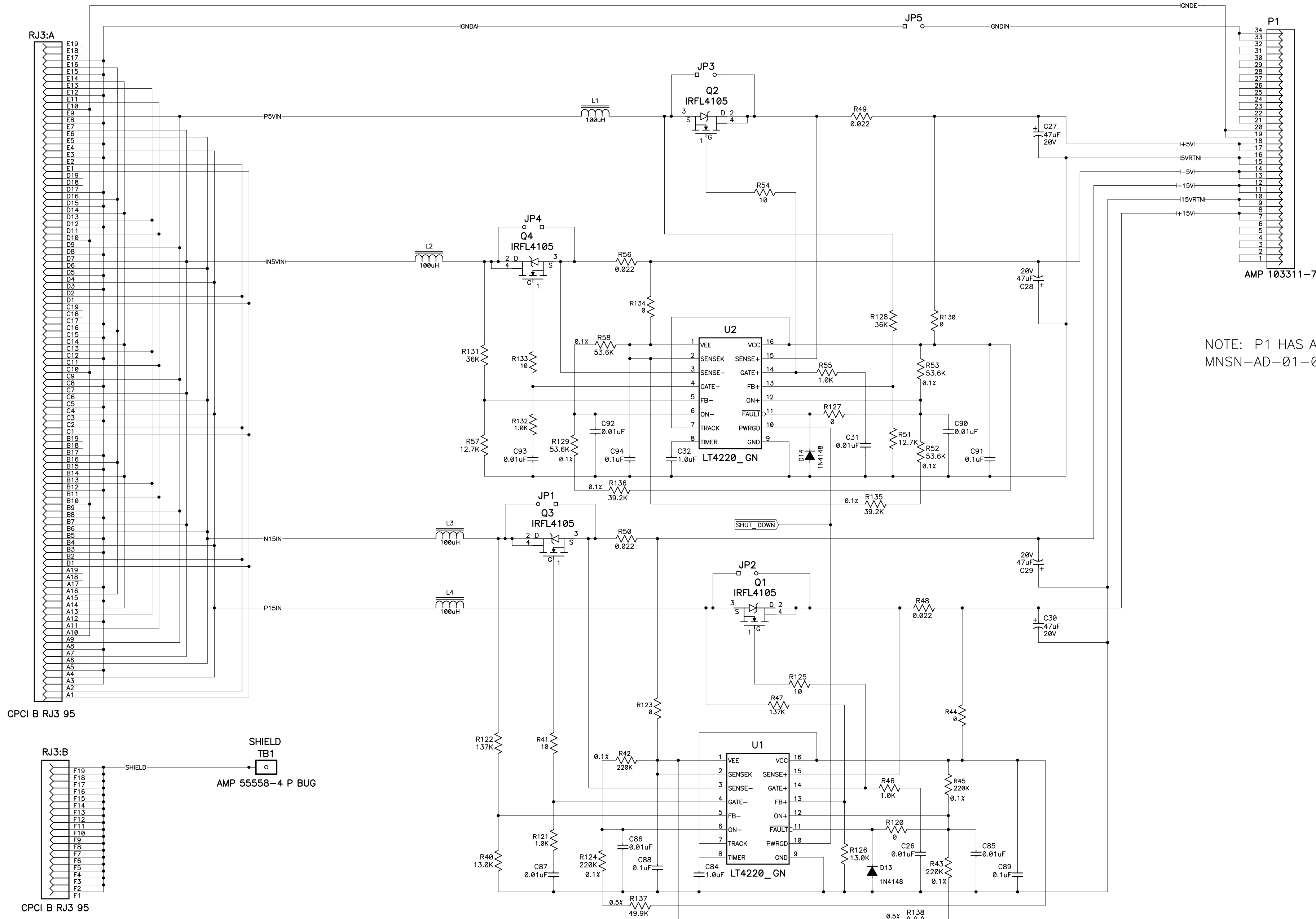
5



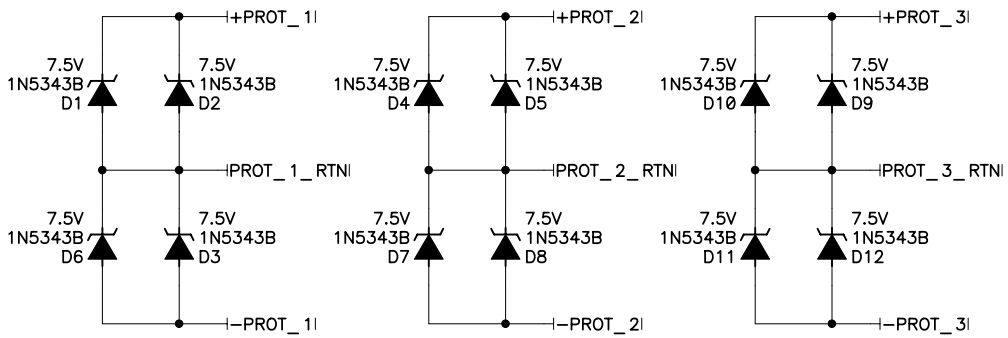
REVISIONS					
LTR	DESCRIPTION	ECR	DATE	BY	APPVD
A	reposition inductors in circuit, change to shield ground connection, add resistors, value changes, cap land pattern change	MNSN-0110	05oct05	dms	p.moore
A1	voltage divider resistor value, spec changes (temp stable) R42,43,45,52,53,58,124,129,135,136,137,138		07SEP06	dms	p.moore

CLK & BIAS BOARD  
Power Connector

Interface Card  
Power Input



NOTE: P1 HAS A POSITIONAL RESTRICTION SEE DRAWING  
MNSN-AD-01-0010 FOR PCB CARD DIMENSIONS



PROTECTION CLAMPS

Supplies are +/- 5% over / under protected.  
Current limit set for 2.1 amps during normal operation  
and 680 ma during start up cycle.

NATIONAL OPTICAL ASTRONOMY OBSERVATORIES			
NAME SCHEMATIC GENERIC Clock and Bias Transition Board			
DWG NO	SIZE	REF	REV
MNSN-EL-04-2010	D		A1
RELEASED		Sheet 2 of 2	

Modified Date: Thu Sep 07, 2006  
Print Date: Mon Feb 25, 2008