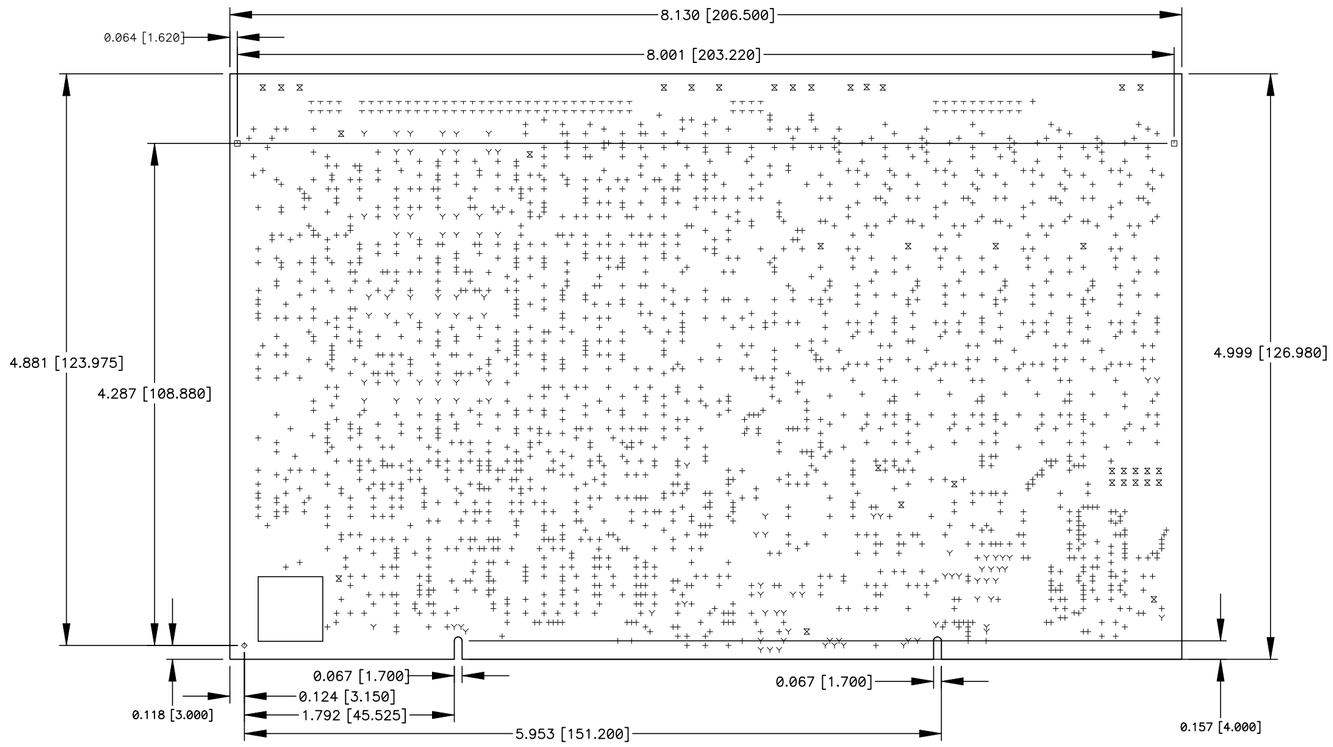
REVISIONS						
ZONE	LTR	DESCRIPTION	ECR	DATE	BY	APRV
	OD	INITIAL RELEASE		JUL 2009	DMS	M.HUNTEN
	A	Major revision, see ECO for details	TRNT–007 TRNT–009	Jun 03, 2010	DMS	M.HUNTEN
	B	Major revision, see ECO for details	TRNT–019	May 09, 2011	DMS	M.HUNTEN
	C	fix cds state connection on U117, optimize for performance See ECO for details	TRNT–025	Oct 12, 2011	DMS	pmoore



Drill Table			
Hole Dia (inch)	Symbol	Quantity	Plated
0.012	+	2004	Yes
0.020	Y	104	Yes
0.032	⊤	96	Yes
0.041	⧖	36	Yes
0.089	⊡	2	No
0.125	◈	1	No

APPROVED FOR CONSTRUCTION 10–20–11 DMS

NOTES: unless otherwise specified

1.0 Fabricate circuit board to conform to IPC–A–600
Applicable documents
The following items are required:
PATTERN FILM / GERBER DATA DWG # TRNT–EL–04–3004
DETAIL DRAWING DWG # TRNT–EL–04–1004 THIS DOCUMENT

1.1 Artwork may not be modified except for process control.

2.0 BASE MATERIAL
2.1 Laminate base material shall be natural color, FR–370 or equivalent. See Detail A–A for layer to layer specification and overall thickness.
2.2 B–Stage shall be selected at vendors discretion to meet over all board thickness and end item requirements.

3.0 COPPER PLATING
3.1 Copper plating shall have a minimum purity of 99.5 percent and a minimum thickness of .001 inch. This also applies to the plating in the holes.

4.0 SOLDERMASK
4.1 Apply LPI GREEN soldermask over bare copper according to the soldermask pattern file per IPC–SM–840. Apply solder mask to layers 1 and 10 using appropriate artwork masters, registration of solder mask IAW IPC–A–600. Current mask clearance is .0025" annular ring. Vendor may resize solder mask openings for minimal (.001–.003 solder mask to pad clearance to accommodate manufacturing processes.

5.0 FINISH
5.1 EXPOSED COPPER SHALL BE Ni/Au –– IMMERSION GOLD 3–5u INCH (0.000003–0.000005) OVER ELECTROLESS NICKEL 100–200u INCH (0.00001–0.00002) THICK IAW IPC–2221 AND IPC–4552 (ENIG).

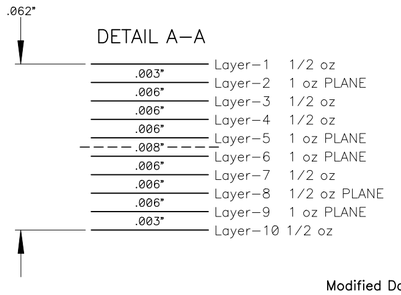
6.0 SILK SCREEN
6.1 Silk screen top (–1) and bottom (–10) side of board using white epoxy ink according to the –1S pattern film and the –10S pattern film. Ink shall not cover any exposed metal.

7.0 DIMENSIONS
7.1 All dimensions are in inches.
7.2 Unless otherwise specified all hole sizes apply after plating. Hole sizes are shown in the drill schedule.

8.0 TOLERANCES
8.1 Hole size tolerance +– .003 after plating unless otherwise specified.
8.2 Conductor widths and spacing shall be within 20% of the artwork originals.
8.3 Layer to layer registration shall be .007 inches of true position
8.4 Board dimensions shall meet the requirements of the board drawing.
8.5 Warp and twist shall not exceed that defined in IPC–A–600.

9.0 APPEARANCE
9.1 All inside and outside corners shall have a maximum radius of .065
9.2 Remove all burrs and smooth sharp edges to .010 max.

VENDOR NOTE: NOTIFY US OF ANY CONFLICTING REQUIREMENTS OR IF BOARDS CANNOT BE MANUFACTURED TO MEET THE ABOVE REQUIREMENTS, DUE TO VENDORS PROCESS AND/OR TECHNIQUES OR BECAUSE PHOTO TOOLS AND/OR SPECIFICATIONS ARE INADEQUATE.



Modified Date: Thu Oct 20, 2011
Print Date: Thu Oct 20, 2011

QTY REQ'D	PART OR IDENTIFYING NO	ITEM DESCRIPTION		ITEM NO

TOLERANCES UNLESS OTHERWISE NOTED
.XX ± .03
.XXX ± .010
ANGULAR ±.5°
THIRD ANGLE PROJECTION

NATIONAL OPTICAL ASTRONOMY OBSERVATORIES
OPERATED BY THE
ASSOCIATION OF UNIVERSITIES FOR RESEARCH IN ASTRONOMY
UNDER COOPERATIVE AGREEMENT WITH
NATIONAL SCIENCE FOUNDATION

DO NOT SCALE DRAWING

NEXT ASSEMBLY: TRNT–EL–04–0004

REFER TO SCHEMATIC: TRNT–EL–04–2004

NAME: DETAIL
TORRENT Analog Front End CCD
AFE CCD

USED ON: TORRENT
REF: NA
DWG SIZE: C
REV: C

SCALE:	DESIGNED BY	DATE	CHECKED BY	DATE	DWG NO
FULL	M.Hunten	28JUL08			TRNT–EL–04–1004
DWG PRODUCED USING: PCAD 2006	DRAWN BY: Dee Stover	DATE: 09JUN09	APPROVED BY	DATE	RELEASED

SHEET 1 OF 1