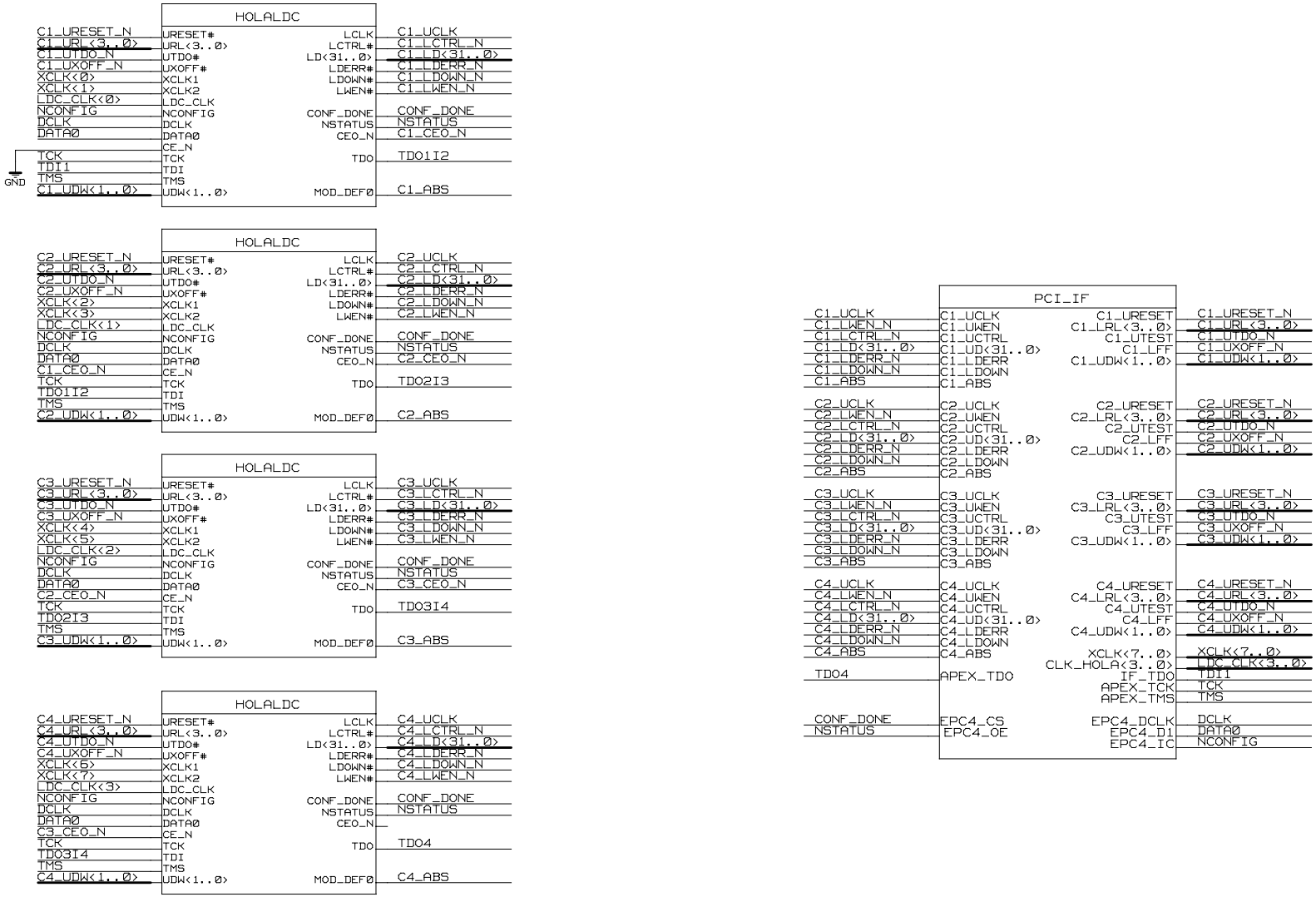
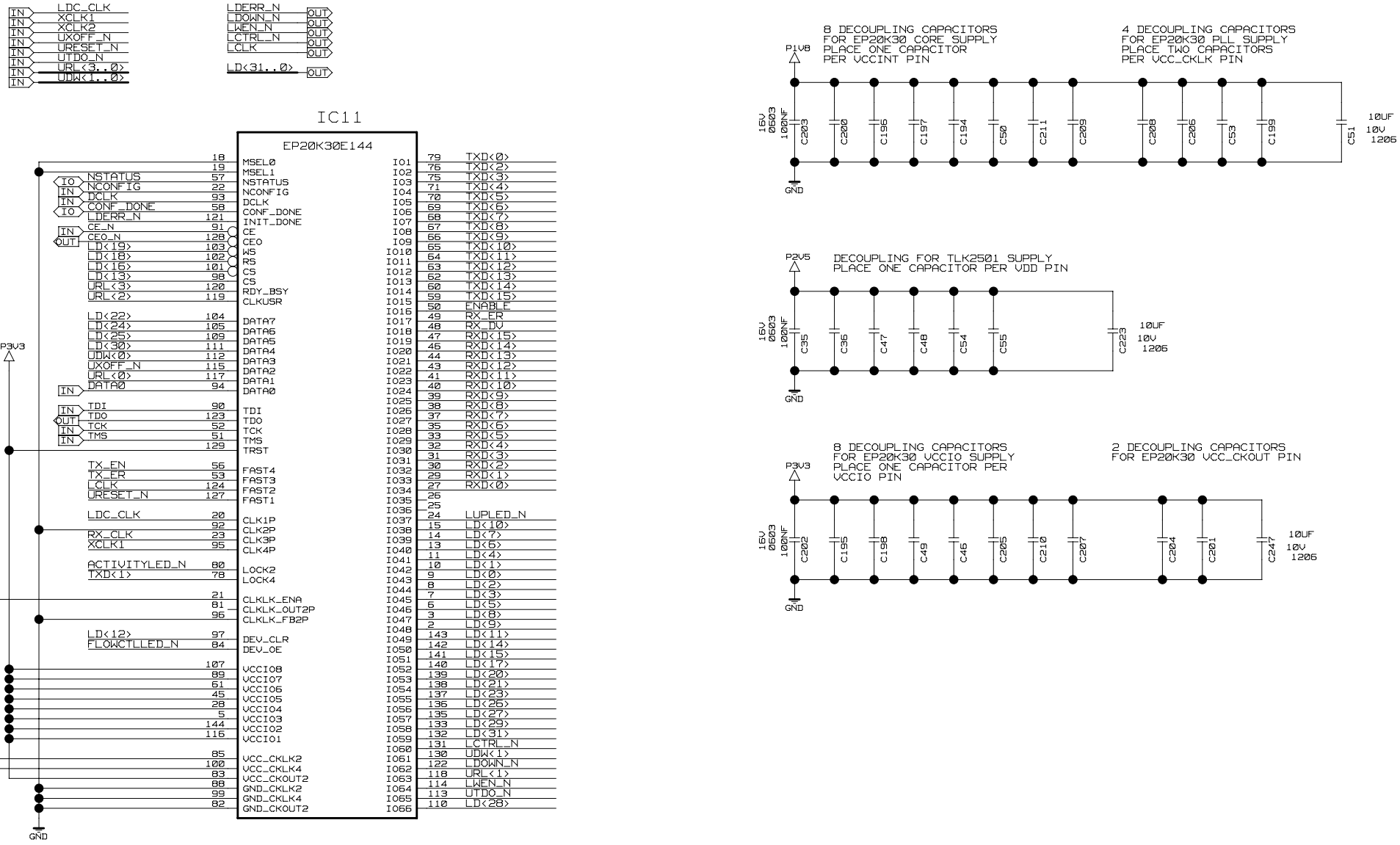


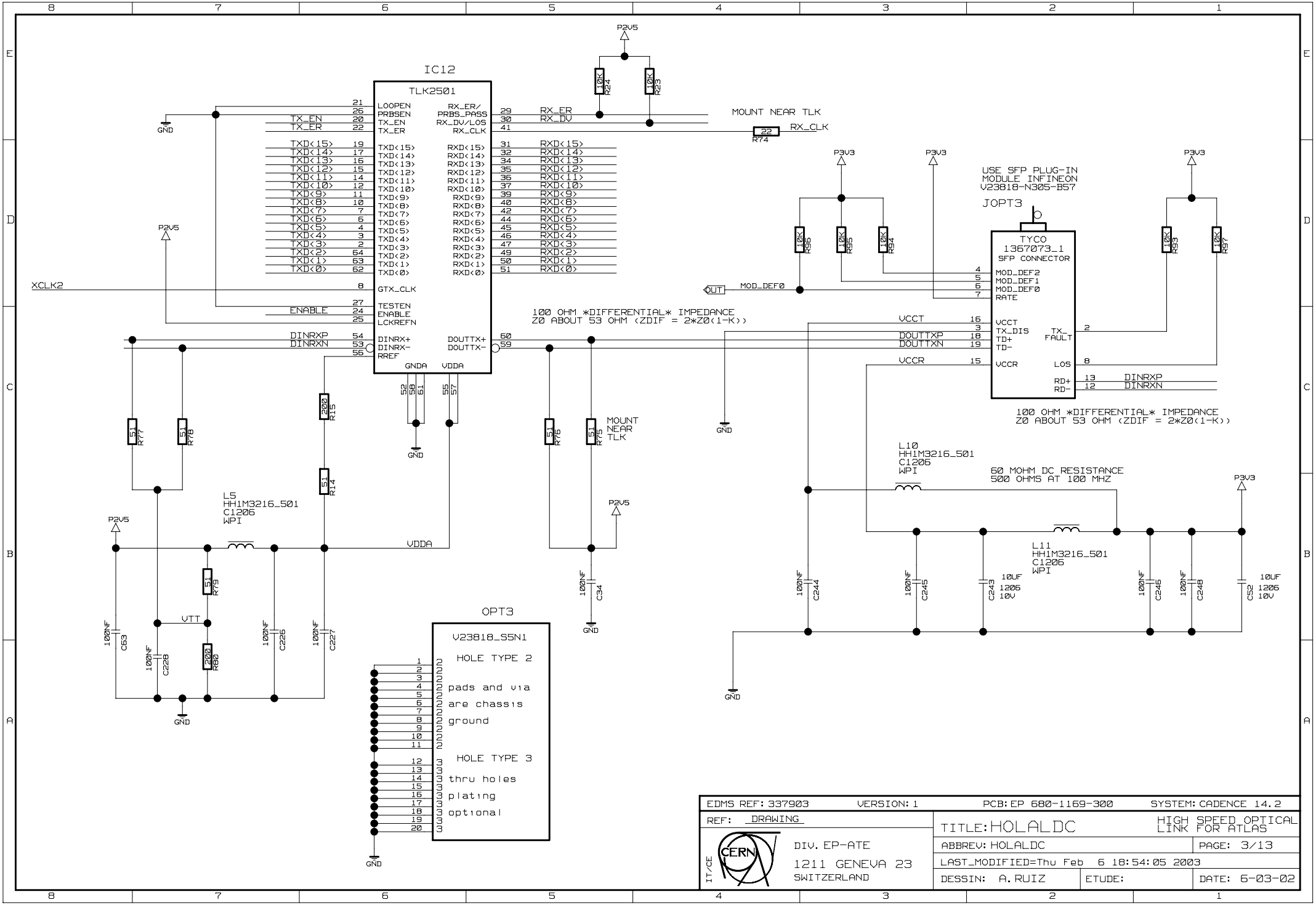
NOTES: PUT THE FOLLOWING TEXT ON PCB:
"THIS DESIGN CONTAINS INFORMATION CREATED AND MADE AVAILABLE AT CERN"

ALL RESISTORS 0603 PACKAGE
100NF CAPACITORS 0603 PACKAGE
10 UF CAPACITORS 1206 PACKAGE

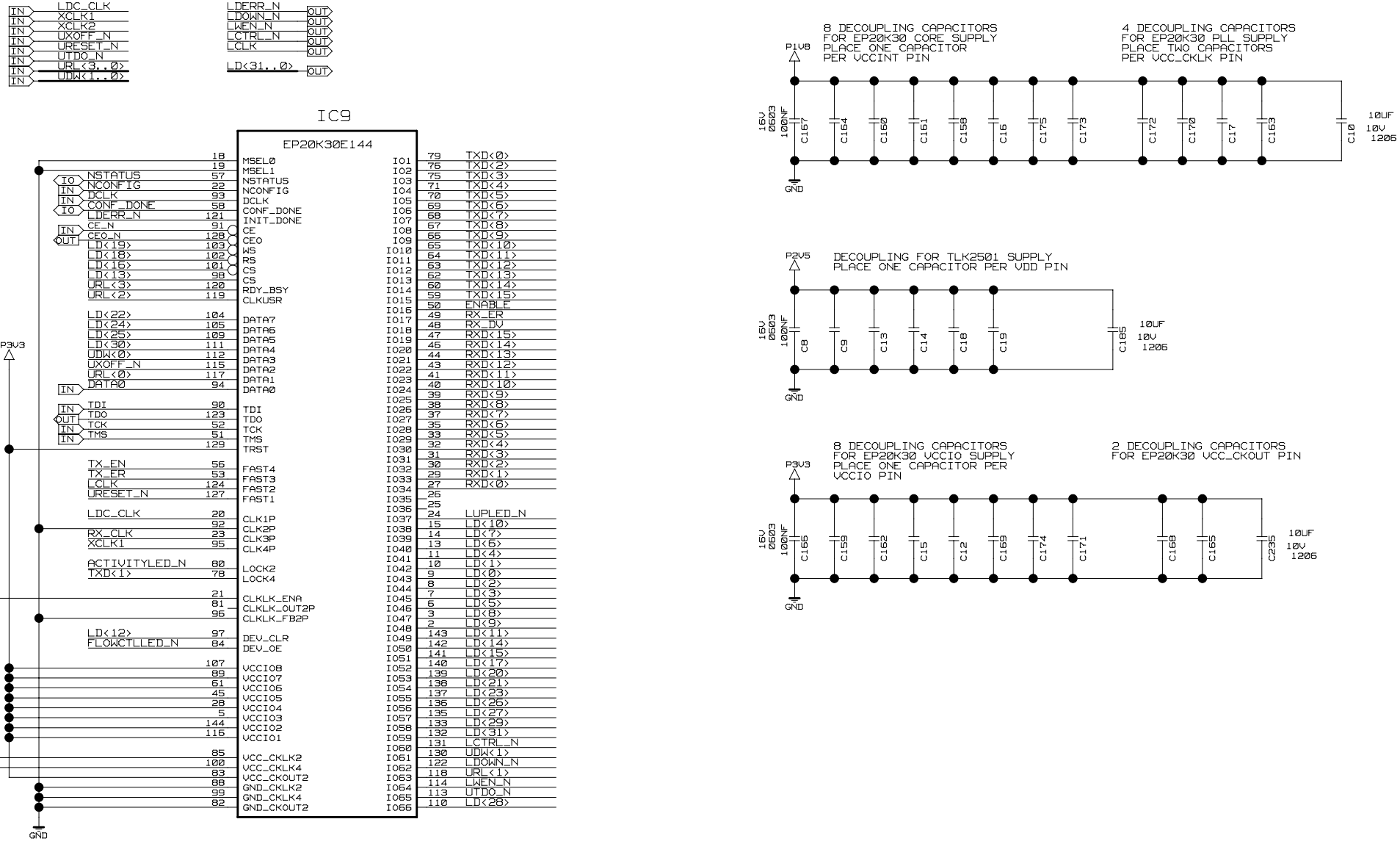
EDMS REF: 337903	VERSION: 1	PCB: EP 680-1169-300	SYSTEM: CADENCE 14.2
REF: DRAWING		TITLE: FILAR	
IT/CE CERN DIV. EP-ATE 1211 GENEVA 23 SWITZERLAND		ABBREV: FILAR	PAGE: 1/13
		LAST_MODIFIED=Thu Feb 6 18:53:28 2003	
		DESSIN: IWANSKI/HAAS ETUDE:	DATE: 23/11/02



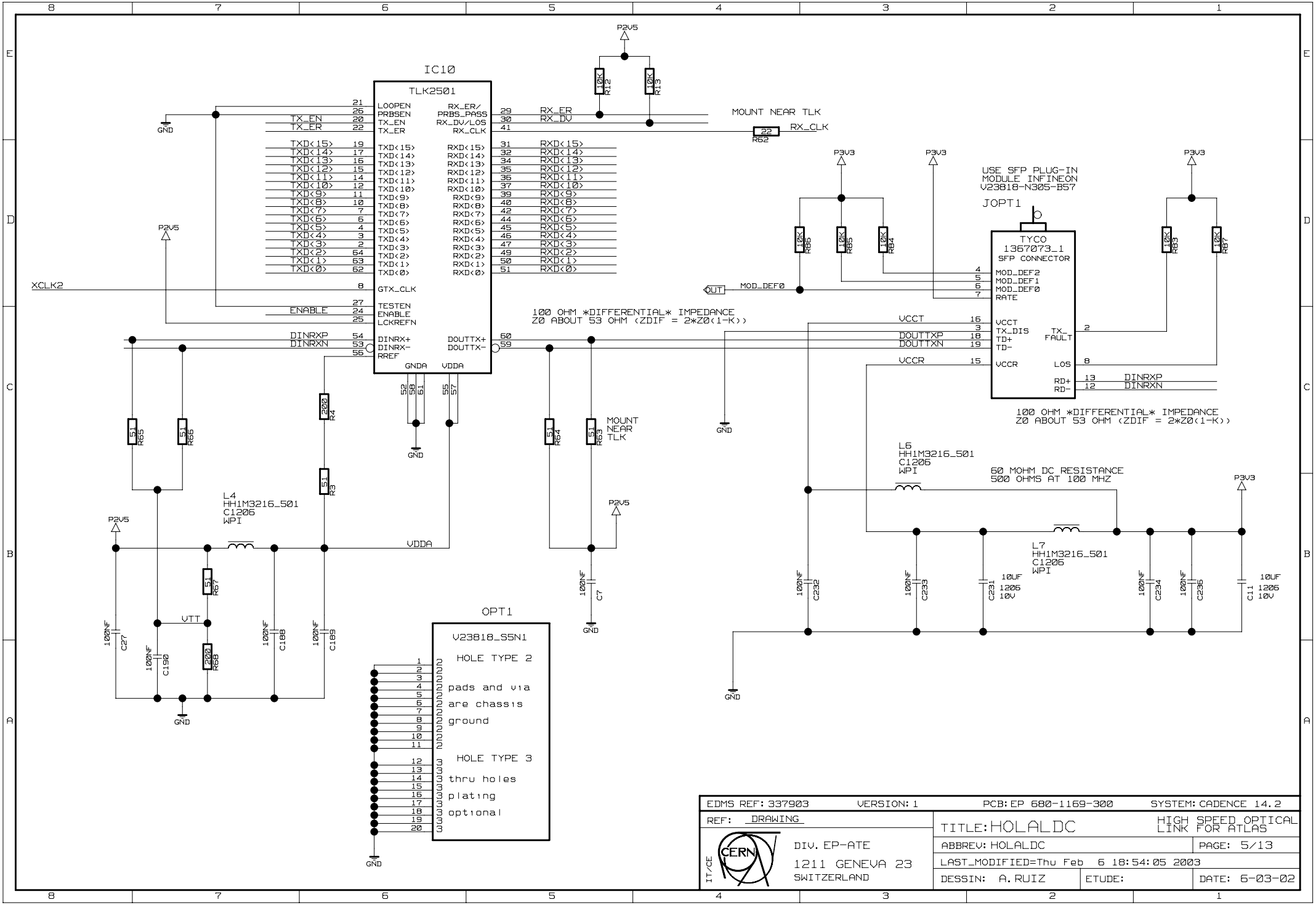
EDMS REF: 337903	VERSION: 1	PCB: EP 680-1169-300	SYSTEM: CADENCE 14.2
REF: DRAWING		TITLE: HOLALDC	HIGH-SPEED OPTICAL LINK FOR ATLAS
IT/CE CERN DIV. EP-ATE 1211 GENEVA 23 SWITZERLAND		ABBREV: HOLALDC	PAGE: 2/13
		LAST_MODIFIED=Thu Feb 6 18:54:02 2003	
		DESSIN: A. RUIZ ETUDE:	DATE: 6-03-02



EDMS REF: 337903	VERSION: 1	PCB: EP 680-1169-300	SYSTEM: CADENCE 14.2
REF: DRAWING		TITLE: HOLALDC	HIGH SPEED OPTICAL LINK FOR ATLAS
CERN IT/CE DIV. EP-ATE 1211 GENEVA 23 SWITZERLAND		ABBREV: HOLALDC	PAGE: 3/13
		LAST_MODIFIED=Thu Feb 6 18:54:05 2003	
		DESSIN: A. RUIZ	ETUDE: DATE: 6-03-02

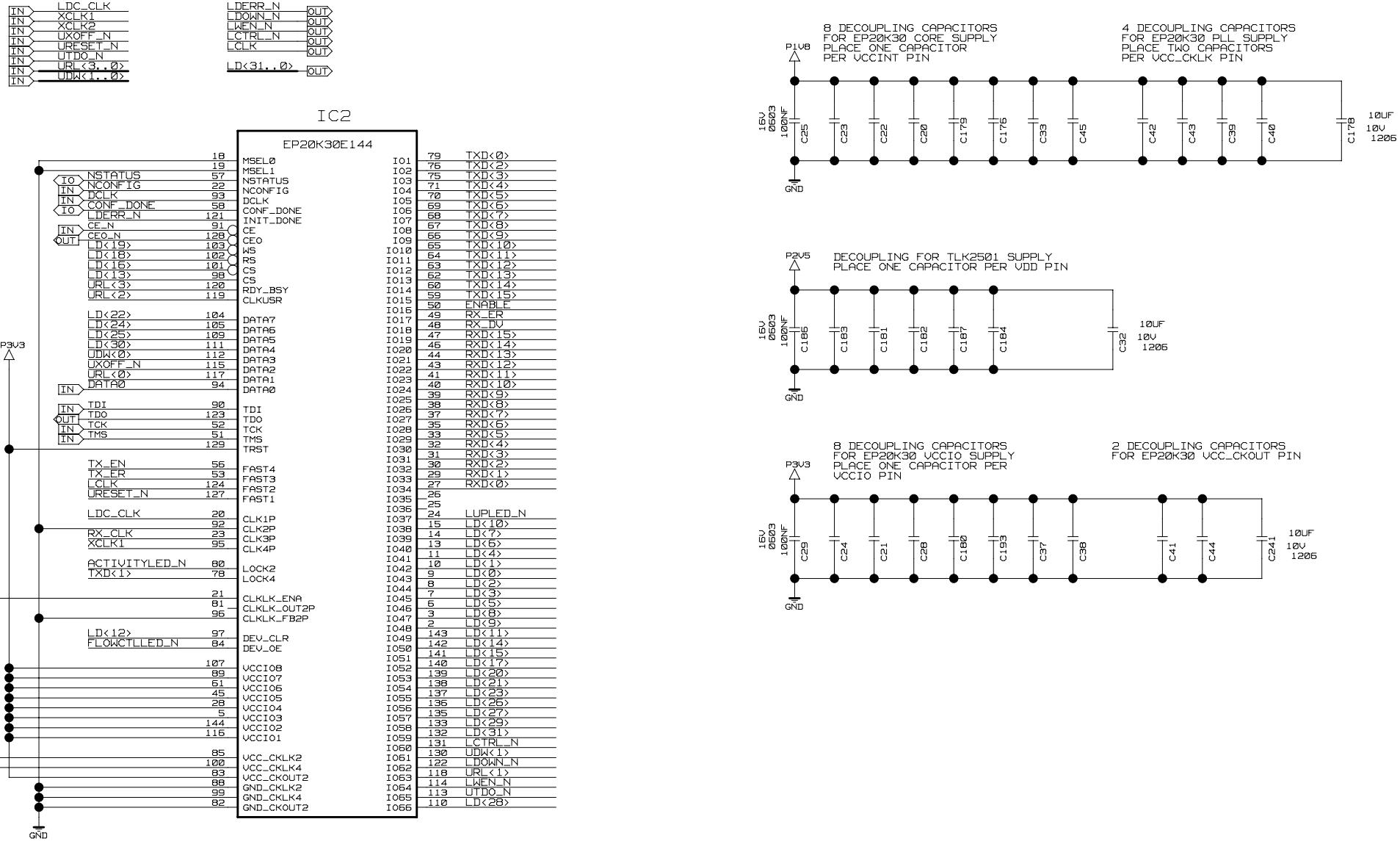


EDMS REF: 337903	VERSION: 1	PCB: EP 680-1169-300	SYSTEM: CADENCE 14.2
REF: DRAWING		TITLE: HOLALDC	HIGH-SPEED OPTICAL LINK FOR ATLAS
IT/CE CERN DIV. EP-ATE 1211 GENEVA 23 SWITZERLAND		ABBREV: HOLALDC	PAGE: 4/13
		LAST_MODIFIED=Thu Feb 6 18:54:02 2003	
		DESSIN: A. RUIZ / ETUDE:	DATE: 6-03-02

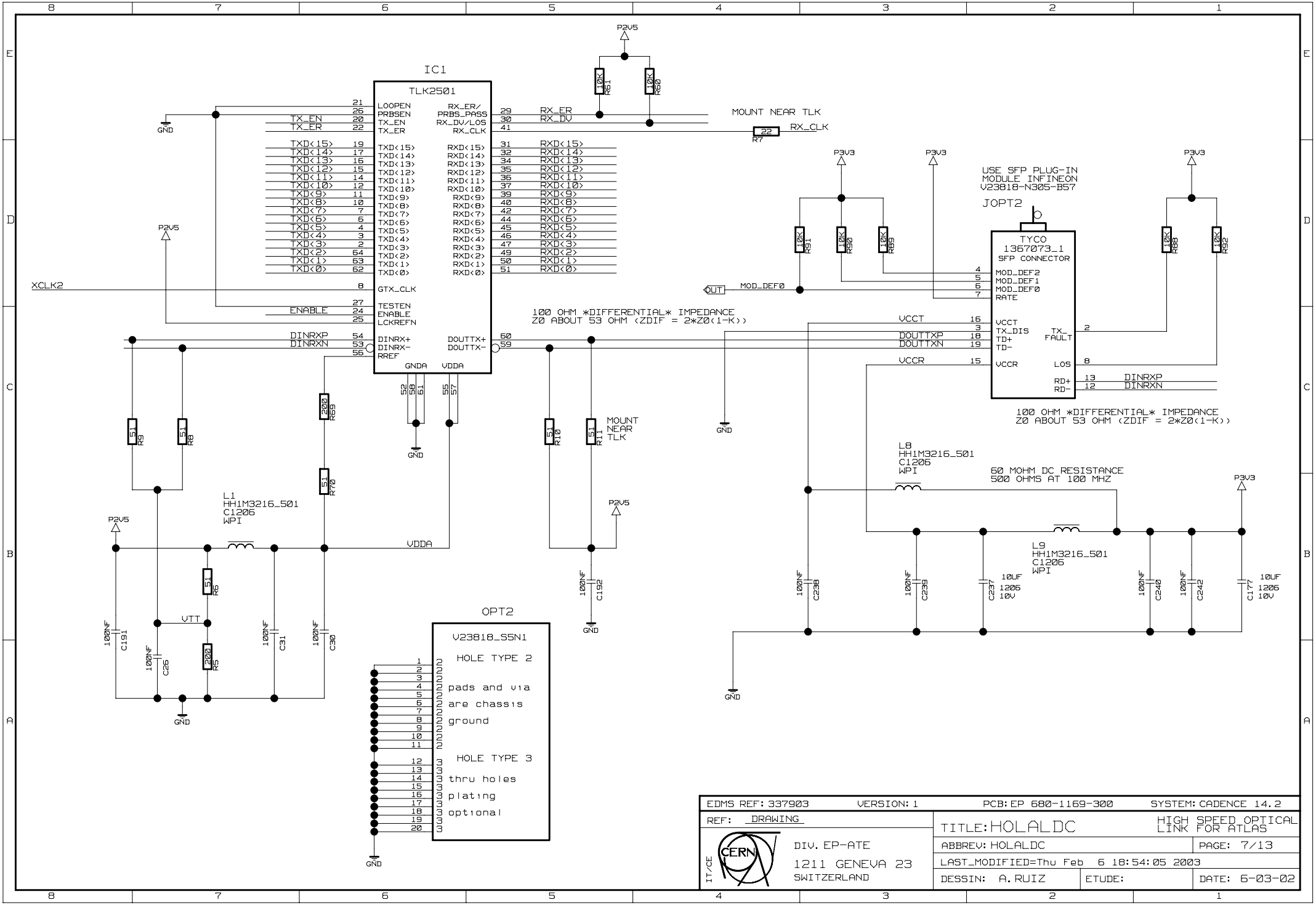


EDMS REF: 337903	VERSION: 1	PCB: EP 680-1169-300	SYSTEM: CADENCE 14.2
REF: DRAWING		TITLE: HOLALDC	HIGH SPEED OPTICAL LINK FOR ATLAS
		ABBREV: HOLALDC	PAGE: 5/13
		LAST_MODIFIED=Thu Feb 6 18:54:05 2003	
		DESSIN: A. RUIZ	ETUDE: DATE: 6-03-02

CERN
IT/CE
DIV. EP-ATE
1211 GENEVA 23
SWITZERLAND



EDMS REF: 337903	VERSION: 1	PCB: EP 680-1169-300	SYSTEM: CADENCE 14.2
REF: DRAWING		TITLE: HOLALDC	HIGH-SPEED OPTICAL LINK FOR ATLAS
		ABBREV: HOLALDC	PAGE: 6/13
		LAST_MODIFIED=Thu Feb 6 18:54:02 2003	
DIV. EP-ATE 1211 GENEVA 23 SWITZERLAND		DESSIN: A. RUIZ	ETUDE: DATE: 6-03-02



EDMS REF: 337903	VERSION: 1	PCB: EP 680-1169-300	SYSTEM: CADENCE 14.2
REF: DRAWING		TITLE: HOLALDC	HIGH SPEED OPTICAL LINK FOR ATLAS
		ABBREV: HOLALDC	PAGE: 7/13
		LAST_MODIFIED=Thu Feb 6 18:54:05 2003	
		DESSIN: A. RUIZ	ETUDE: DATE: 6-03-02

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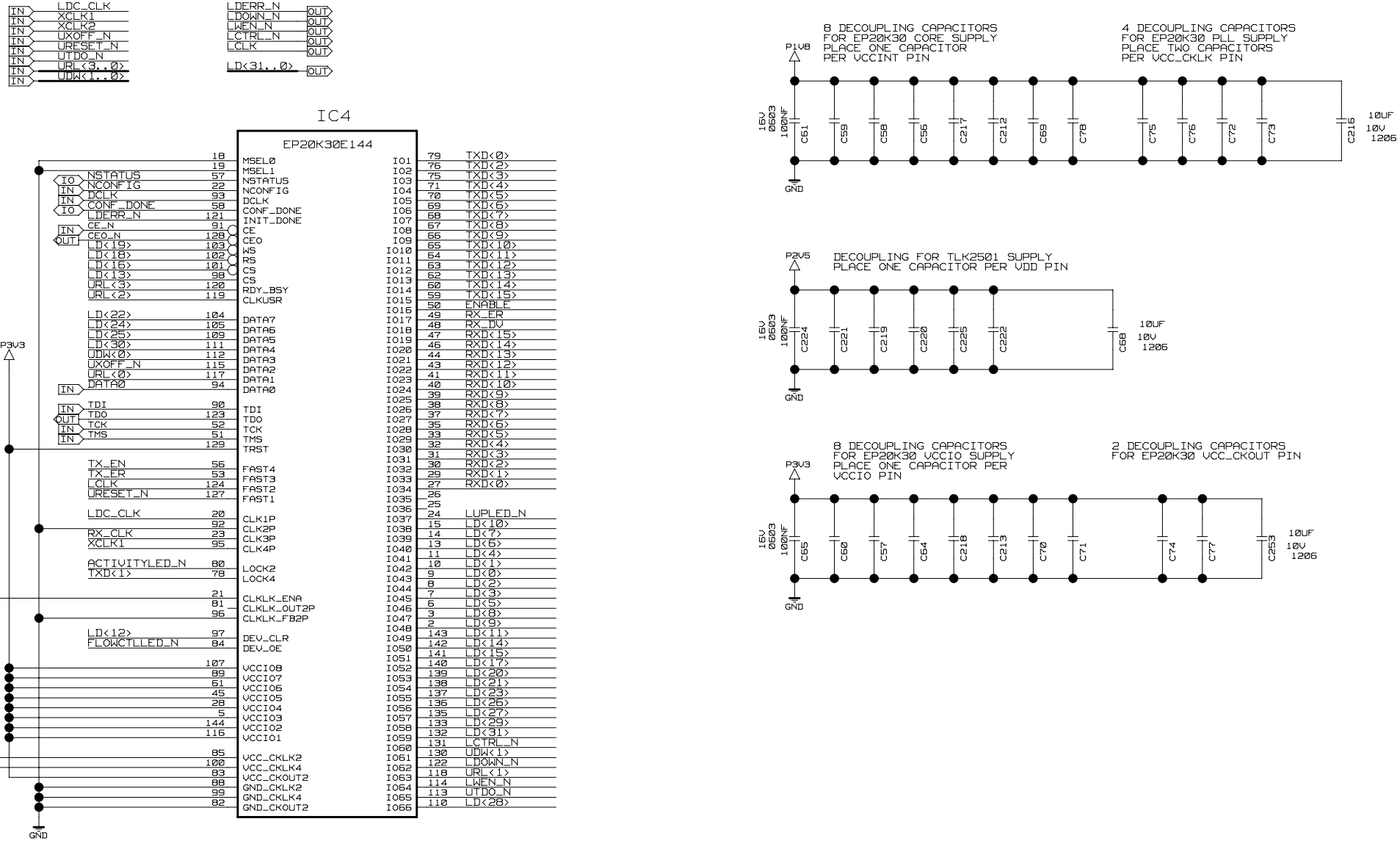
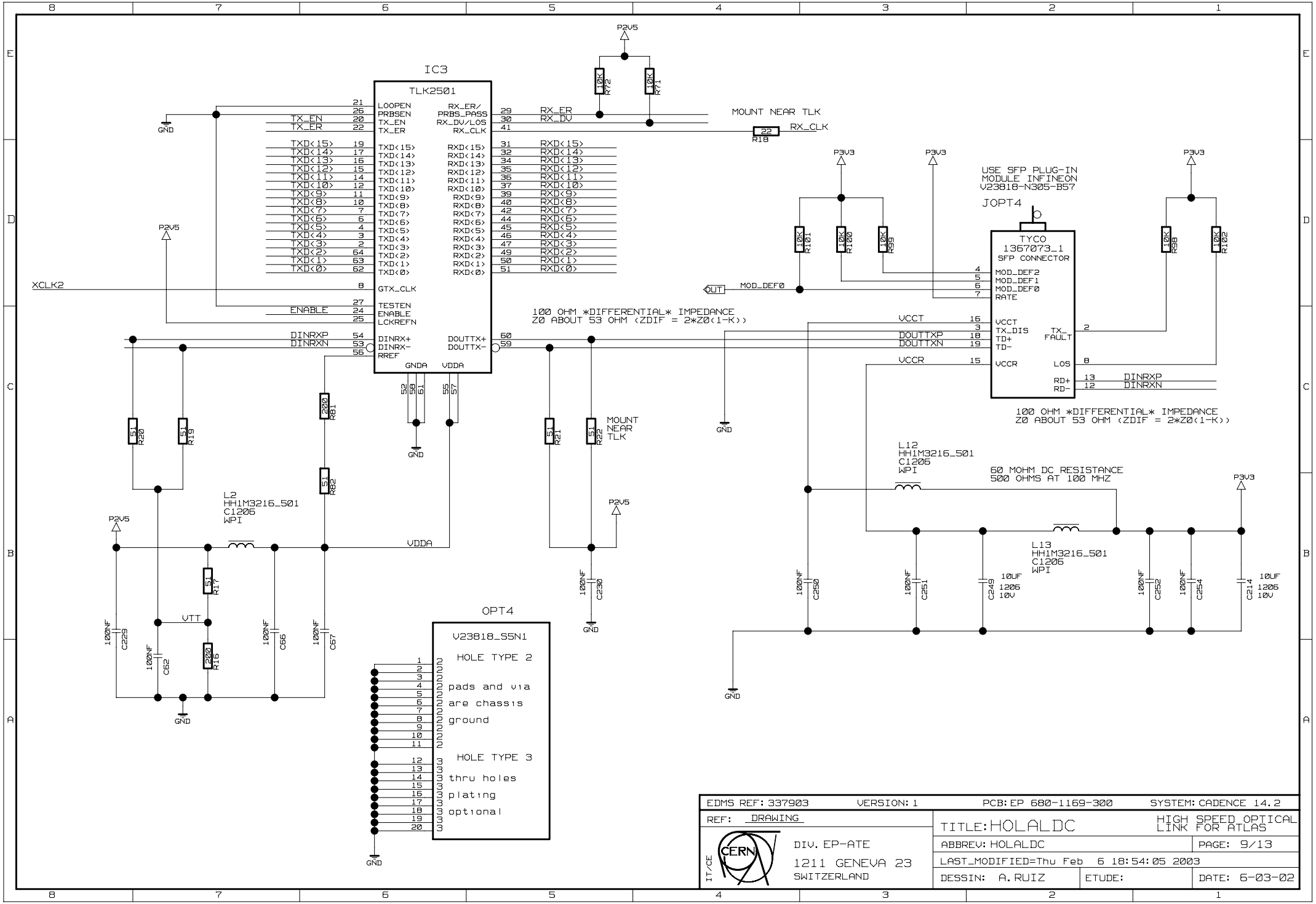
DIV. EP-ATE
1211 GENEVA 23
SWITZERLAND



EDMS REF: 337903	VERSION: 1	PCB: EP 680-1169-300	SYSTEM: CADENCE 14.2
REF: DRAWING		TITLE: HOLALDC	HIGH-SPEED OPTICAL LINK FOR ATLAS
IT/CE CERN DIV. EP-ATE 1211 GENEVA 23 SWITZERLAND		ABBREV: HOLALDC	PAGE: 8/13
		LAST_MODIFIED=Thu Feb 6 18:54:02 2003	
		DESSIN: A. RUIZ	ETUDE: DATE: 6-03-02



EDMS REF: 337903	VERSION: 1	PCB: EP 680-1169-300	SYSTEM: CADENCE 14.2
REF: DRAWING		TITLE: HOLALDC	HIGH SPEED OPTICAL LINK FOR ATLAS
		ABBREV: HOLALDC	PAGE: 9/13
		LAST_MODIFIED=Thu Feb 6 18:54:05 2003	
		DESSIN: A. RUIZ	ETUDE: DATE: 6-03-02

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1211 GENEVA 23
SWITZERLAND

(GND: B3, B15, B17, A18, B22, A24, B28, A30, B34, A35, A37, B38, A42, B46, A48, A56, B57, A63, B64, B67, A69, A72, B73, B76, A78, A81, B82, B85, A87, A90, B91, A93, B94, B50, B51, A50, A51)
(VCCA: A5, B5, B6, A8)
(VCCB: A61, B61, A62, B62)

(P3V3: A10, A16, B19, B59, A59, A66, B70, A75, B79, A84, B88)
(P3V3: A21, B25, A27, B31, A33, B36, A39, B41, B43, A45, A53, B54)

J4
EDGE

CON94AB
PCI_2.2
3V3 CART

AD63	B68	AD63	TRST	A1	
AD62	A68	AD62	TCK	B2	
AD61	B69	AD61	TMS	A3	
AD60	A70	AD60	TDO	B4	
AD59	B71	AD59	TDI	A4	
AD58	A71	AD58			
AD57	B72	AD57			
AD56	A73	AD56	INTA	A6	INTA
AD55	B74	AD55	INTB	B7	
AD54	A74	AD54	INTC	A7	
AD53	B75	AD53	INTD	B8	
AD52	A76	AD52			
AD51	B77	AD51			
AD50	A77	AD50	PRSNT1	B9	
AD49	B78	AD49	PRSNT2	B11	
AD48	A79	AD48			
AD47	B80	AD47			
AD46	A80	AD46	RST	A15	RESET
AD45	B81	AD45	CLK	B16	PCI_CLK
AD44	A82	AD44	GNT	A17	GNT
AD43	B83	AD43	REQ	B18	REQ
AD42	A83	AD42			
AD41	B84	AD41			
AD40	A85	AD40	C/BE7	A64	CBE7
AD39	B86	AD39	C/BE6	B65	CBE6
AD38	A86	AD38	C/BE5	A65	CBE5
AD37	B87	AD37	C/BE4	B66	CBE4
AD36	A88	AD36	C/BE3	B26	CBE3
AD35	B89	AD35	C/BE2	B33	CBE2
AD34	A89	AD34	C/BE1	B44	CBE1
AD33	B90	AD33	C/BE0	A52	CBE0
AD32	A91	AD32			
AD31	B20	AD31			
AD30	A20	AD30	IDSEL	A26	IDSEL
AD29	B21	AD29	FRAME	A34	FRAME
AD28	A22	AD28	IRDY	B35	IRDY
AD27	B23	AD27	TRDY	A36	TRDY
AD26	A23	AD26	DEVSEL	B37	DEVSEL
AD25	B24	AD25	STOP	A38	STOP
AD24	A25	AD24	LOCK	B39	LOCK
AD23	B27	AD23	PERR	B40	PERR
AD22	A28	AD22	3.3VAUX	A14	
AD21	B29	AD21	PME	A19	
AD20	A29	AD20	SERR	B42	SERR
AD19	B30	AD19	PAR	A43	PAR
AD18	A31	AD18	ACK64	B60	ACK64
AD17	B32	AD17	REQ64	A60	REQ64
AD16	A32	AD16	PAR64	A67	PAR64
AD15	A44	AD15	M66ENA	B49	M66ENA
AD14	B45	AD14			
AD13	A46	AD13	+12V	A2	
AD12	B47	AD12	-12V	B1	
AD11	A47	AD11			
AD10	B48	AD10	RESERVED11	A9	
AD9	A49	AD9	RESERVED10	B10	
AD8	B52	AD8	RESERVED9	A11	
AD7	B53	AD7	RESERVED8	B14	
AD6	A54	AD6	RESERVED7	A40	
AD5	B55	AD5	RESERVED6	A41	
AD4	A55	AD4	RESERVED5	B63	
AD3	B56	AD3	RESERVED4	B92	
AD2	A57	AD2	RESERVED3	A92	
AD1	B58	AD1	RESERVED2	B93	
AD0	A58	AD0	RESERVED1	A94	

CP1
FRONT-PANEL MOUNTING HOLES GROUND
CP2
GND

15 W MAXIMUM POWER DISSIPATION
(ONLY 3V3 SUPPLY USED)
GND

C87
100NF
16V
0603
DECOUPLING CAPACITOR REQUIRED
(SECTION 7.8 PCI 2.1 &PCI 2.2)
LOCATE WITHIN 0.25 INCH FROM EDGE CONTACT
GND

3.3V/64-BIT CARD EDGE CONNECTOR
B01 B11 B62 B94

VCCA VCCB
VCC_BAR VCC_BAR
C81
100NF
16V
0603
C88
GND

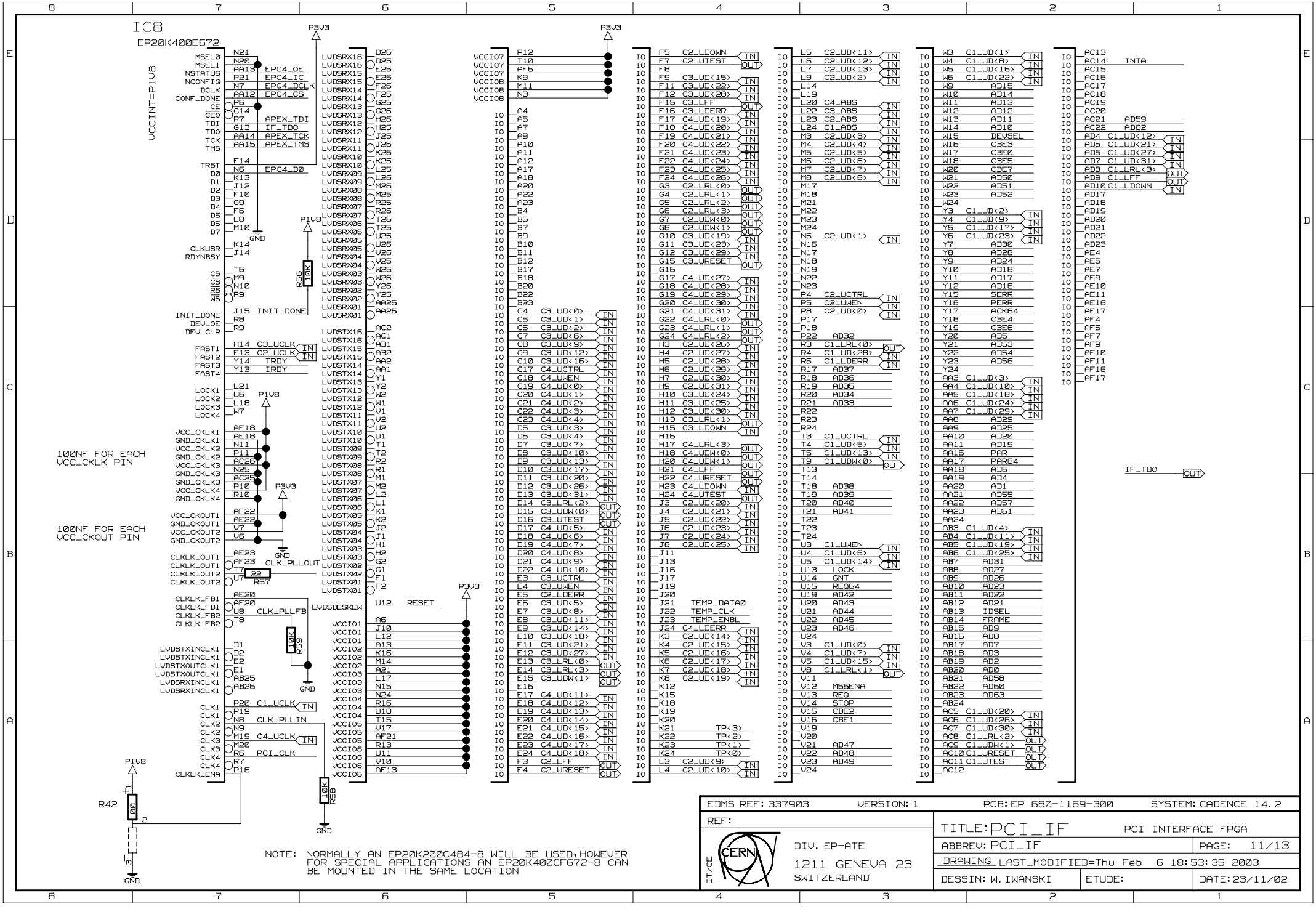
DECOUPLING OF 5V NEAR PCI CONNECTOR
(NO 5V POWER PLANE)

USE CARD IN 3V3 PCI SLOTS ONLY

ROUTING CONSTRAINTS
32-BIT PCI SIGNAL TRACE LENGTH < 1500MIL
64-BIT PCI SIGNAL TRACE LENGTH < 2000MIL
PCI CLK TRACE LENGTH = 2500MIL (+/-100MIL)

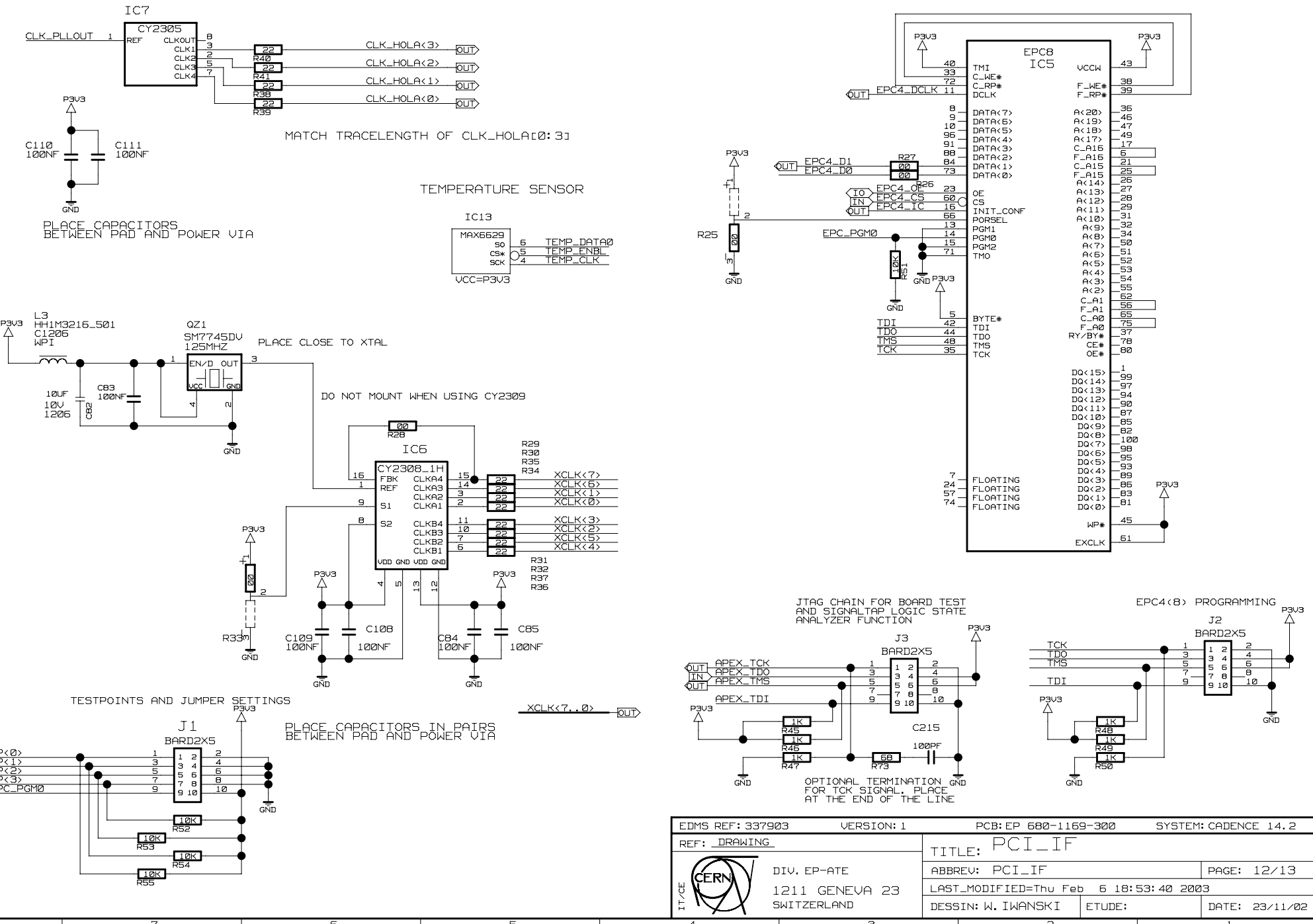
EDMS REF: 337903	VERSION: 1	PCB: EP 680-1169-300	SYSTEM: CADENCE 14.2
REF: DRAWING		TITLE: PCI_IF	PCI EDGE CONNECTOR
		ABBREV: PCI_IF	PAGE: 10/13
		LAST_MODIFIED=Thu Feb 6 18:53:30 2003	
		DESSIN: W. IWANSKI	ETUDE: DATE: 23/11/02

IT/CE
CERN
DIV. EP-ATE
1211 GENEVA 23
SWITZERLAND



NOTE: NORMALLY AN EP20K200C484-8 WILL BE USED, HOWEVER FOR SPECIAL APPLICATIONS AN EP20K400CF672-8 CAN BE MOUNTED IN THE SAME LOCATION

EDMS REF: 337903	VERSION: 1	PCB: EP 680-1169-300	SYSTEM: CADENCE 14.2
REF:		TITLE: PCI_IF	PCI INTERFACE FPGA
DIV. EP-ATE 1211 GENEVA 23 SWITZERLAND		ABBREV: PCI_IF	PAGE: 11/13
		DRAWING_LAST_MODIFIED=Thu Feb 6 18:53:35 2003	
		DESSIN: W. IWANSKI	ETUDE: DATE: 23/11/02


IC7
CY2305
CLK_PLLOUT
REF
CLKOUT
CLK1
CLK2
CLK3
CLK4
R40 22
R41 22
R38 22
R39 22
CLK_HOLA<3>
CLK_HOLA<2>
CLK_HOLA<1>
CLK_HOLA<0>
OUT
P3V3
C110 100NF
C111 100NF
GND
PLACE CAPACITORS
BETWEEN PAD AND POWER VIA
MATCH TRACELENGTH OF CLK_HOLA[0:3]
TEMPERATURE SENSOR
IC13
MAX6529
SO
CS#
SCK
TEMP_DATA0
TEMP_ENBL
TEMP_CLK
VCC=P3V3
L3
HH1M3216_501
C1206
WPI
QZ1
SM7745DV
125MHZ
EN/D
OUT
VCC
GND
PLACE CLOSE TO XTAL
10UF
10V
1206
C82
C83 100NF
DO NOT MOUNT WHEN USING CY2309
R28 00
IC6
CY2308_1H
FBK
REF
S1
S2
CLKA4
CLKA3
CLKA2
CLKA1
CLKB4
CLKB3
CLKB2
CLKB1
VDD GND VDD GND
R29
R30
R35
R34
R31
R32
R37
R36
XCLK<7>
XCLK<6>
XCLK<1>
XCLK<0>
XCLK<3>
XCLK<2>
XCLK<5>
XCLK<4>
R33 00
C109 100NF
C108 100NF
C84 100NF
C85 100NF
TESTPOINTS AND JUMPER SETTINGS
J1
BARD2X5
TP<0>
TP<1>
TP<2>
TP<3>
EPC_PGM0
R52 10K
R53 10K
R54 10K
R55 10K
PLACE CAPACITORS IN PAIRS
BETWEEN PAD AND POWER VIA
XCLK<7..0>
EPC8
IC5
TMI
C_WE#
C_RP#
DCLK
DATA<7>
DATA<6>
DATA<5>
DATA<4>
DATA<3>
DATA<2>
DATA<1>
DATA<0>
OE
CS
INIT_CONF
PORSEL
PGM1
PGM0
PGM2
TMO
BYTE#
TDI
TDO
TMS
TCK
FLOATING
VCCW
F_WE#
F_RP#
A<20>
A<19>
A<18>
A<17>
C_A16
F_A16
C_A15
F_A15
A<14>
A<13>
A<12>
A<11>
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A<4>
A<3>
A<2>
C_A1
F_A1
C_A0
F_A0
RY/BY#
CE#
OE#
DQ<15>
DQ<14>
DQ<13>
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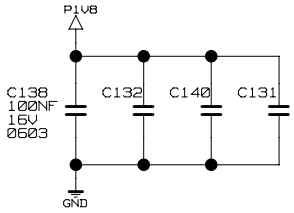
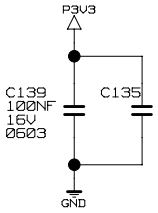
DQ<11>
DQ<10>
DQ<9>
DQ<8>
DQ<7>
DQ<6>
DQ<5>
DQ<4>
DQ<3>
DQ<2>
DQ<1>
DQ<0>
WP#
EXCLK
EPC4_DCLK
EPC4_D1
EPC4_D0
EPC4_OE
EPC4_CS
EPC4_IC
IO
IN
R27 00
R26 00
R25 00
EPC_PGM0
10K R51
JTAG CHAIN FOR BOARD TEST
AND SIGNALTAP LOGIC STATE
ANALYZER FUNCTION
J3
BARD2X5
APEX_TCK
APEX_TDO
APEX_TMS
APEX_TDI
1K R45
1K R46
1K R47
68 R73
C215 100PF
OPTIONAL TERMINATION
FOR TCK SIGNAL. PLACE
AT THE END OF THE LINE
EPC4(8) PROGRAMMING
J2
BARD2X5
TCK
TDO
TMS
TDI
1K R48
1K R49
1K R50
EDMS REF: 337903
VERSION: 1
PCB: EP 680-1169-300
SYSTEM: CADENCE 14.2
REF: DRAWING
TITLE: PCI_IF
DIV. EP-ATE
1211 GENEVA 23
SWITZERLAND
IT/CE
ABBREV: PCI_IF
PAGE: 12/13
LAST_MODIFIED=Thu Feb 6 18:53:40 2003
DESSIN: W. IWANSKI
ETUDE:
DATE: 23/11/02

PLL POWER SUPPLY DECOUPLING



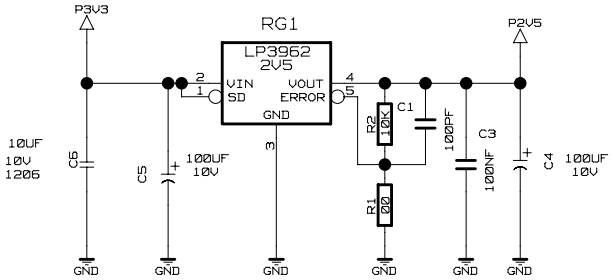
PLACE CERAMIC CAPACITORS
CLOSE TO VCC_CKLK PINS
(ONE CAPACITOR PER PIN)



PLACE CERAMIC CAPACITORS
CLOSE TO VCC_CKOUT PINS
(ONE CAPACITOR PER PIN)

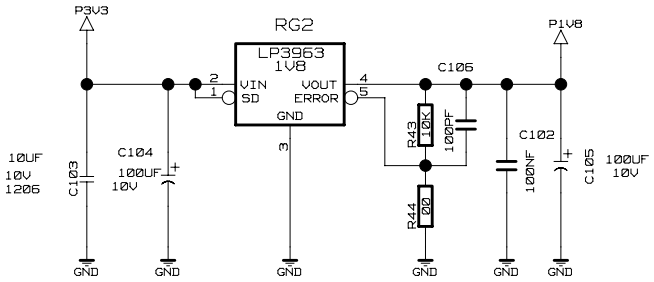
TI SERDES SUPPLY 2.5V

1.5A ULTRA-LOW DROPOUT REGULATOR
THE FOLLOWING VOLTAGE REGULATORS CAN BE USED:
MIC39151, LP3962/3965, LT1963A

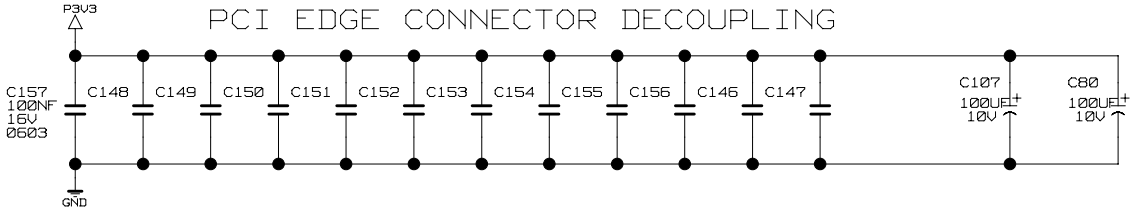


ALTERA CORE SUPPLY 1.8V

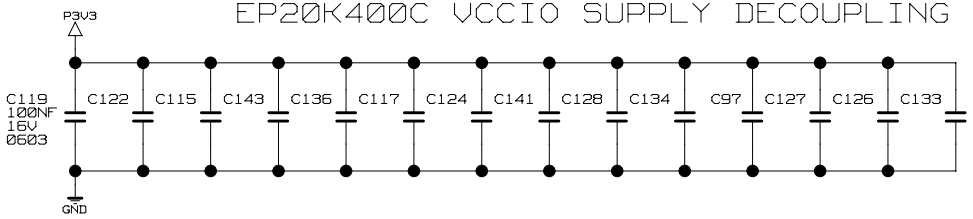
3A ULTRA-LOW DROPOUT REGULATOR
THE FOLLOWING VOLTAGE REGULATORS CAN BE USED:
MIC29301/29302, LP3963/3966, LT1764A



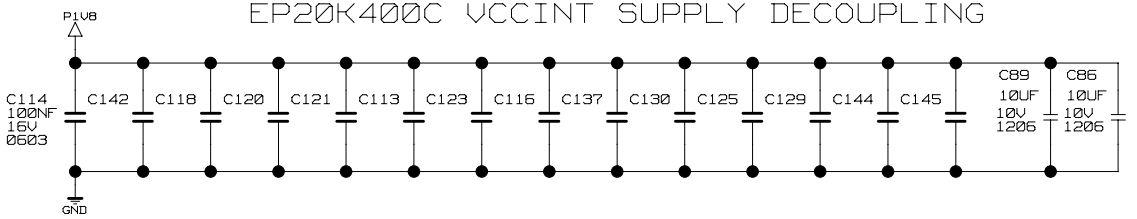
PCI EDGE CONNECTOR DECOUPLING

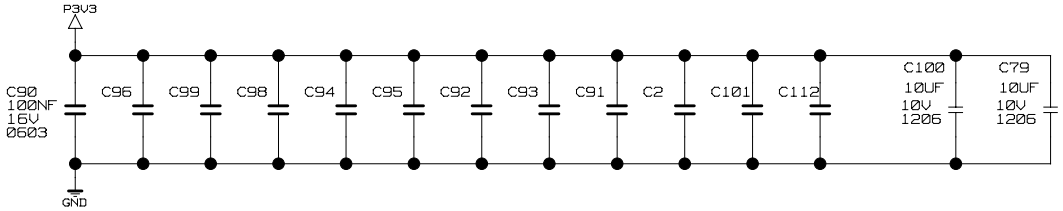


EP20K400C VCCIO SUPPLY DECOUPLING



EP20K400C VCCINT SUPPLY DECOUPLING





EDMS REF: 337903	VERSION: 1	PCB: EP 680-1169-300	SYSTEM: CADENCE 14.2
REF:		TITLE: PCI_IF	DECOUPLING CAPACITORS
DIV. EP-ATE 1211 GENEVA 23 SWITZERLAND		ABBREV: PCI_IF	PAGE: 13/13
		DRAWING LAST_MODIFIED=Thu Feb 6 18:53:44 2003	
		DESSIN: W. IWANSKI	ETUDE: DATE: 23/11/02