NOAO	DOC #			SERL #	REV #	Next assembly	TITLE FLD 1 DOC TYPE	TITLE FIELD 2 ITEM NAME	TITLE FIELD 3 DESCRIPTION	TITLE FIELD 4 INFORMATION	comments
MNSN-	**EL-06-**	**0**	**001**				Firmware	Standard Template	FPGA	Bus Interface	Bus Ifc Templates for 7.09 & 7.10
MNSN-	EL-06-	0	002				Firmware	Standard Template	FPGA	Personality Module	Address decode for Peripheral Board
MNSN-	EL-06-	0	003		V34	MNSN-EL-10-0400	Firmware	Master Control Board	Sequencer FPGA	Prototype Hardware	Early VIRTEX device
MNSN-	EL-06-	0	004		V34	MNSN-EL-10-0400	Firmware	Master Control Board	Fiber FPGA	Prototype Hardware	Early VIRTEX device
MNSN-	EL-06-	0	005		V40	MNSN-EL-10-0400	Firmware	Master Control Board	Sequencer FPGA	Rev 'A' Hardware	First Stable version for Rev 'A' HW
MNSN-	EL-06-	0	006		V40	MNSN-EL-10-0400	Firmware	Master Control Board	Pixel FPGA	Rev 'A' Hardware	First Stable version for Rev 'A' HW
MNSN-	EL-06-	0	007		V42	MNSN-EL-10-0400	Firmware	Master Control Board	Pixel FPGA	Rev 'A' Hardware	Fixed bug in Serial EEPROM module
MNSN-	EL-06-	0	008		V421	MNSN-EL-10-0400	Firmware	Master Control Board	Sequencer FPGA	Rev 'A' Hardware	8 & 6 Slot backplane compatible
MNSN-	EL-06-	0	009		V43	MNSN-EL-10-0400	Firmware	Master Control Board	Sequencer FPGA	Rev 'A' Hardware	Bug fix on MPU seq initialization
MNSN-	EL-06-	0	010		V44	MNSN-EL-10-0400	Firmware	Master Control Board	Sequencer FPGA	Rev 'A' Hardware	Added double pix transfer capability
MNSN-	EL-06-	0	011		V44	MNSN-EL-10-0400	Firmware	Master Control Board	Pixel FPGA	Rev 'A' Hardware	Added double pix transfer capability
MNSN-	EL-06-	0	012		V45	MNSN-EL-10-0400	Firmware	Master Control Board	Sequencer FPGA	Rev 'A' Hardware	event register and debug register func
MNSN-	EL-06-	0	013		V45	MNSN-EL-10-0400	Firmware	Master Control Board	Pixel FPGA	Rev 'A' Hardware	Debug for data dropout analysis
MNSN-	EL-06-	0	014		V451	MNSN-EL-10-0400	Firmware	Master Control Board	Pixel FPGA	Rev 'A' Hardware	Attempt to fix data dropout problem
MNSN-	EL-06-	0	015		V46	MNSN-EL-10-0400	Firmware	Master Control Board	Pixel FPGA	Rev 'A' Hardware	Bug Fix on PAN Comms Sync bit
MNSN-	EL-06-	0	016		V461	MNSN-EL-10-0400	Firmware	Master Control Board	Sequencer FPGA	Rev 'A' Hardware	support for pix simulation functions
MNSN-	EL-06-	0	017		V461	MNSN-EL-10-0400	Firmware	Master Control Board	Pixel FPGA	Rev 'A' Hardware	
MNSN-	EL-06-	0	018		V462	MNSN-EL-10-0400	Firmware	Master Control Board	Sequencer FPGA	Rev 'A' Hardware	Adaption for use with S-LINK comms
MNSN-	EL-06-	0	019		V462	MNSN-EL-10-0400	Firmware	Master Control Board	Pixel FPGA	Rev 'A' Hardware	Adaption for use with S-LINK comms
MNSN-	EL-06-	0	020		V463	MNSN-EL-10-0400	Firmware	Master Control Board	Sequencer FPGA	Rev 'A' Hardware	PAN command "echo disable" bit added
MNSN-	EL-06-	0	021		V491	MNSN-EL-10-0402	Firmware	Master Control Board	Sequencer FPGA	Rev 'A' Hardware	QUOTA Sequencer functions added
MNSN-	EL-06-	0	022		V35	MNSN-EL-10-0100	Firmware	IR Acquisition	FPGA	Prototype Hardware	First Stable version
MNSN-	EL-06-	0	023		V35	MNSN-EL-10-0100	Firmware	IR Acquisition	CPLD	Prototype Hardware	First Stable version
MNSN-	EL-06-	0	024		V371	MNSN-EL-10-0100	Firmware	IR Acquisition	FPGA	Prototype Hardware	V41 compatile with Prototype Boards
MNSN-	EL-06-	0	025		V40	MNSN-EL-10-0100	Firmware	IR Acquisition	FPGA	Rev 'A' Hardware	Use with CPLD Version 4.0
MNSN-	EL-06-	0	026		V40	MNSN-EL-10-0100	Firmware	IR Acquisition	CPLD	Rev 'A' Hardware	rev A & B compatible
MNSN-	EL-06-	0	027		V413	MNSN-EL-10-0100	Firmware	IR Acquisition	FPGA	Rev 'A' Hardware	Use with CPLD Version 4.0
MNSN-	EL-06-	0	028		V42	MNSN-EL-10-0100	Firmware	IR Acquisition	FPGA	Rev 'B' Hardware	Use with CPLD Version 4.0
MNSN-	EL-06-	0	029		V11	MNSN-EL-10-0300	Firmware	Clock & Bias	Sequencer CPLD	Prototype Hardware	First Stable version
MNSN-	EL-06-	0	030		V12	MNSN-EL-10-0300	Firmware	Clock & Bias	Configuration CPLD	Prototype Hardware	First Stable version
MNSN-	EL-06-	0	031		V12	MNSN-EL-10-0300	Firmware	Clock & Bias	FPGA	Prototype Hardware	First Stable version
MNSN-	EL-06-	0	032		V40	MNSN-EL-10-0300	Firmware	Clock & Bias	Configuration CPLD	Rev 'A' Hardware	First Stable version for Rev 'A' HW
MNSN-	EL-06-	0	033		V41	MNSN-EL-10-0300	Firmware	Clock & Bias	Configuration CPLD	Rev 'A' Hardware	Changed polarity for the MUX ENP bit
MNSN-	EL-06-	0	034		V40	MNSN-EL-10-0300	Firmware	Clock & Bias	Sequencer CPLD	Rev 'A' Hardware	First Stable version for Rev 'A' HW
MNSN-	EL-06-	0	035		V40	MNSN-EL-10-0300	Firmware	Clock & Bias	FPGA	Rev 'A' Hardware	First Stable version for Rev 'A' HW
MNSN-	EL-06-	0	036		V41	MNSN-EL-10-0300	Firmware	Clock & Bias	FPGA	Rev 'A' Hardware	Changed Fbias Addressing scheme
MNSN-	EL-06-	0	037		V42	MNSN-EL-10-0300	Firmware	Clock & Bias	FPGA	Rev 'A' Hardware	Bug fix for Fbias functions
MNSN-	EL-06-	0	038		V490	MNSN-EL-10-0300	Firmware	Clock & Bias	FPGA	Rev 'A' Hardware	Specific to OTA Testing. Emul DOP.
MNSN-	EL-06-	0	039		V11	MNSN-EL-10-0500	Firmware	CCD 8 Ch Acquisition Board	FPGA	Prototype Hardware	First Stable version
MNSN-	EL-06-	0	040		V14	MNSN-EL-10-0500	Firmware	CCD 8 Ch Acquisition Board	CPLD	Prototype Hardware	First Stable version
MNSN-	EL-06-	0	041		V15	MNSN-EL-10-0500	Firmware	CCD 8 Ch Acquisition Board	CPLD	Prototype Hardware	Development Version
MNSN-	EL-06-	0	042		V16	MNSN-EL-10-0500	Firmware	CCD 8 Ch Acquisition Board	FPGA	Prototype Hardware	Built to support ADC busy signal
MNSN-	EL-06-	0	043		V16	MNSN-EL-10-0500	Firmware	CCD 8 Ch Acquisition Board	CPLD	Prototype Hardware	Modified ADC Busy logic
MNSN-	EL-06-	0	044		V17	MNSN-EL-10-0500	Firmware	CCD 8 Ch Acquisition Board	FPGA	Prototype Hardware	Bug fix to version 1.6
MNSN-	EL-06-	0	045		V17	MNSN-EL-10-0500	Firmware	CCD 8 Ch Acquisition Board	CPLD	Prototype Hardware	Bug fix to version 1.6
MNSN-	EL-06-	0	046		V18	MNSN-EL-10-0500	Firmware	CCD 8 Ch Acquisition Board	FPGA	Prototype Hardware	Enhancements to 1.7
MNSN-	EL-06-	0	047		V18	MNSN-EL-10-0500	Firmware	CCD 8 Ch Acquisition Board	CPLD	Prototype Hardware	Enhancements to 1.7
MNSN-	EL-06-	0	048		V191	MNSN-EL-10-0500	Firmware	CCD 8 Ch Acquisition Board	FPGA	Prototype Hardware	Bug fix to version 1.8
MNSN-	EL-06-	0	049		V20	MNSN-EL-10-0500	Firmware	CCD 8 Ch Acquisition Board	FPGA	Prototype Hardware	Added MicroSequencer module
MNSN-	EL-06-	0	050		V40	MNSN-EL-10-0500	Firmware	CCD 8 Ch Acquisition Board	FPGA	Rev 'A' Hardware	First Stable version for Rev 'A' HW
MNSN-	EL-06-	0	051		V41	MNSN-EL-10-0500	Firmware	CCD 8 Ch Acquisition Board	FPGA	Rev 'A' Hardware	Added debug registers, enhancements

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MNSN-	EL-06-	0	052		V41	MNSN-EL-10-0500	Firmware	CCD 8 Ch Acquisition Board	CPLD	Rev 'A' Hardware	Minor enhancements to Version 4.0
MNSN-	EL-06-	0	053		V411	MNSN-EL-10-0500	Firmware	CCD 8 Ch Acquisition Board	FPGA	Rev 'A' Hardware	Added DOP/CDS port priority scheme
MNSN-	EL-06-	0	054		V42	MNSN-EL-10-0500	Firmware	CCD 8 Ch Acquisition Board	FPGA	Rev 'A' Hardware	Uses ADC Slave serial data clocking
MNSN-	EL-06-	0	055		V42	MNSN-EL-10-0500	Firmware	CCD 8 Ch Acquisition Board	CPLD	Rev 'A' Hardware	Uses ADC Slave serial data clocking
MNSN-	EL-06-	0	056		V490	MNSN-EL-10-0501	Firmware	CCD 8 Ch Acquisition Board	FPGA	Rev 'A' Hardware	Support for OTA Row/Col DOP logic
MNSN-	EL-06-	0	057		V491	MNSN-EL-10-0501	Firmware	CCD 8 Ch Acquisition Board	FPGA	Rev 'A' Hardware	DOP port bit re-assignment for MIB
MNSN-	EL-06-	0	058		V41	MNSN-EL-10-0100	Firmware	IR Acquisition	CPLD	Rev 'B' Hardware	use with FPGA v42 whirc specific
MNSN-	EL-06-	0	059		V463	MNSN-EL-10-0400	Firmware	Master Control Board	Pixel FPGA	Rev 'A' Hardware	syn pxl gen, pxl data sim
MNSN-	EL-06-	0	060		V492	MNSN-EL-10-0402	Firmware	Master Control Board	Sequencer FPGA	Rev 'A' Hardware	QUOTA Sequencer functions added
MNSN-	EL-06-	0	061		V43	MNSN-EL-10-0300	Firmware	Clock & Bias	Configuration CPLD	Rev 'A' Hardware	removed front pnl clk mux enable logic
MNSN-	EL-06-	0	062		V492	MNSN-EL-10-0300	Firmware	Clock & Bias	FPGA	Rev 'A' Hardware	Specific to OTA Testing. Emul DOP.
MNSN-	EL-06-	0	063		V495	MNSN-EL-10-0501	Firmware	CCD 8 Ch Acquisition Board	FPGA	Rev 'A' Hardware	open comment for complete desc.
MNSN-	EL-06-	0	064		V464	MNSN-EL-10-0402	Firmware	Master Control Board	Pixel FPGA	Rev 'A' Hardware	synchronization logic
MNSN-	EL-06-	0	065		V495	MNSN-EL-10-0402	Firmware	Master Control Board	Sequencer FPGA	Rev 'A' Hardware	Chg use of ExData signals enhance synchronization logic
MNSN-	EL-06-	0	066		V467	MNSN-EL-10-0402	Firmware	Master Control Board	Sequencer FPGA	Rev 'A' Hardware	temp sensor fix
MNSN-	EL-06-	0	067		V44	MNSN-EL-10-0300	Firmware	Clock & Bias	FPGA	Rev 'A' Hardware	temp sensor fix
MNSN-	EL-06-	0	068		V412	MNSN-EL-10-0501	Firmware	CCD 8 Ch Acquisition Board	FPGA	Rev 'A' Hardware	temp sensor fix
MNSN-	EL-06-	0	069		V416	MNSN-EL-10-0100	Firmware	IR Acquisition	FPGA	Rev 'A' Hardware	Use with CPLD Version 4.0
MNSN-	EL-06-	0	070		V421	MNSN-EL-10-0100	Firmware	IR Acquisition	FPGA	Rev 'B' Hardware	Use with CPLD Version 4.1
MNSN-	**EL-06-**	**9**	**500**		V1.6		Firmware	Current Monsoon Firmware	Quick Guide Loader Files		