NATIONAL
OPTICAL
ASTRONOMY
OBSERVATORY

MAJOR INSTRUMENTATION GROUP
950 N. Cherry Ave.
P. O. Box 26732
Tucson, Arizona 85726-6732
(520) 318-8000 FAX: (520) 318-8303

MONSOON

Clock and Bias Board

Clock and Bias Board Description
With Version 4.1x Firmware

NOAO Document MNSN-AD-08-0003
Revision: 1.3

Authored by:
Peter Moore
6/19/2006

Please send comments:
pmoore@noao.edu

Revision History

Version	Date Approved	Sections Affected	Remarks
0	6/19/2006	--	Original Version
1.0	4/20/2007	Figures 1 and 2 Figure 3 1.4 2.1.2 2.2 Tables 15 and 15 Table 17 Appendix II	Updated. Added new data path graphic. Removed figures that were duplicated in Table 8. Expanded to provide power supply information and to update Table 11. Extensive update. Updated. Corrected specifications. Added to provide information on Front Panel Test Point Programming.
1.1	5/11/2007	1.3.2	Added Figure 4, Clock and Bias Board Principal Data Path. Enhanced diagrams for Figures 10 and 11.
1.2	1/16/2008	1.3 2.1.1 2.2.2 2.2.3 2.2.7	Repaired Figure 4. Change U142 to U203. Change JP12 and JP14 to JP9 and JP10. Change U70 to U204. Change U143 to U200. Change J7 to J6. Add "/MAS9187" after "AD8802 and change 3.04v to 2.048v.
1.3	11/5/2009	1.4	Added addresses to function names in the descriptions following Table 7.

Table of Contents

Revision History **2**

Table of Contents **3**

List of Figures **5**

List of Tables **5**

Preface **6**

Document Scope **6**

Document Legend **6**

1.0 Board Functional Description **7**

1.1 Purpose of Board 7
1.2 Interface Description 8
1.2.1 PCI Connectors J1 and J2 8
1.2.1.1 Board Clock and Board Select Signals 8
1.2.1.2 Sequencer Bus Interface 8
1.2.1.3 Pixel Data Bus Interface 10
1.2.2 JTAG Interface, Reset and Power On Boot 10
1.2.3 Front Panel Indicators 11
1.2.4 Front Panel Test Points 12
1.2.5 PCI Connectors J3, J4 and J5 13
1.3 Data Paths 16
1.3.1 Control Data 16
1.3.2 Configuration Data 16
1.4 Control Functions 17
1.4.1 Clock Control Register 19
1.4.2 Fast Bias Index Registers 19
1.4.3 Fast Bias DAC Bank Registers 20
1.4.4 Bias Voltage DAC Registers 20
1.4.5 Clock Low Rail Voltage Registers 20
1.4.6 Clock High Rail Voltage Registers 20
1.4.7 Bias and Clock Enables Register 20
1.4.8 Front Panel Clock Monitor Port Selector Register 21
1.4.9 Bias Voltage Telemetry Mode Registers 21
1.4.10 Bias Current Telemetry Mode Registers 22
1.4.11 Clock Voltage Telemetry Mode Registers 22
1.4.12 Fast Bias Voltage Telemetry Mode Registers 22
1.4.13 Supply Voltage Telemetry Mode Registers 23
1.4.14 Reference Voltage Telemetry Mode Registers 23
1.4.15 Bias Voltage Telemetry Data Registers 23
1.4.16 Bias Current Telemetry Data Registers 23

Table of Contents (Cont.)

1.4.17 Clock Voltage Telemetry Data Registers 23
1.4.18 Fast Bias Voltage Telemetry Data Registers 23
1.4.19 Power Supply Voltage Telemetry Data Registers 24
1.4.20 Reference Voltage Telemetry Data Registers 24
1.4.21 Global Event Register 24
1.4.22 Front Panel LED Control Register 24
1.4.23 Silicon Serial Number Register 25
1.4.24 Board Temperature Register 25
1.4.25 Board Control Register 25
1.4.26 Board Status Register 25
1.4.27 Board Identity Code Register 25
1.4.28 Firmware Code Revision register 25

2.0 Board Hardware Description 26
2.1 Power Supplies 26
2.1.1 Digital Supplies 26
2.1.2 Analog Supplies 26
2.2 Logic Section 27
2.2.1 Clock Generation 27
2.2.2 Reset and FPGA Boot Logic 27
2.2.3 JTAG Interface 27
2.2.4 FPGA CPLD Communication Path 28
2.2.5 Configuration CPLD Logic 30
2.2.6 Sequencer Clock CPLD Logic 33
2.2.7 Reference Voltage Generators 34
2.2.8 Bias Voltage Generators 36
2.2.9 Fast Bias Voltage Generators 38
2.2.10 Clock Generator Circuits 39
2.3 Jumper Descriptions 41

3.0 Board Specifications 43

4.0 Appendix I - MONSOON to NEWFIRM 44

Appendix II - Front Panel Test Point Programming 45

List of Figures

Figure 1 Clock and Bias Board Block Diagram 7
Figure 2 JTAG Device Ordering 10
Figure 3 Clock and Bias Board Front Panel 12
Figure 4 Clock and Bias Board Principal Data Paths 16
Figure 5 Fast Bias Index Register 20
Figure 6 Bias and Clock Enables Register 20
Figure 7 Front Panel Clock Monitor Port Select Register 21
Figure 8 Board Control Register Bit Fields 25
Figure 9 Board Status Register 25
Figure 10 Clock and Bias FPGA 29
Figure 11 U119 Configuration CPLD 31
Figure 12 Sequencer Clock CPLD 34
Figure 13 Bias DAC Voltage Reference Generator 35
Figure 14 Typical Offset Reference Voltage Generator 36
Figure 15 Typical Bias Generator Circuit 37
Figure 16 Typical Fast Bias Circuit 39
Figure 17 Clock Driver Circuit 40
Figure 18 Sample Bill of Materials 44
Figure 19 Telnet Connect Host Window 45
Figure 20 Authentication Window 45
Figure 21 PAN and MEC Windows 47
Figure 22 Configuration Files Window 48
Figure 23 Attribute Categories Window 48
Figure 24 Attribute Categories Window 49

List of Tables

Table 1 Sequencer Bus Mode Bit Definitions 9
Table 2 Front Panel Indicator Functions 11
Table 3 J3 Connector Pinout Description 13
Table 4 J4 Connector Pinout Description 14
Table 5 J5 Connector Pinout Description 15
Table 6 Sequencer Bus Address Mapping 17
Table 7 Clock and Bias Memory Map 18
Table 8 Bit Significance 22
Table 9 Global Event Register Bit Fields 24
Table 10 LED Indicator Function Codes 24
Table 11 Power Supply Current Draws 27
Table 12 JTAG Pin Assignments 28
Table 13 Serial Data Stream Decoding 32
Table 14 Sequencer Clock CPLD Logic Values 33
Table 15 Configuration Jumper Descriptions 41
Table 16 Test Point Functions 41
Table 17 Specifications 43

Preface

This document has relevence to the hardware implementation of the MONSOON Clock and Bias Board that boots the FPGA firmware revision 4.1 and later. Minor revisions and modifications to the capabilities and functionality of this board can be added as an appendix to this document. Major modifications to the functionality of the board that would require extensive modification to this document must originate a new and separate board description document.

Document Scope

This document provides an overall description, as well as detailed information on the architecture, configuration, testing and functionality of the MONSOON Clock and Bias Board. The intention is that this document be read by anyone who is considering, building, using or testing a MONSOON system that requires this hardware module.

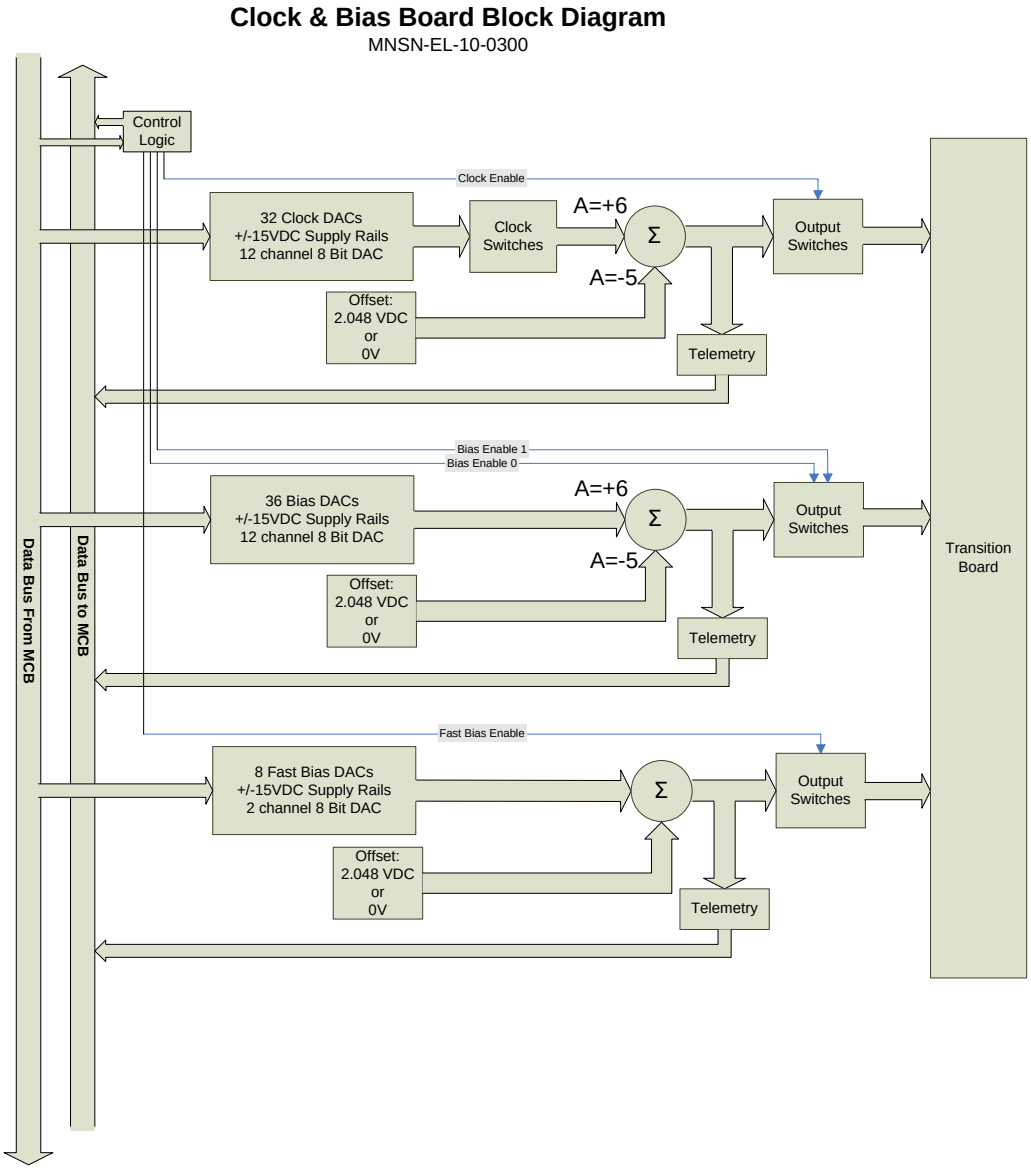
Document Legend

Within this document, hardware signals are highlighted using an upper case bold black 12-point script typeface (e.g. **CLK_SIGNAL**). Hardware signals that are negative true are preceded by a slash character (e.g. **/SIGNAL**). Firmware control registers and internal device signals are highlighted using an upper case purple 12-point typeface (e.g. FIRMWARE_SIGNAL). Negative true firmware signals are denoted by a '_N' suffix (e.g. TRUE_N). Additionally, the various buttons on the MONSOON Engineering Console and other computer displays are represented as ***>Xxxxx<*** where xxxx is the title of the particular button to be acted on.

1.0 Board Functional Description

1.1 Purpose of Board

The Clock and Bias board (CLK) is designed to stimulate IR and CCD optical detectors. It is one of a series of peripheral boards using the MONSOON open source specification to allow medium and large arrays of detector elements to be controlled using a generic architecture. Each Clock and Bias board plugs into a standard MONSOON Detector Head Electronics (DHE) backplane and provides 32 clock drivers, 36 low voltage biases (-12 to +12 V) for detector biasing, and eight fast bias supplies that can be used for multilevel clocking. See Figure 1 for a block diagram.



Clock and Bias Board
Figure 1

1.2 Interface Description

1.2.1 PCI Connectors J1 and J2

These two hard metric connectors form the interface to the MONSOON backplane and support the signal bus structures described in the sub paragraphs below. The complete physical description of these connectors is contained in the document 'ICD 7.0 DHE Backplane Definition' (MNSN-AD-01-0006_V13).

1.2.1.1 Board Clock and Board Select Signals

Each board fitted to the MONSOON backplane has a separate clock feed that is sourced from the MCB and received on connector J1 pin D6 (J1:D6). This clock is fed to the Clock and Bias Control FPGA U116. It provides for the synchronization of all bus transactions and clocks all internal functions of this board. The appropriate bit of the MCB clock control register (MCB_CLKENABLES) corresponding to the physical slot where the Clock and Bias board is located controls the clock. The nominal frequency of this system clock is 40.0 MHz and events are synchronized to the positive transition of the clock.

All bus transactions on the sequencer bus and destined for the Clock and Bias board are accompanied by the board **/SEL** signal (J1:E5) going true for the duration of the transaction. There is a corresponding /ACK signal (J1:A6) that is currently not used.

1.2.1.2 Sequencer Bus Interface

All data and control transactions involving the Clock and Bias board are performed via the Sequencer Bus. There are four basic transaction types to control the board. They are described in more detail in the DHE backplane description document (ICD 7.0). The four transactions are reset, write 32-bit data, write 16-bit data, and read data (all reads are 32-bit). Bus activity is synchronous and timed to the rising edge of the board clock.

The Sequencer Bus is made up from four groups of signals: eight board select signals (**/SEL2 => /SEL8**), two bits of mode (**SEQ_MODE [1:0]**), six bits of device address (**DEV_ADDR [5:0]**), and thirty two bits of data (**SEQ_DATA [31:0]**).

The board select bits (**/SEL2 => /SEL8**) are used to activate a board for a bus transaction. Each slot of a CPCI backplane has a unique signal line that comes from the master slot. The actual signal that selects the board will depend on which backplane slot the board is physically located in. It is legal for multiple board select lines to be active for either a reset or write transaction, however; only a single board select can be active for a read transaction.

The **SEQ_MODE [1:0]** signals define the four types of bus transactions and are detailed in Table 1.

Table 1 - Sequencer Bus Mode Bit Definitions

Mode	Transaction	Mode	Description
00	Reset	Hard or Soft	Reboot FPGA or soft reset the addressed board depending on **SEQ_DEVADDR** bits.
01	Read	32 bits	Read a word from the addressed board.
10	Write	16 bits	Write a 16-bit word to the addressed board.
11	Write	32 bits	Write a 32-bit word to the addressed board.

NOTE: A reset or write transaction takes one clock cycle to complete. A read transaction occupies three clock cycles.

Reset transactions:
Reset mode timing is similar to a write transaction.

If all bits of the **SEQ_DEVADDR [5:0]** signals are high, the board will reboot the firmware of FPGA and all configuration data is set to their default values. Approximately 30 milliseconds are required after a power cycle or reboot command before the board becomes functionally active.

If all bits of the **SEQ_DEVADDR [5:0]** signals are low during a reset transaction, the board performs a 'soft reset' where only functionality is reset (i.e., state machines, etc.). Current configuration data is preserved.

Read transactions:
During a read transaction, the board interprets the required address from the least significant 16 bits of the sequencer bus signals (**SEQ_DATA [15:0]**) while the board select signal (**/SEL**) is true. One bus clock cycle later, the data from the decoded address is placed on the pixel data bus. On the next bus clock cycle, the MCB latches this data and the board releases the pixel data bus. The board select signal remains true for the complete three clock cycle period.

Write transactions:
By specification, only the lowest sixty-four memory locations (0x0000 => 0x003F) of a peripheral board can be written using the 32-bit mode. In 32-bit write mode, the **SEQ_DEVADDR [5:0]** signals define the address information to the board. Data is defined on signals **SEQ_DATA [31:0]**. The data is written into the appropriate register of the board on the rising edge of the bus clock when the board select signal is true.

When a 16-bit write transaction takes place, the address is defined by the most significant 16 bits of the sequencer data bus (**SEQ_DATA [31:16]**) signals and data is defined by the least significant sequencer data bus bits (**SEQ_DATA [15:0]**). The timing is equivalent to the 32-bit mode.

An additional signal is defined in the sequencer bus interface specification called the Acknowledge Strobe (**/ACK2 => /ACK8**). This signal is not used in this implementation.

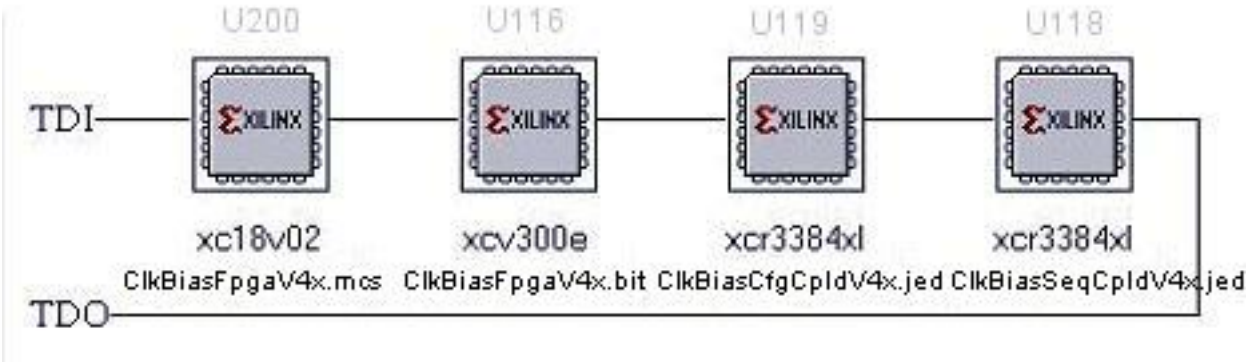
1.2.1.3 Pixel Data Bus Interface

The Pixel Data Bus (**PIX_DATA [47:0]**) exists to transfer data from peripheral boards to the MCB and from there to the PAN via the Systran link. It is a unidirectional 48-bit bus that connects to a 128-word FIFO (Pixel Bus FIFO) within the MCB pixel FPGA. The bus width allows three 16-bit, two 24-bit, or one 32-bit data value to be transferred to the MCB in one clock cycle. The Clock and Bias board supports single 32-bit transfers.

In the read mode, when responding to a read transaction, 32-bit data is latched into the MCB on the rising edge of the bus clock when commanded to do so by the MCB sequencer FPGA. This mode of operation (normal mode) is used exclusively to read individual addresses (registers) of the board under command of the PAN. All timing is controlled by the MCB firmware logic and results in three bus clock cycles being required for each 32-bit data value read.

1.2.2 JTAG Interface, Reset and Power on Boot.

The JTAG order is: J6:**TDI** => U200 FPGA boot EEPROM (type 18V02) => U116 Clock and Bias control FPGA (type Virtex300E) => U119 configuration control CPLD (type XCR3384) => U118 Clock and Fast Bias control CPLD for channels 4,5,6,7 (type XCR3384) => J6:**TDO**. Figure 2 illustrates a typical JTAG Pod view of the chain.



JTAG Device Ordering
Figure 2

The FPGA boot EEPROM at U200 is programmed via the JTAG interface with the configuration data for the Clock and Bias control FPGA. This configuration data is automatically sent to the FPGA whenever a boot operation is performed. The interface can also be used to read the checksum of the EEPROM contents against a known value for each firmware version.

The Virtex300E programmable logic device at U116 (Clock and Bias control) contains all essential timing and interface logic for the Clock and Bias board to function on the backplane. Code stored in the FPGA boot EEPROM is loaded to this device during power up, when the front panel reset switch is used or during a board reboot command from the PAN. The time to boot the code and perform power up initialization is approx. 30 milliseconds. It is normally not necessary to configure this device through the JTAG interface. The interface can however, be used to verify that the correct configuration is loaded to the FPGA during a boot. In addition, the JTAG interface can be used to read back the 'User Code' stored into the FPGA at boot time to verify the correct version and build date. The FPGA firmware configuration establishes the logic functionality of the entire Clock and Bias board and the interface to the MONSOON backplane.

The Xilinx Coolrunner CPLDs at U119 and U118 are static devices that retain their programmed functions during power cycles. U118 is a sequencer clock CPLD that provides a clock state register and fast bias control logic. U119 is a configuration CPLD that provides serial configuration streams, serial telemetry streams and auxiliary functions including OUTPUT ENABLE. In this way the device is programmed once through the JTAG interface and is functional immediately after any power or reset cycle. These devices are reset by any reboot operation performed on the circuit board. The checksum of these devices can be read back through the interface to verify that the correct firmware version is loaded.

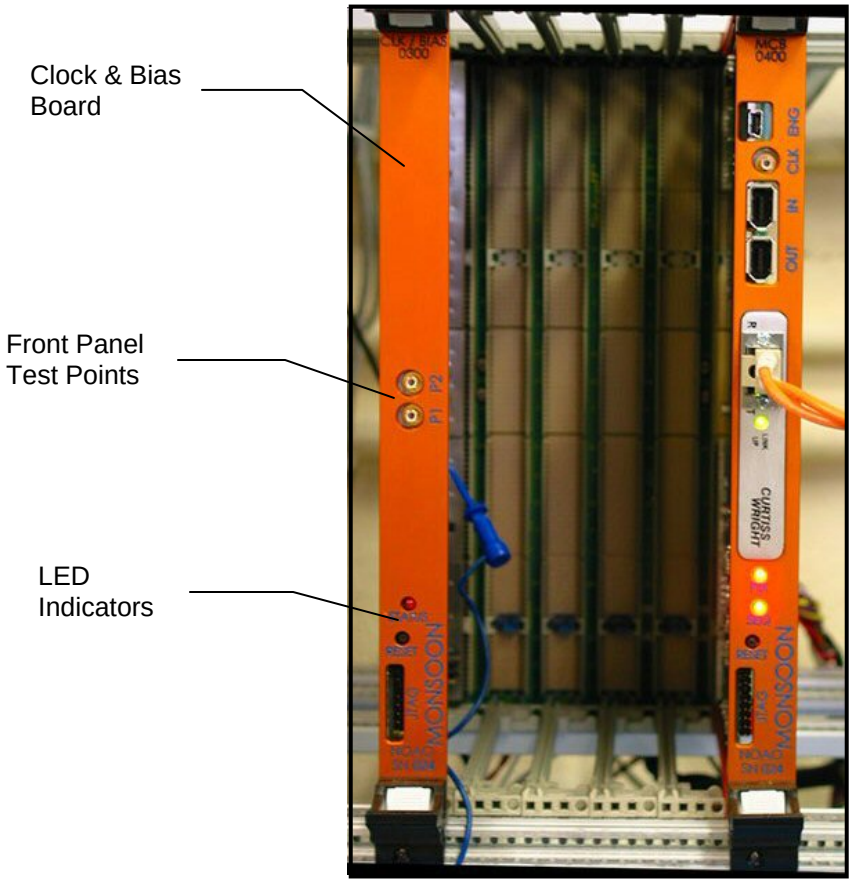
1.2.3 Front Panel Indicators

There is a front panel LED indicator (D1) used for basic diagnostics of the board. D1 is controlled by firmware in the Clock and Bias control FPGA. See Figure 3.

During power up, the indicator is off until the firmware has been booted and started. After booting, the indicator will be steadily on until a valid bus transaction is received from the MCB (Board clock must be enabled + a read or write command transaction preformed). At this time, the indicator will extinguish until programmed to indicate some functionality through the associated control register (CLK_LEDCTL). For version 4.1x FPGA firmware, Table 2 lists the functionality that is provided.

Table 2 - Front Panel Indicator Functions

CCD_LEDCTL	
BIT	**Function**
0	CLK Board Select Signal Active
1	Not used - always ON
2	Not used - always OFF



Clock and Bias Board Front Panel
Figure 3

1.2.4 Front Panel Test Points

P1 and P2 each provide access to any of the 32 clock signals by way of independent multiplexers (CLK_P1_SLCT, CLK_P2_SLCT). The buffered output signal can be used to monitor the clock signal or to provide oscilloscope synchronization for other signals. See Figure 3 for test point locations. Instructions for programming these test points are presented in Appendix II.

1.2.5 PCI Connectors J3, J4 and J5

These three hard metric connectors form the analog signal interface between the Clock and Bias board and the detector(s) of an instrument.

J3 provides for clean analog power supplies and analog ground references to be connected. The specifications for J3 are contained in the document 'ICD 7.0 DHE Backplane Definition' (MNSN-AD-01-0006_V13). These specifications are shown in Table 4 for convenience.

Table 3 - J3 Connector Pinout Description

Pin	Z	A	B	C	D	E	F
19	AGND	+Vaux	+Vaux	+Vaux	+Vaux	+Vaux	AGND
18	AGND	-Vaux	-Vaux	-Vaux	-Vaux	-Vaux	AGND
17	AGND	+/-Vaux Return	+/-Vaux Return	+/-Vaux Return	+/-Vaux Return	+/-Vaux Return	AGND
16	AGND	+16.5VA	+16.5VA	+16.5VA	+16.5VA	+16.5VA	AGND
15	AGND	+/-16.5VA Return	+/-16.5VA Return	+/-16.5VA Return	+/-16.5VA Return	+/-16.5VA Return	AGND
14	AGND	-16.5VA	-16.5VA	-16.5VA	-16.5VA	-16.5VA	AGND
13	AGND	-6.5VA	-6.5VA	-6.5VA	-6.5VA	-6.5VA	AGND
12	AGND	+/-6.5VA Return	+/-6.5VA Return	+/-6.5VA Return	+/-6.5VA Return	+/-6.5VA Return	AGND
11	AGND	+6.5VA	+6.5VA	+6.5VA	+6.5VA	+6.5VA	AGND
10	AGND	Chassis GND	Chassis GND	Chassis GND	Chassis GND	Chassis GND	AGND
9	AGND	+5VA	+5VA	+5VA	+5VA	+5VA	AGND
8	AGND	+/-5VA Return	+/-5VA Return	+/-5VA Return	+/-5VA Return	+/-5VA Return	AGND
7	AGND	-5VA	-5VA	-5VA	-5VA	-5VA	AGND
6	AGND	-15VA	-15VA	-15VA	-15VA	-15VA	AGND
5	AGND	+/-15VA Return	+/-15VA Return	+/-15VA Return	+/-15VA Return	+/-15VA Return	AGND
4	AGND	+15VA	+15VA	+15VA	+15VA	+15VA	AGND
3	AGND	+/- HV Return	+/- HV Return	+/- HV Return	+/- HV Return	+/- HV Return	AGND
2	AGND	-HV	-HV	-HV	-HV	-HV	AGND
1	AGND	+HV	+HV	+HV	+HV	+HV	AGND

NOTE: +/-Vaux is reserved for auxiliary power.

NOTE: +/-HV is a user-defined high voltage power supply, nominally +/-30V.

Connector J4 provides clock outputs and shutdown.

The **/SHUTDOWN** signal is provided as an input to the Clock and Bias board to allow supply and/or critical condition monitoring circuitry on a transition board to isolate the detector. Taking this signal true will open all the bias and clock output enable switches from the Clock and Bias board and isolate the detector from these supplies.

The pinout of the J4 connector is provided in Table 5.

Table 4 - J4 Connector Pinout Description

Pin	Z	A	B	C	D	E	F
25	AGND	AGND	AGND	AGND	AGND	AGND	N/C
24	AGND	CLKOUT10	N/C	CLKOUT21	/SHUTDWN	N/C	N/C
23	AGND	AGND	AGND	AGND	AGND	AGND	N/C
22	AGND	CLKOUT9	N/C	CLKOUT20	NC	CLKOUT31	N/C
21	AGND	AGND	AGND	AGND	AGND	AGND	N/C
20	AGND	CLKOUT8	N/C	CLKOUT19	NC	CLKOUT30	N/C
19	AGND	AGND	AGND	AGND	AGND	AGND	N/C
18	AGND	CLKOUT7	N/C	CLKOUT18	NC	CLKOUT29	N/C
17	AGND	AGND	AGND	AGND	AGND	AGND	N/C
16	AGND	CLKOUT6	N/C	CLKOUT17	NC	CLKOUT28	N/C
15	AGND	AGND	AGND	AGND	AGND	AGND	N/C
11	AGND	CLKOUT5	N/C	CLKOUT16	NC	CLKOUT27	N/C
10	AGND	AGND	AGND	AGND	AGND	AGND	N/C
9	AGND	CLKOUT4	N/C	CLKOUT15	NC	CLKOUT26	N/C
8	AGND	AGND	AGND	AGND	AGND	AGND	N/C
7	AGND	CLKOUT3	N/C	CLKOUT14	NC	CLKOUT25	N/C
6	AGND	AGND	AGND	AGND	AGND	AGND	N/C
5	AGND	CLKOUT2	N/C	CLKOUT13	NC	CLKOUT24	N/C
4	AGND	AGND	AGND	AGND	AGND	AGND	N/C
3	AGND	CLKOUT1	N/C	CLKOUT12	NC	CLKOUT23	N/C
2	AGND	AGND	AGND	AGND	AGND	AGND	N/C
1	AGND	CLKOUT0	N/C	CLKOUT11	NC	CLKOUT22	N/C

Connector J5 provides the interface to the 36 output channels of high voltage bias (**BIAS[31:0]**). It also accepts a remote shutdown signal (**/SHUTDOWN**) to open all the isolation switches for biases.

Bias voltages have an output range of 12.5 Volts and can be configured for either unipolar 0v => 12.5v unipolar or bipolar +/- 12.5v. These ranges are determined by hard configuring reference voltage jumpers on the Clock and Bias board.

Table 5 - J5 Connector Pinout Description

Pin	Z	A	B	C	D	E	F
22	AGND	BIAS11	BIAS23	BIAS35	N/C	N/C	N/C
21	AGND	AGND	AGND	AGND	AGND	AGND	N/C
20	AGND	BIAS10	BIAS22	BIAS34	N/C	N/C	N/C
19	AGND	AGND	AGND	AGND	AGND	AGND	N/C
18	AGND	BIAS9	BIAS21	BIAS33	N/C	N/C	N/C
17	AGND	AGND	AGND	AGND	AGND	AGND	N/C
16	AGND	BIAS8	BIAS20	BIAS32	N/C	N/C	N/C
15	AGND	AGND	AGND	AGND	AGND	AGND	N/C
14	AGND	BIAS7	BIAS19	BIAS31	N/C	FBIAS7	N/C
13	AGND	AGND	AGND	AGND	AGND	AGND	N/C
12	AGND	BIAS6	BIAS18	BIAS30	N/C	FBIAS6	N/C
11	AGND	BIAS5	BIAS17	BIAS29	N/C	FBIAS5	N/C
10	AGND	AGND	AGND	AGND	AGND	AGND	N/C
9	AGND	BIAS4	BIAS16	BIAS28	N/C	FBIAS4	N/C
8	AGND	AGND	AGND	AGND	AGND	AGND	N/C
7	AGND	BIAS3	BIAS15	BIAS27	N/C	FBIAS3	N/C
6	AGND	AGND	AGND	AGND	AGND	AGND	N/C
5	AGND	BIAS2	BIAS14	BIAS26	N/C	FBIAS2	N/C
4	AGND	AGND	AGND	AGND	AGND	AGND	N/C
3	AGND	BIAS1	BIAS13	BIAS25	N/C	FBIAS1	N/C
2	AGND	AGND	AGND	AGND	AGND	AGND	N/C
1	AGND	BIAS0	BIAS12	BIAS24	N/C	FBIAS0	N/C

1.3 Data Paths

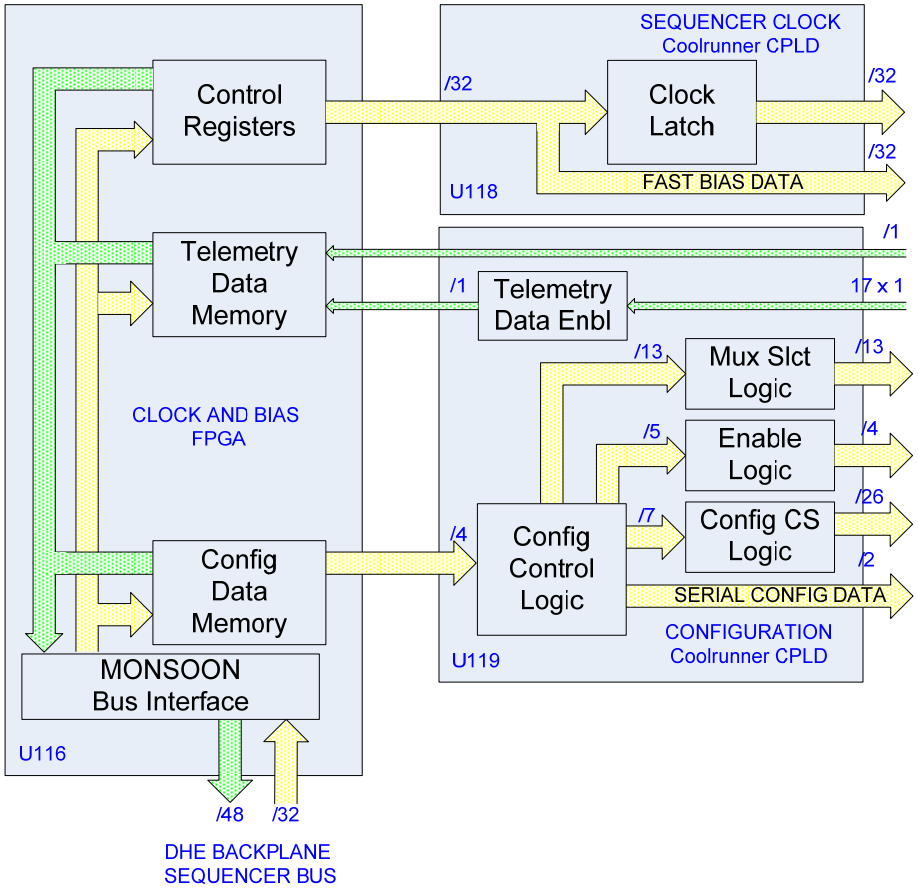
There are three principle data paths associated with the functions of the Clock and Bias board: Control data path, Configuration data path, and Pixel data path. See Figure 4 for a graphic representation of these data paths.

1.3.1 Control Data

All control functions are performed using an on-board flat memory (register) address space to provide read and write access to control registers located in the Clock and Bias interface FPGA. Generally, the data width of these registers is 16 bits. A few control registers in the lower address space area are 32-bit values. Values written to the registers establish the modes of operation and the synchronization of events.

1.3.2 Configuration Data

Configuration data is transmitted to the relevant hardware devices through a common synchronous serial link. The serial data stream is generated by the FPGA, fed to U119 CPLD where the address of the device is decoded and serial data distributed to the individual hardware component.



Clock and Bias Board Principal Data Paths
Figure 4

1.4 Control Functions

All control and acquisition functions that the Clock and Bias board is capable of are initiated by writing to specific memory locations on the board. There are two parts to forming the 24-bit address to these memory locations. They are the 'board select address' (or slot address), and the 'board register address'.

The 8-bit board select address is defined by the physical position of the Clock and Bias board on the DHE backplane. By definition, the Master Control Board (MCB) always occupies board select address 1 and occupies slot 1 of the backplane. Slot positions are numbered from the MCB position in linear fashion up to a maximum of slot 8. Board select addresses are expressed as bit positions in the command word address field during a PAN ⇔ DHE command transaction. See document ICD 6.1 DHE Command and Hardware Interface Definition for additional information. This mechanism allows multiple boards to be accessed in any write or reset transaction. In a similar fashion, the 8-bit board select address is written to the LSR register in the MCB Sequencer register set to access the peripheral boards. Table 7 defines the board select address with respect to the slot position.

Table 6 - Sequencer Bus Address Mapping

Slot Position	Board Select Address	32-Bit Word on Board Register Address Range	16-Bit Word on Board Register Address Range
1	0x010000	0x010000 => 0x01003F	0x010040 => 0x01FFFF
2	0x020000	0x020000 => 0x02003F	0x020040 => 0x02FFFF
3	0x040000	0x040000 => 0x04003F	0x040040 => 0x04FFFF
4	0x080000	0x080000 => 0x08003F	0x080040 => 0x08FFFF
5	0x100000	0x100000 => 0x10003F	0x100040 => 0x10FFFF
6	0x200000	0x200000 => 0x20003F	0x200040 => 0x20FFFF
7	0x400000	0x400000 => 0x40003F	0x400040 => 0x40FFFF
8	0x800000	0x800000 => 0x80003F	0x800040 => 0x80FFFF

The on-board register address of the Clock and Bias board is divided into two areas as indicated in the document ICD 7.0 DHE Backplane Definition. This allows sixty-four 32-bit registers to be defined in the lower board register address space. The rest of the space is occupied by sixteen bit registers. Thirty-two bit space is normally used for functions that are occupied by the MCB Sequencer.

A summary of the memory space for the Clock and Bias is given in Table 7 followed by a more detailed description of each function.

Table 7 - CLK Memory Map

Address	Function Name	Function Description
0x0000	CLK_CLKPORT	Sets the clock level (high/low) for the 32 clock signals
0x0001	CLK_FBIAS0123	Writes the Fast Bias signal DACS for channels 0,1,2, and 3 from the specified bank (0 => 15)
0x0002	CLK_FBIAS4567	Writes the Fast Bias signal DACS for channels 4,5,6, and 7 from the specified bank (0 => 15)
0x0040 => 0X004F	CLK_FBIAS_0	Banks 0=>15 of Fast Bias channel 0 values.
0x0050 => 0X005F	CLK_FBIAS_1	Banks 0=>15 of Fast Bias channel 1 values.
0x0060 => 0X006F	CLK_FBIAS_2	Banks 0=>15 of Fast Bias channel 2 values.
0x0070 => 0X007F	CLK_FBIAS_3	Banks 0=>15 of Fast Bias channel 3 values.
0x0080 => 0X008F	CLK_FBIAS_4	Banks 0=>15 of Fast Bias channel 4 values.
0x0090 => 0X009F	CLK_FBIAS_5	Banks 0=>15 of Fast Bias channel 5 values.
0x00A0 => 0X00AF	CLK_FBIAS_6	Banks 0=>15 of Fast Bias channel 6 values.
0x00B0 => 0X00BF	CLK_FBIAS_7	Banks 0=>15 of Fast Bias channel 7 values.
0x0100 => 0X0123	CLK_BIASPORT	Bias DAC registers for channels 0 thru 35
0x0124 => 0X0143	CLK_LOWPORT	Clock rail low state voltage DAC registers for channels 0 thru 31
0x0144 => 0X0163	CLK_HIGHPORT	Clock rail high state voltage DAC registers for channels 0 thru 31
0x016E	CLK_GLOBAL_ENBL	Enables or isolates all clock and bias signals to the back plane connector
0x016F	CLK_MUXSLCT	Selects which clock signals to be connected to the front panel test ports P1 and P2 and controls D5
0x0170 => 0x0193	CLK_TELBIASVMODE	Sets the telemetry data mode (ADC Mode) for Bias channels 0 through 35 to read voltage
0x0198 => 0x01BB	CLK_TELBIASIMODE	Sets the telemetry data mode (ADC Mode) for Bias channels 0 through 35 to read current
0x01C0 => 0X01DF	CLK_TELCLKMODE	Sets the telemetry data mode (ADC Mode) for Clock channels 0 through 31 to read voltage
0x01E0 => 0X01E7	CLK_TELFBIASMODE	Sets the telemetry data mode (ADC Mode) for Fast Bias channels 0 through 7 to read voltage
0x01E8 => 0X01EF	CLK_TELSUPPLYMODE	Sets the telemetry data mode (ADC Mode) for reading supply voltages
0x01F0 => 0X01F7	CLK_TELREFMODE	Sets the telemetry data mode (ADC Mode) for reading reference voltages
0x0270 => 0X0293	CLK_TELBIASVDATA	Telemetry data for Bias channels 0 through 35 to read bias voltage
0X0298 => 0X02BB	CLK_TELBIASIDATA	Telemetry data for Bias channels 0 through 35 to read bias current
0x02C0 => 0X02DF	CLK_TELCLOCKDATA	Telemetry data for Clock channels 0 through 31 to read clock voltage
0x02E0 => 0X02E7	CLK_TELFBIASDATA	Telemetry data for Fast Bias channels 0 through 7 to read bias voltage

Table 7 - CLK Memory Map (Cont.)

Address	Function Name	Function Description
0x02E8 => 0X02EF	CLK_TELSUPPLYDATA	Telemetry data for supply voltages
0x02F0 => 0X02F7	CLK_TELREFDATA	Telemetry data for reference voltages
0xFFF0	CLK_EVENT_REG	Global event register used to receive event strobes
0xFFF9	CLK_LEDCTL	Front panel LED indicator configuration register
0xFFFA	CLK_SERNUM	Electronic serial number read only register
0xFFFB	CLK_TEMP	Access to the local board temperature sensor
0xFFFC	CLK_CTLREG	Bit register used to control functionality of the board
0xFFFD	CLK_STATUSREG	Board status register
0xFFFE	CLK_IDENTREG	Board function identity register + shadow reset
0xFFFF	CLK_FIRMVERS	Board firmware version register + shadow reboot
0xFFFE	CLK_RESET	Writing to this location causes a soft reset of the board. Does not affect configuration data
0xFFFF	CLK_REBOOT	Writing to this location causes a hard reset (reboot) of the board with default configuration values

1.4.1 Clock Control Register (CLK_CLKPORT – 0x0000)

Writing a 32 bit value to this register establishes the level of the 32 clock signals available on the P?? connector. Each bit of this register corresponds to one clock signal (Bit 0 = CLK00, Bit 1 = CLK01, etc.) of the connector. When a clock register bit is set high (1) then the voltage programmed by the corrosponding clock high level DAC (CLK_HIGHPORT DAC) is output on the clock signal. When a clock register bit is set low (0) then the voltage programmed by the corresponding clock low DAC register (CLK_LOWPORT) is output on the clock signal. Note that it is permissable for the clock low DAC register to be programmed with a higher voltage than the clock high DAC register. This feature allows "not clock" and P-Channel device clock signals to be generated using standard logic convention. Reading this register returns the current status of the clock bits. The register may be written to at anytime however, the Bias and Clock Enables Register (CLK_GLOBAL_ENBL) bit 3 must be set true to enable the Clock signals to the output on J4.

1.4.2 Fast Bias Index Registers (CLK_FBIAS0123 – 0x0001 & CLK_FBIAS4567 – 0x0002)

These two 32-bit registers are used to change the voltages of the fast bias signals available on the J5 connector. CLK_FBIAS0123 controls Fast Bias channel group 0 through to 3. CLK_FBIAS4567 controls channel group 4 through to channel 7. Although these registers are within the 32 bit address space, only the least significant 4 bits of each register is used. A 4 bit value written to these registers is used as an index to identify one of sixteen Fast Bias DAC Bank Registers (CLK_FBIAS_n) where a value for the DAC has been previously stored. In this way one of sixteen different combinations of the four grouped Fast Bias signals can be selected with one write transaction to the register. Reading these registers returns the last index value written. The registers may be written to at anytime however, the Bias and Clock Enables Register (CLK_GLOBAL_ENBL) bit 2 must be set true to enable the Fast Bias signals to the output on J5. Figure 5 shows the bit significance of this register.

Fast Bias Index Register
Figure 5

1.4.3 Fast Bias DAC Bank Registers (CLK_FBIAS_0 thru CLK_FBIAS_7)

CLK_FBIAS_0	0x0040=>0x004F
CLK_FBIAS_1	0x0050 => 0X005F
CLK_FBIAS_2	0x0060 => 0X006F
CLK_FBIAS_3	0x0070 => 0X007F
CLK_FBIAS_4	0x0080 => 0X008F
CLK_FBIAS_5	0x0090 => 0X009F
CLK_FBIAS_6	0x00A0 => 0X00AF
CLK_FBIAS_7	0x00B0 => 0X00BF

The total address space of 128 8-bit registers is logically divided into eight banks of 16 registers each. Each bank of 16 registers corresponds to one Fast Bias DAC and allows sixteen 8-bit values to be stored that represent the desired Fast Bias output voltages. Writing a 4-bit index value to the corresponding Fast Bias Index Register selects the appropriate voltage for the four Fast Bias DACs of that group and sets these values to the hardware that produces a voltage at the corresponding signal on connector J5. Reading these registers returns the value last written to them.

1.4.4 Bias Voltage DAC Registers (CLK_BIASPORT – 0x0100=>0x0123)

A total of thirty-six 8-bit registers are used to control the voltage of the Bias signals available on J5. Writing an 8-bit value to these registers immediately sets the value of the corresponding DAC and produces a voltage at the output signal. The registers may be written to at any time, however, the Bias and Clock Enables Register (CLK_GLOBAL_ENBL) bit 0 & 1 must be set true to enable the Bias signals to the output on J5. Reading these registers returns the value last written to them.

1.4.5 Clock Low Rail Voltage Registers (CLK_LOWPORT – 0x0124=>0x0143)

These thirty two 8-bit registers write directly to the clock low rail DACs and control the voltage set to the Clock ouput signals when the corresponding Clock Control Register bit is set false (0). Reading these registers returns the value last written to them.

1.4.6 Clock High Rail Voltage Registers (CLK_HIGHPORT - 0x0144=>0x0163)

These thirty two 8-bit registers write directly to the clock high rail DACs and control the voltage set to the Clock ouput signals when the corresponding Clock Control Register bit is set true (1). Reading these registers returns the value last written to them.

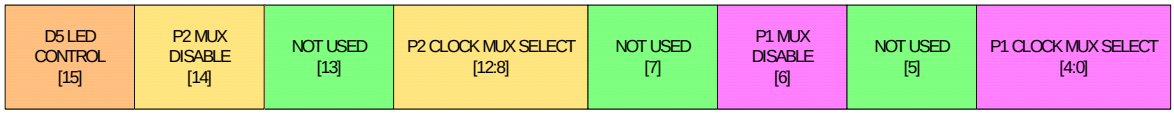
1.4.7 Bias and Clock Enables Register (CLK_GLOBAL_ENBL – 0x016E)

This 16-bit register controls the application (i.e. enabling) of bias, fast bias, and clock voltages to the rear connectors J4 and J5. Figure 6 shows the significance of the bits in this register. A bit set true in the register enables that group of voltages to the rear connector. Reading this register returns the value last written to it.

Bias and Clock Enables Register
Figure 6

1.4.8 Front Panel Clock Monitor Port Select Register (CLK_MUXSLCT – 0x016F)

Two front panel connectors (P1, P2) are provided to monitor the state of any of the 32 clock signals. These two buffered ports are independent and allow two clocks to be sampled simultaniously. This 16-bit register allows the selection of the clock signals multiplexed to P1 and P2. The signal available at these connectors is taken from the rear connector point and is therefore after the enable switches. This means that the clocks should be enabled to allow the clock signal to be monitored. The bit significance of this register is shown in Figure 7. In addition, the test LED (D5) can be controlled by the most significant bit of this register. The purpose of the LED is to test the basic serial configuration bus of the board. Control of this LED by writing to the register indicates that the basic serial configuration data bus (SDO, SCLK, U116, U119) is working. Since this bus is also used to control the setting of all DACs, the reading of all telemetry ADCs, and the control of the enable switches, this LED is important in any fault finding of the board. Reading this register returns the value last written to it.



Front Panel Clock Monitor Port Select Register
Figure 7

1.4.9 Bias Voltage Telemetry Mode Registers (CLK_TELBIASVMODE – 0x0170=>0x0193)

These thirty-six 16-bit registers allow the setting of the voltage range and mode of the telemetry channel ADC associated to the bias voltage telemetry functions. The nominal voltage of the ADC is 5v or 10v full scale. A resistor in series with the individual bias voltage signal (nominally 10K Ohms) acts in conjunction with the internal telemetry ADC voltage divider allowing the voltage range to be expanded to accommodate the bias voltage dynamic range. The mode bit is used to control the coding of the ADC to be either 12-bit twos-compliment bipolar or 12-bit unipolar depending on the voltage range set for the bias voltage signal by way of the voltage reference jumpers. Table 8 shows the bit significance of these registers. Note that depending on the mode and range selected the scale and offset values used in the attribute calculations require adjustment to accommodate the data. These registers are set by default to their normal values (0xD i.e. +/- 10V Range, external clock mode) after power on or reboot function. Reading these registers returns the value last written to them.

Table 8 – Bit Significance

MAX 1207 Mode Bit Significance			
Bit 3	**Bit 2**	**Bit 1**	**Bit 0 (LSB)**
RNG	BIP	PD1	PD0

PD1	PD0	Mode
0	0	Normal operation (always on) Internal clock mode
0	1	Normal operation (always on) External clock mode
1	0	Standby Power-Down Mode (STBYPD) Clock mode unaffected
1	1	Full Power-Down mode (FULLPD) Clock mode unaffected

Range and Polarity Selection for MAX 1207					
Input Range	**RNG**	**BIP**	**Negative Full Scale**	**Zero Scale (V)**	**Full Scale**
0 to 5V	0	0	-	0	V_{REF} 1.2207
0 to 10V	1	0	-	0	V_{REF} 2.4414
±5V	0	1	$-V_{REF}$ 1.2207	0	V_{REF} 1.2207
±10V	1	1	$-V_{REF}$ 2.4414	0	V_{REF} 2.4414

1.4.10 Bias Current Telemetry Mode Registers (CLK_TELBIASIMODE – 0x0198=>0x01BB)

Similar to the bias voltage telemetry mode registers, these 36 registers provide a way to set the bias current telemetry range and mode. Likewise, these registers are set by default to a value of 0xD (i.e. +/-10V, external clock) that provides for approximately +/- 200ma measurement range for each of the generated bias signals.

1.4.11 Clock Voltage Telemetry Mode Registers (CLK_TELCLKMODE – 0x01C0=>0x01DF)

These thirty-two mode registers perform the mode and range selection for those telemetry channels dedicated to clock signals. Similarly, these registers are set by default to the value of 0xD (i.e. +/-10V, external clock) and the range extended by a series resistor in the clock signal line.

1.4.12 Fast Bias Voltage Telemetry Mode Registers (CLK_TELFBIASMODE – 0x01E0=>0x01E7)

The eight registers provide the telemetry ADC mode and range settings for the fast bias channels. These registers are set by default to the value of 0xD (i.e. +/-10V, external clock) and the range extended by a series resistor in the fast bias signal line.

1.4.13 Supply Voltage Telemetry Mode Registers (CLK_TELSUPPLYMODE – 0x01E8=>0x01EF)

These eight registers provide the mode and range and range selection for those telemetry channels dedicated to monitor the power supplies. Similarly, these registers are set by default to the value of 0xD (i.e. +/-10V, external clock) and the range extended by a series resistor in the appropriate signal line.

1.4.14 Reference Voltage Telemetry Mode registers (CLK_TELREFMODE – 0x01F0=>0x01F7)

Finally, eight registers that enable the mode and range to be set for those telemetry channels dedicated to monitor the DAC and offset reference supplies. Similarly, these registers are set by default to the value of 0xD (i.e. +/-10V, external clock) but the range is not extended for these signals.

1.4.15 Bias Voltage Telemetry Data Registers (CLK_TELBIASVDATA – 0x0270=>0x0293)

These thirty-six registers are used to control the telemetry ADC devices and obtain a telemetry data value representative of the voltage value for the selected bias channel. To read a value from the telemetry ADC you must first write a value to the bias channel address that you desire to read. The actual data value written is not significant and only serves to trigger an ADC conversion cycle. After approximately 30us the data value is available to be read from the same location.

1.4.16 Bias Current Telemetry Data Registers (CLK_TELBIASIDATA – 0x0298=>0x02BB)

These thirty-six registers are used to control the telemetry ADC devices and obtain a telemetry data value representative of the current draw on the selected bias channel. To read a value from the telemetry ADC you must first write a value to the bias channel address that you desire to read. The actual data value written is not significant and only serves to trigger an ADC conversion cycle. After approximately 30us the data value is available to be read from the same location.

1.4.17 Clock Voltage Telemetry Data Registers (CLK_TELCLOCKDATA – 0x02C0=>0x02DF)

These thirty-two registers are used to control the telemetry ADC devices and obtain a telemetry data value representative of the voltage value for the selected clock channel. To read a value from the telemetry ADC you must first write a value to the bias channel address that you desire to read. The actual data value written is not significant and only serves to trigger an ADC conversion cycle. After approximately 30us the data value is available to be read from the same location.

1.4.18 Fast Bias Voltage Telemetry Data Registers (CLK_TELFBIASDATA – 0x02E0=>0x02E7)

These eight registers are used to control the telemetry ADC devices and obtain a telemetry data value representative of the voltage value for the selected fast bias channel. To read a value from the telemetry ADC you must first write a value to the bias channel address that you desire to read. The actual data value written is not significant and only serves to trigger an ADC conversion cycle. After approximately 30us the data value is available to be read from the same location.

1.4.19 Power Supply Voltage Telemetry Data Registers (CLK_TELSUPPLYDATA – 0x02E8=>0x02EF)

These eight registers are used to control the telemetry ADC devices and obtain a telemetry data value representative of the voltage value for the selected power supply. To read a value from the telemetry ADC you must first write a value to the bias channel address that you desire to read. The actual data value written is not significant and only serves to trigger an ADC conversion cycle. After approximately 30us the data value is available to be read from the same location.

1.4.20 Reference Voltage Telemetry Data Registers (CLK_TELREFDATA – 0x02F0=>0x02F7)

These eight registers are used to control the telemetry ADC devices and obtain a telemetry data value representative of the voltage value for the selected reference supply. To read a value from the telemetry ADC you must first write a value to the bias channel address that you desire to read. The actual data value written is not significant and only serves to trigger an ADC conversion cycle. After approximately 30us the data value is available to be read from the same location.

1.4.21 Global Event Register (CLK_EVENT_REG – 0xFFF0)

The Global Events register is designed to provide a common and synchronized event signaling mechanism across all peripheral boards in a DHE chassis. Events can be issued by a PAN write to the appropriate board address or from the MCB sequencer. There are currently two such events defined. Table 13 lists the bit fields of this register.

Table 9 - Global Event Register Bit Fields

Bit	Event Name	Purpose
15	START_EXPOSURE	Issued at the beginning of a pixel acquisition that will result in a new image file being produced.
14:1		Not specified
0	START_FRAME	Issued at the beginning of a pixel acquisition cycle that will be used to build up the current image file.

NOTE: Currently these events are only used as an aid to function debugging i.e. to identify when such events have occurred.

1.4.22 Front Panel LED Control Register (CLK_LEDCTL – 0xFFF9)

The least significant three bits of this register control the function of the board front panel indicator LED (D1). This indicator provides base level diagnostic information on the functionality of the board. After power on or a reboot, the indicator will be on permanently until the first valid sequencer bus transaction has occurred. After this, writing to one or more of the control bits will provide a 10ms indicator flash each time the specific function goes true. The functions that can be assigned as triggers to illuminate this LED are listed in Table 10.

Table 10 - LED Indicator Function Codes

CLK_LEDCTL	
Bit	**Function**
0	Flash each time the board is selected on the sequencer bus (**/SEL**)
1	Not Used.
2	Not Used.

1.4.23 Silicon Serial Number Register (CLK_SERNUM – 0xFFFA)

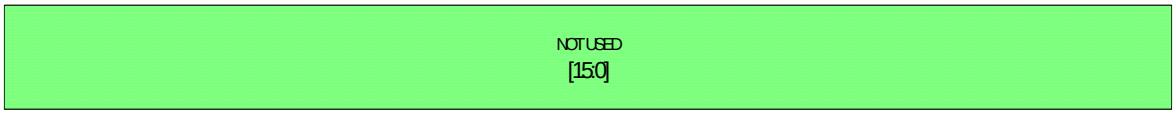
Reading this register returns a 32-bit word that is a unique serial number read from U110.

1.4.24 Board Temperature Register (CCD_TEMP – 0xFFFB)

Reading this register returns a 10-bit signed number that indicates the current ambient temperature of device U199. This is representative of the operating temperature of the board. Each LSB corresponds to 0.25deg. C. The temperature is read from U199 by first writing to this register with non-significant data, then waiting for at least 35 microseconds before reading the register that contains the new value.

1.4.25 Board Control Register (CLK_CTLREG – 0xFFFC)

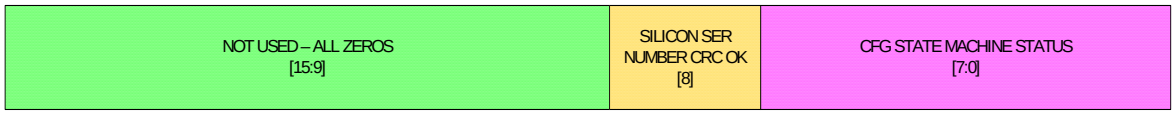
This 16-bit register controls the major mode of operation of the board. Figure 8 details the relevant bit fields of this register. The current firmware does not use this register.



Board Control Register Bit Fields
Figure 8

1.4.26 Board Status Register (CLK_STATREG – 0xFFFD)

This read only 16-bit register contains status information from various functions on the board FPGA. Bit significance is shown in Figure 9.



Board Status Register
Figure 9

1.4.27 Board Identity Code Register (CLK_IDENTREG – 0xFFFE) (CLK_RESET – 0xFFFE)

Reading from this address will return data that identifies this board as a Clock and Bias Board (Code = 0x012C, Decimal 300).

Writing to this address will result in the board going through a soft reset cycle. Current configuration data will not be affected and all state machines will be reset to their idle state.

1.4.28 Firmware Code Revision Register (CLK_FIRMVERS - 0xFFFF)(CLK_REBOOT – 0xFFFF)

Reading from this address will return data that will identify the version of firmware running on the board. The data is returned in fixed point decimal that should be divided by 100 to find the correct major and minor version number (XX.nn).

Writing to this address will result in the board going through a hard reset cycle. This will set to true the firmware signal TPS_RESET_N which results in a reloading of the firmware of the board FPGA. This will reset all configuration data to default power up values.

2.0 Board Hardware Description

Refer to drawing MNSN-EL-04-0008.

2.1 Power Supplies

There are eight power supplies required by the Clock and Bias board.

2.1.1 Digital Supplies

The majority of the logic is powered from a 3.3v supply (**+3.3VD**). This supply can be either supplied from the backplane (P1) or generated internally from the **+5VD** supply by U203. The jumpers JP9 and JP10 select the source for this supply. The internal logic cell of the FPGAs requires 1.8v (**+1.8v**) that is generated on board by U204. U204 is supplied internally from the **3.3VD** supply rail.

The +5VD digital supply is only used to supply the MAX1207 telemetry ADC devices. If an external **+3.3VD** supply is used, and no other MONSOON board requires the +5VD supply, then this supply can be strapped on the board to the analog +5VA supply.

2.1.2 Analog Power Supplies

The analog section requires +/-15v and +/-5v analog supplies with, at minimum, a ripple component to reduce noise feed through. These supplies are connected to the board by way of the backplane connector P3. The return current path for these supplies is by way of the circuit board ground plane, through the P1 and P2 connectors to the backplane. The analog power supplies should have their return grounds connected directly to the MONSOON DHE backplane star point; not to the P3 connector. Each power supply is locally fused and shunted by a bulk capacitor to supply local current demands.

CAUTION: **Do not use poly-silicon fuses on any supply since the impedance (and hence the voltage drop) for these devices with the required characteristics compromises the board performance.**

There is no specific order for the supplies to be turned on and no damage to the circuit can be done by unexpected application of power. However, the digital supplies should be sequenced first, then the +/-5va and finally the +/-15va supplies. This ensures that digital control is in place before the voltage generators are turned on and that the output amplifiers and signal isolation are enabled last.
Telemetry for the power supplies is provided for by U112. The series resistors (**TBD32**) extend the range of the MAX1270 device to accommodate the power supply voltages. The telemetry data are accessed through a write-to-read operation on the corresponding board register (**CLK_TELSUPPLYDATA**). The write operation to the address that specifies the register initiates an ADC conversion cycle on the addressed channel. After a 35 microsecond delay, the result of that conversion is available in the same register for analysis.
The nominal current drawn on these supplies are shown in Table 11.

Table 11 - Power Supply Current Draws

Digital Supply Rails	Quiescent	Peak
+5VD (with separate 3.3V supply)	0.60 Amp	1.0 Amp
+3.3VD	0.16 Amp	0.3 Amp
+1.8V		
Analog Supply Rails	**Quiescent**	**Peak**
+5VA	0.30 Amp	0.85 Amp
-5VA	0.01 Amp	0.25 Amp
+15VA	0.20 Amp	1.5 Amp
-15VA	0.20 Amp	1.5 Amp

2.2 Logic Section

2.2.1 Clock Generation

All operation of the logic on the board is controlled by and synchronous to the SYSCLK signal. This clock signal is sent through the PCI backplane from the Master Control Board (MCB). It is nominally 40MHz.

2.2.2 Reset and FPGA Boot Logic

A power-on reset active low signal is generated by the linear supply U204. This signal (**/TPS_RESET**) is asserted for 100ms after the core voltage becomes stable. When this signal is released, the FPGA device begins the boot process that involves sequencing the signals **/INIT** low then high, asserting **/DONE** false and supplying a clock to the **CCLK** pin. This resets the EEPROM (U200) internal address counter, enables the data output through D0 to the **EDAT** signal, and begins serially transferring the function code to the FPGA core. After the load sequence is complete, the FPGA takes the **DONE** signal high and executes an internal startup sequence that, finally, enables the output pins of the FPGA. This process takes approximately 30 ms to complete. The same process as a power on reset can be forced either by a PAN command (writing to the CLK_REBOOT register) or via the front panel switch SW1 which merely takes the **/RESET** signal low while activated and that is coupled internally to the FPGA to the same **/TPS_RESET** signal.

2.2.3 JTAG Interface

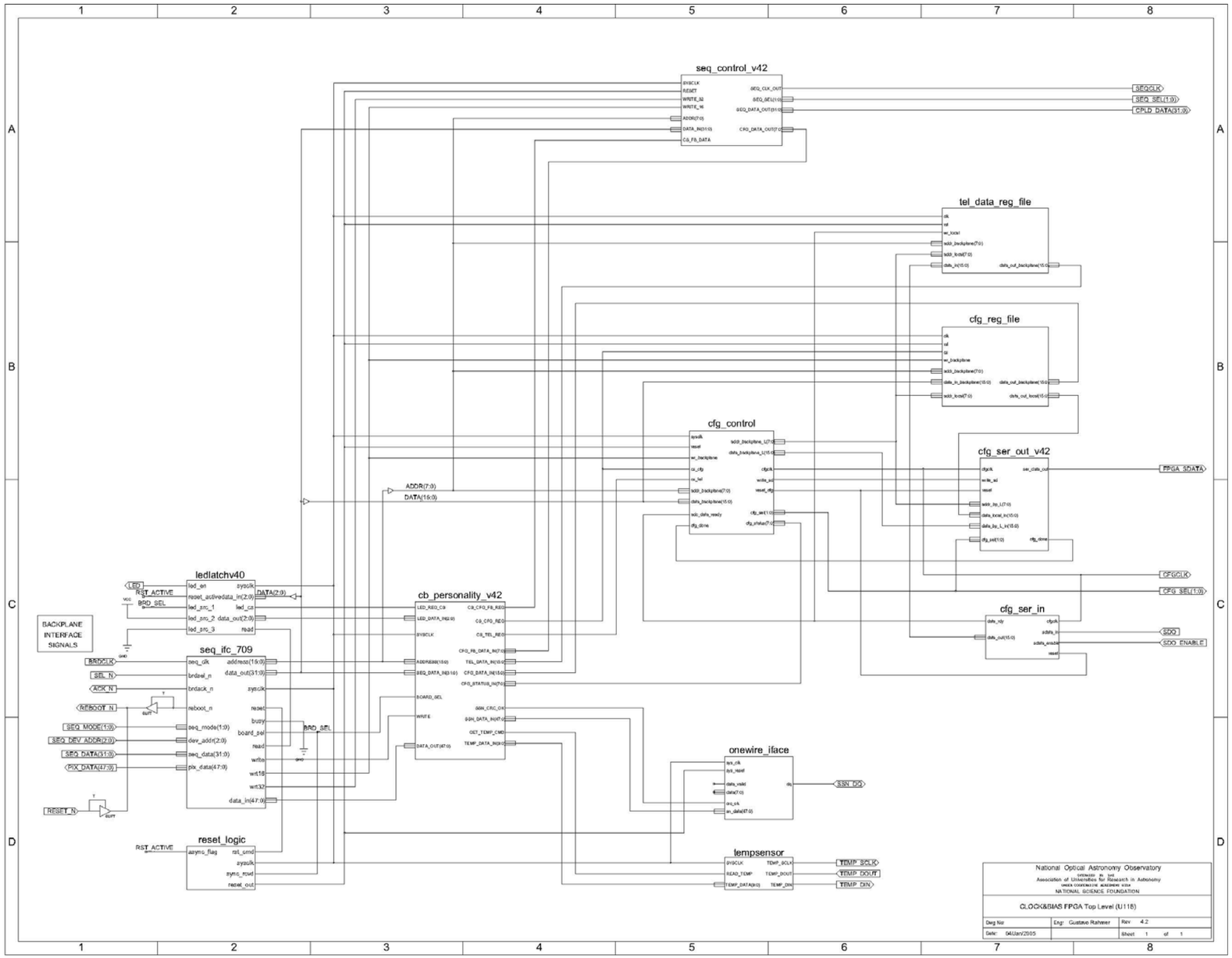
The front panel JTAG connector (J6) provides access to the boot EEPROM device, the FPGA, and the two CPLD devices. The front panel connector pin assignment is designed to mate on a one-to-one basis with most JTAG pod devices. See Table 12.

Table 12 - JTAG Pin Assignments

Pin	Function
1	+3.3VD
2	DGND
3	KEY
4	TCLK
5	N.C.
6	TDO
7	TDI
8	TMS

2.2.4 FPGA CPLD Communication Path

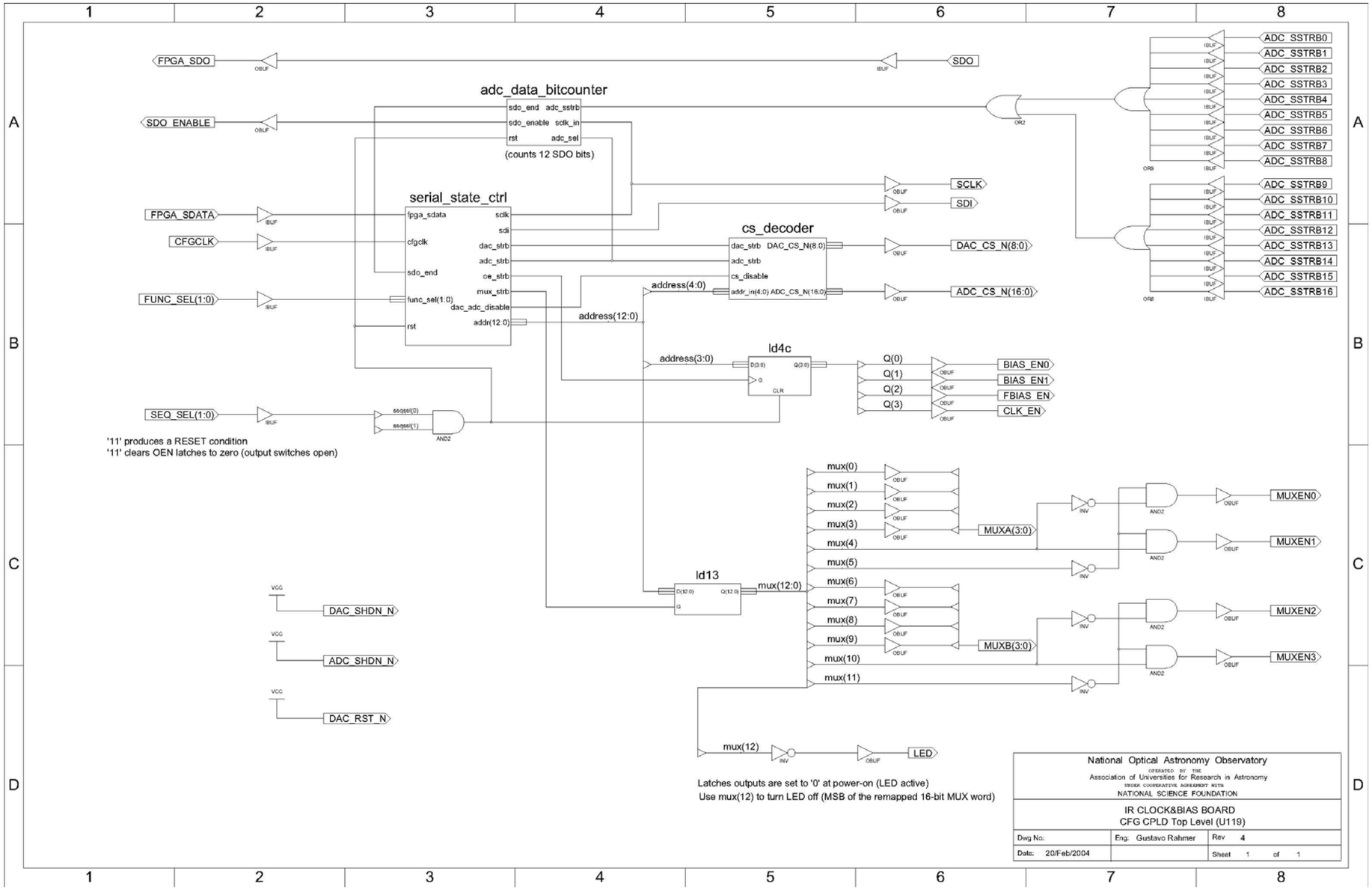
All logic processes are originated in the FPGA device at U116. The FPGA communicates to the two CPLD devices to complete certain functions.
The Configuration CPLD (U119) decodes and executes functions that are generally low speed / low priority processes. These functions configure and set the DAC devices, configure and read the telemetry devices and control the output enable switches and the clock select multiplexer.
The Sequencer Clock CPLD device (U118) contains logic that executes the higher speed functions of the board. These are the setting of the clock state switches and the control of the fast bias channels.
The communication path between the FPGA and the two CPLD devices is a simple 32-bit unidirectional bus driven by the FPGA. There are actually 36 physical traces laid out on the board but **DATA[32:35]** are not used by the current firmware.
Seven common control signals command the function to be performed by the CPLD devices. Again, there are actually 12 physical lands laid out on the board but **CPLDCTL[7:11]** are not used by the current firmware.
Two independent clock signals are used to synchronize events to the CPLD devices (**SYSCLK1** and **SYSCLK2**).
The signaling method on the bus and control signals is negative true to avoid false trigger events during the FPGA boot process time. See Figure 10.



FPGA (U116)
Figure 10

2.2.5 Configuration CPLD Logic

Device U119 (Figure 11) controls the functions used to set configuration and data to the DAC devices. It also incorporates functions to synchronize the data return from the telemetry ADC devices and generates latched signals for the control of the enable switches and clock multiplexer logic. The principle logic block of this design analyzes a serial data stream generated by the FPGA and decodes the correct chip select to direct the serial data to the correct device. Each command to set a DAC voltage or read a telemetry device is decoded in a similar manner.



U119 Configuration CPLD
Figure 11

The serial data stream is composed of a serial clock (**SYSCLK2**), the synchronous serial data stream (CPLDCT3), and a 2-bit function code **FUNCT_SEL[1:0]** mapped to signals **CPLDCTL5** and **CPLDCTL6**. The **SYSCLK2** signal has a nominal frequency of 1.25 MHz (**SYSCLK / 32**). The function codes are decoded to direct the serial data stream to the correct device group. The decoding is shown in Table 13.

Table 13 – Serial Data Stream Decoding

FUNC_SEL[1] CPLDCTL6	FUNC_SEL[0] CPLDCTL5	Firmware Function	Hardware Function
0	0	CLK_BIASPORT CLK_LOWPORT CLK_HIGHPORT	Write to a Voltage DAC device
0	1	CLK_TELBIASVDATA CLK_TELBIASIDATA CLK_TELCLOCKDATA CLK_TELFBIASDATA CLK_TELSUPPLYDATA CLK_TELREFDATA	Write to a Telemetry ADC device
1	0	CLK_GLOBAL_ENBL	Write to the Output Enables latch
1	1	CLK_MUXSLCT	Write to the Clock Multiplexer latch

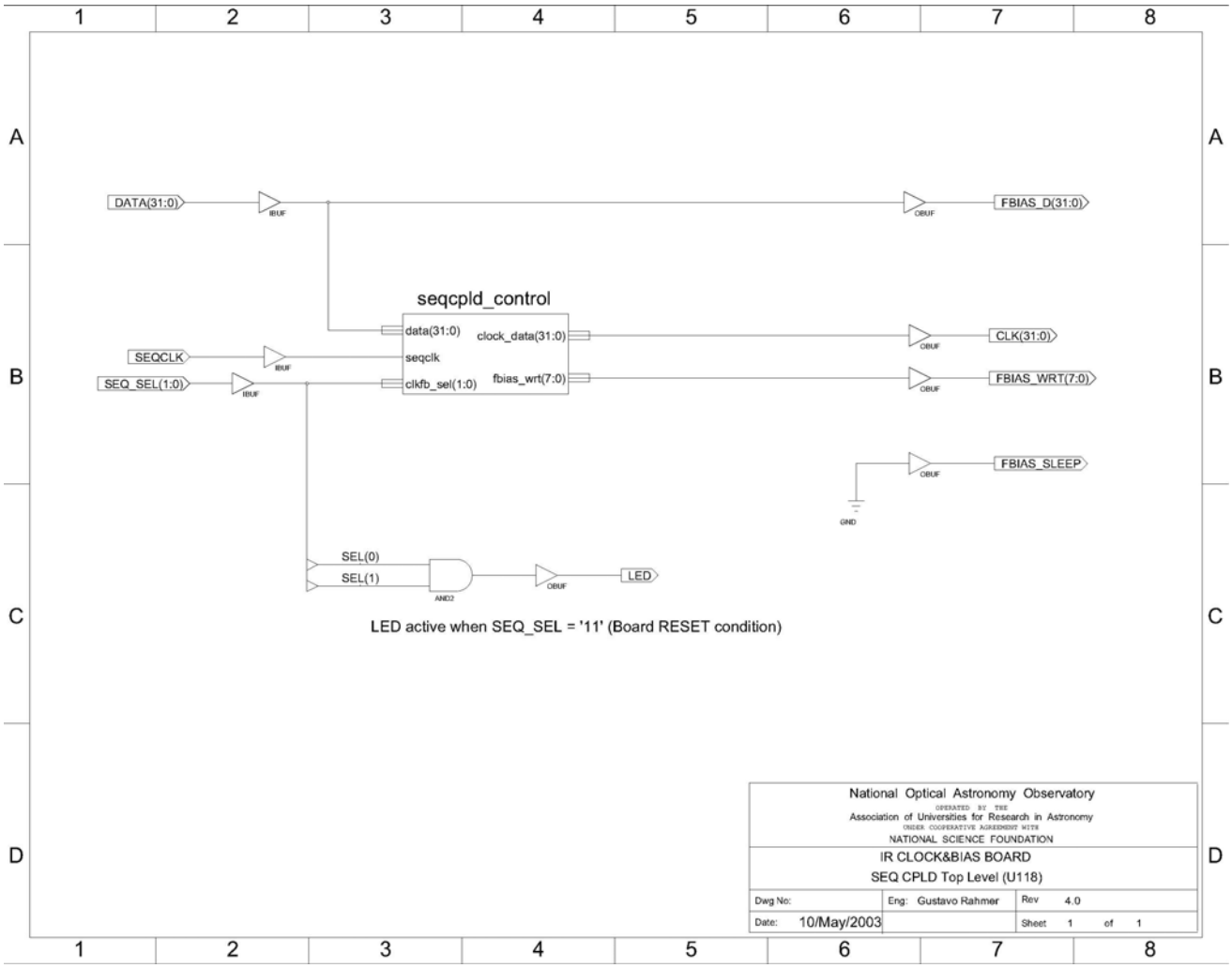
The serial data stream sent from the FPGA contains the address of the device and the channel number within the device. These data are decoded by the CPLD firmware and the correct chip select signal activated (**DAC_CS[0:8]**, **ADC_CS[0:16]**). The serial data stream is reformatted by the CPLD logic and re-emitted in the device dependent form by way of the signals **SDI** and **SCLK**. These signals can be monitored through test points **TP31** and **TP30**. Telemetry data returning from the ADC devices is received on the signal SDO (**TP32**) and retransmitted to the FPGA by way of signal **CPLDCTL2**. Logic internal to the CPLD frames the returned 12-bit data to create the signal data enable signal **CPLDCTL4** that is sent to the FPGA. The 2-bit **SEQ_SEL[1:0]** code common to both CPLD devices is monitored to detect a reset event. When this occurs, the Output Enables register is cleared. Table 13 defines this condition.

2.2.6 Sequencer Clock CPLD Logic

Device U118 (Figure 12) controls the latch to contain the clock port state and the write mechanism to load the fast bias DAC devices. Note that two write strobes are generated to the write fast bias DAC device data. The first loads the input register and the second transfers the latch data to the analog section. The routing of CPLD input data is a function of the **SEQ_SEL[1:0]** bits which are mapped to **CPLDCTL0** and **CPLDCTL1** signals. Table 14 shows the decode values.

Table 14 – Sequencer Clock CPLD Logic Values

SEQ_SEL[1] CPLDCTL1	**SEQ_SEL[0] CPLDCTL0**	Firmware Function	Hardware Function
0	0	CLK_CLKPORT	Write to Clock Port register
0	1	CLK_FBIAS0123	Write to fast bias channels 0, 1, 2, and 3
1	0	CLK_FBIAS4567	Write to fast bias channels 4, 5, 6, and 7
1	1	CLK_RESET	Board Reset Active



Sequencer Clock CPLD (U118)
Figure 12

Analog Sections:

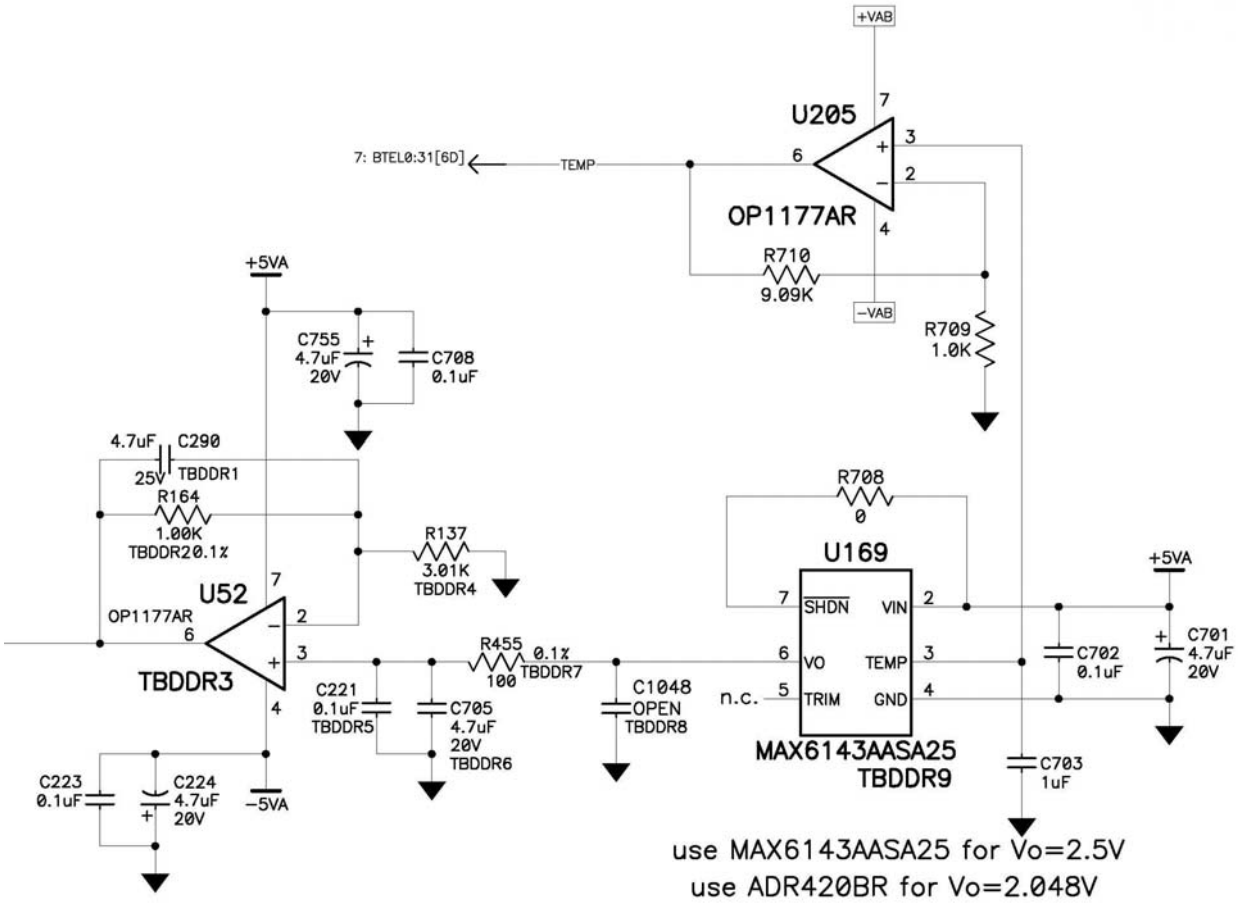
2.2.7 Reference Voltage Generators

There are two principal reference voltages generated for the analog circuitry: the DAC voltage reference and the offset voltage reference.

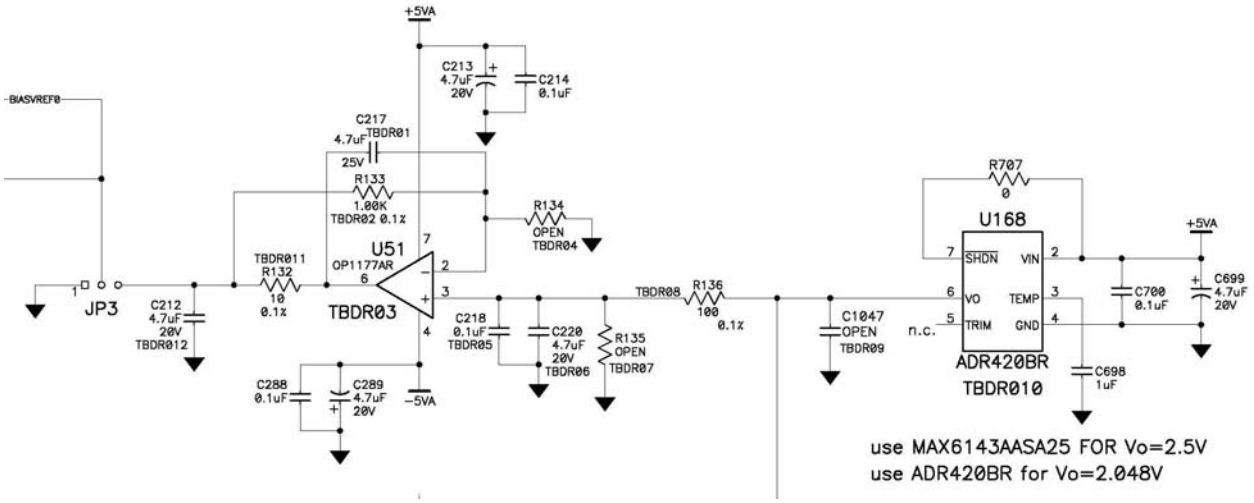
The DAC voltage reference is applied to all AD8802/MAS9187 devices and is normally set to +2.5v for the bias generators and 2.048v for the clock generators. U100, buffered by U195, supplies the DAC reference to the clock section. U195 has a nominal gain of 1.21. U169 buffered by U52 supplies this reference to the bias section with unity gain. Figure 13 shows the bias DAC reference voltage generator.

The offset voltage reference is used to bias the respective bias or clock output amplifiers so that bipolar operation is possible. These references are selected by jumpers on the individual signal groups. These references are injected into the inverting node of the bias or clock amplifiers to generate a negative offset at the output of the amplifier. U168 is the source for the bias signal groups. U92 is the source for the clock signal groups. These reference sources are normally set to 2.048v.

The 36 bias signals are divided into two groups to allow separate customization of the dynamic range of the two groups. U51 sets the offset reference voltage for the bias group 0:17. U31 sets the offset reference voltage for bias group 18:35. The offset reference is multiplied by the inverting gain of the bias amplifiers to set the most negative bias voltage required. These amplifiers have a nominal inverting gain of 5. With a 2.048v reference, this sets the negative bias voltage limit to –10.24v. Installing a gain resistor (**TBDR04** in schematic) and/or a shunt resistor (**TBDR07**) in the relevant offset reference buffer network allows setting of the most negative voltage of the bias signals to any desired value within the power supply range. Note that the amplifiers have a maximum input voltage rating relative to the power supply voltage. Figure 14 shows the typical offset reference voltage generator. U151 supplies a similar offset reference voltage to the fast bias amplifiers.
U91, U191, and U192 perform a similar role as offset reference voltage buffers for the three clock signal groups. The reference voltage values may be monitored through the corresponding telemetry channels (**CLK_TELREFDATA**). U101, a MAX1270 device, provides this functionality. The method of access is described in the power supply section.



Bias DAC Voltage Reference Generator
Figure 13



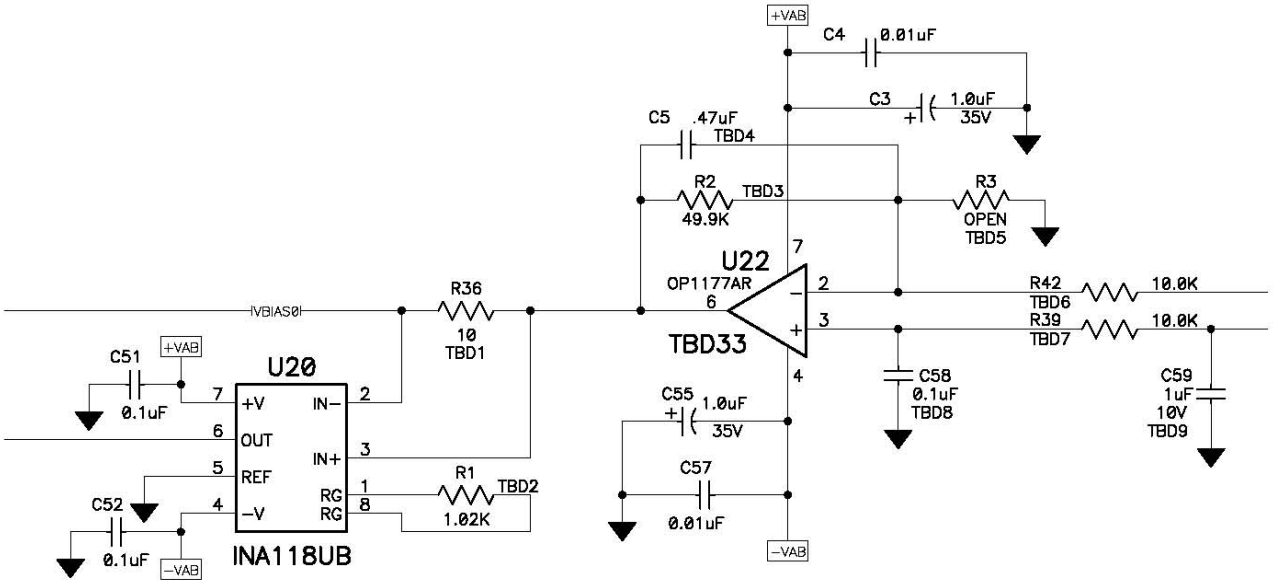
Typical Offset Reference Voltage Generator
Figure 14

2.2.8 Bias Voltage Generators

There are 36 channels of low voltage bias generators. These are divided into two groups of 18 biases each (**BIAS[0:17], BIAS[18:35]**). This allows the dynamic range of the two groups to be independently configured. This is achieved by selecting the offset reference voltage applied to the inverting node of the bias output amplifiers. Jumper JP3 controls the configuration for BIAS[0:17] and jumper JP1 controls **BIAS[18:35]**.

Shorting the jumper pins 1 to 2 sets the bias group to provide a positive unipolar dynamic range between 0v and (**BIASDACREF** x **GAIN**). Strapping pins 2 to 3 on these jumpers provides a bipolar dynamic range between (**BIASVREFN** x **INVGAIN**) and ((**BIASVREFN** x **INVGAIN**) + (**BIASDACREF** x **GAIN**)) for the bias group.

Each bias channel is controlled by the output of an 8-bit voltage DAC with an output range of 0v to **+BIASDACREF** (nominally 2.5v). The DACs are programmed to a value through firmware when the corresponding control register is written to. The output of each DAC is an unbuffered voltage with 5K Ohm source impedance. This voltage is filtered by a two stages of low order RC network and applied to the non-inverting input of the bias generator operational amplifier. The nominal non-inverting gain of this amplifier is six (6) set by the feedback resistor network (**TBD3, TBD5, TBD6**). For a board built with 'standard' specifications, this allows each bias signal to range between either 0v and 15v (with offset jumper shorted between pins 1 and 2) or between –10.24v and +4.75v. Wideband noise filtering for the individual bias signals is provided by the large capacitors in the feedback loop (TBD4). There is normally additional space on the transition boards for another low pass first order RC filter. For bias signals coupled to detector signals with high transconductance, additional filtering should be considered at the connection point to the detector. Figure 15 shows a typical bias generator circuit.



Typical Bias Generator Circuit
Figure 15

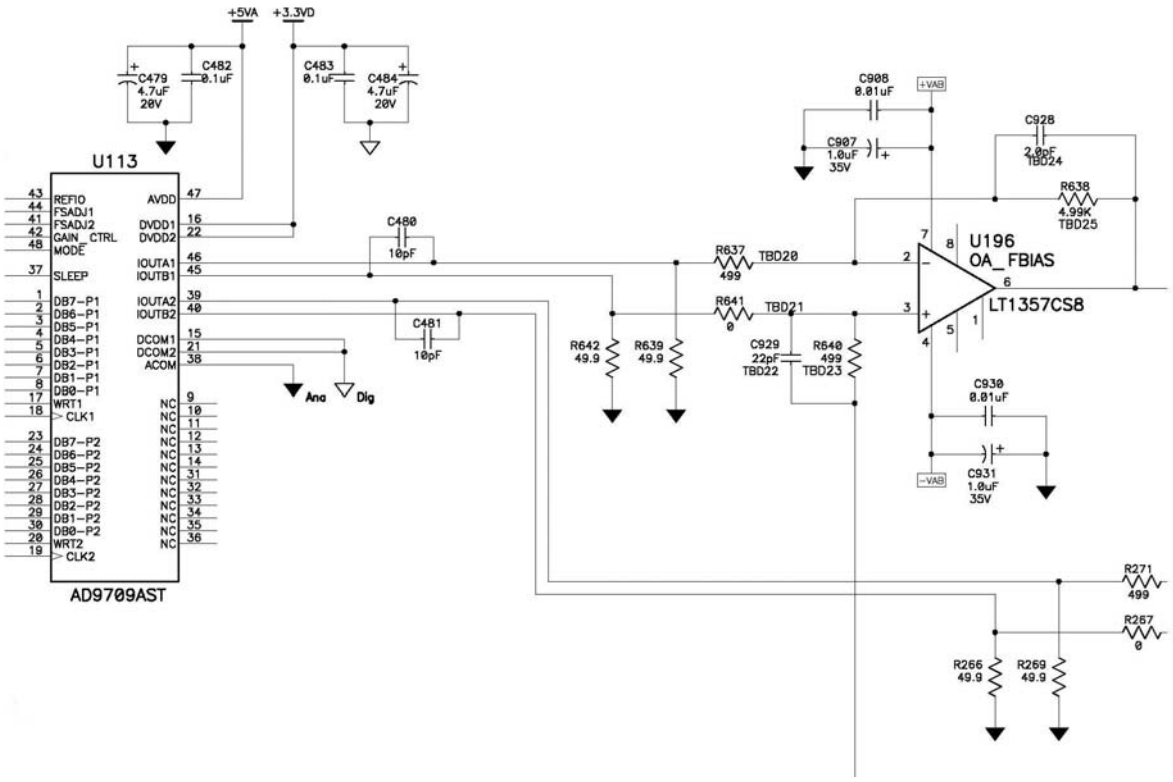
Each bias signal is provided with two monitor points to provide telemetry data for the voltage and the current draw. These telemetry data are accessed through a write-to-read operation on the corresponding board register (**CLK_TELBIASVDATA** and **CLK_TELBIASIDATA**). The write operation to the address that specifies the register initiates an ADC conversion cycle on the addressed channel. After a 35 microsecond delay, the result of that conversion is available in the same register for analysis. The telemetry ADC devices are eight-channel multiplexed MAX 1270 devices.
Each bias channel has a low value series resistor in series with the signal (**TBD1**) and an instrumentation amplifier (Type INA118 device) that amplifies the voltage difference across the resistor. Normally, a resistor value of 10 Ohms is installed and the gain of the amplifier set to 50 via a 1.02K Ohms resistor (**TBD2**). This provides for a sensitivity of 500mv per milliamp. This voltage is directed to the telemetry ADC devices that accept voltage ranges of +5, or +10v depending on the mode programmed by the MONSOON software (via the **CLK_TELBIASIMODE** register bank).
The voltage telemetry is derived by tapping the bias signal through a series resister. This resistor (**TBDRN2**) extends the nominal range of the ADC devices by using the internal voltage divider network of the MAX1270 device at the expense of producing an offset error in the conversion result. This offset error (which affects only bipolar measurements) is corrected in the MONSOON software. The mode of these telemetry channels is similarly controlled by MONSOON software by way of the **CLK_TELBIASVMODE** register bank.
Each group of bias signals can be isolated from the detector by an electronic switch controlled through MONSOON software. Two bias enable bits in the **CLK_GLOBAL_ENBL** register control this function.

2.2.9 Fast Bias Voltage Generators

There are eight high speed bias channels on the board. These signals are designed to provide multilevel clocks for detectors that would benefit from complex clocking. These bias channels can also be used to advantage in IR MUX applications where fast transitions of bias voltages are required. Each channel is controlled through an 8-bit value stored in the channel bank registers (**CLK_FBIAS_n**). The value is written directly to a DAC register on the four devices when the index register (**CLK_FBIAS0123** and **CLK_FBIAS4567**) is loaded with a pointer to the value. The DAC devices (U113, U117, U201, U202 and AD9709) each have two channels that operate in current mode. The internal reference of these DACs is normally used. The aforementioned external voltage reference for these DACs can be used with these devices by populating R297, R290, R666, and/or R679. Observe the maximum reference voltage rating on the DAC REFIO pin. The differential output current terms of the DAC are converted to a voltage by 50 Ohm resistors. The full scale output current of the AD9709 DAC is 20ma which corresponds to a voltage dynamic range of –1.0v to +1.0v. The voltage differential is amplified by a buffer amplifier (U93, U94, U102, U103, U193, U194, U196, and U198) with a gain of 10. This provides a dynamic range for the fast bias signals between –10v and +10v. If unipolar operation is required, resistor **TBD23** should be installed and resistor **TBD21** removed. This results in an inverse relationship of the fast bias DAC code to the output and, by suitable adjustment of the **FBIASVREF** value (**TBDFR2, TBDFR4**) an arbitrary output dynamic range can be created. Figure 16 shows a typical fast bias circuit topology.

The bandwidth of the fast bias signals is limited by the write cadence and the capacitor (TBD24) in the feed back network of the amplifiers.

The fast bias signal voltage telemetry functions in a similar fashion to the bias signal circuitry and in a like wise manner, the fast bias signals may be enabled / disabled through a bit in the **CLK_GLOBAL_ENBL** register.



Typical Fast Bias Circuit
Figure 16

2.2.10 Clock Generator Circuits

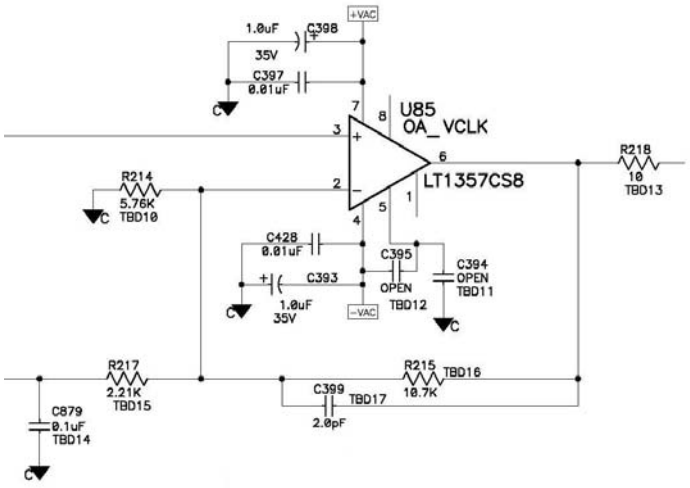
There are 32 clock channels available on the board. These are divided into two clock groups of twelve signals each and one clock group of eight clock signals (**CLK[0:11], CLK[12:23]** and **CLK[24:31]**). Each group can be adjusted independently for unipolar or bipolar operation.

This feature is controlled by the jumpers JP4, JP5, and JP6 in a similar fashion to the bias operating range adjustment. Boards are normally configured and delivered for bipolar operation with jumper pins 2 and 3 shorted.

Each clock has two DAC channels associated with it to establish the lower and upper clock voltages. These DACs are controlled in a similar manner to the bias DAC devices by way of arrays of registers (**CLK_LOWPORT** and **CLK_HIGHPORT**). The DAC reference voltage (**CLKDACREF**) is normally set to 3.04v by the resistors **TBDCR2** and **TBDCR4**.

The output voltage pair from the DAC is connected through low pass filters to an electronic switch. This switch acts as a multiplexer and selects either of the DAC voltage levels to the clock amplifier. The selection of the voltage from the multiplexer is controlled by a bit in the **CLK_CLKPORT** register that corresponds to the clock channel number. Turning a bit logically 'on' selects the voltage level from DAC controlled by the **CLK_HIGHPORT** register that corresponds to the channel number. Turning the **CLK_CLKPORT** register bit 'off' selects the voltage level from the DAC controlled by the **CLK_LOWPORT** register. Note that **CLK_LOWPORT** values do not have to be set to a lower voltage level than **CLK_HIGHPORT** values. This allows P channel CCD detectors and most IR arrays to be set up to use logical true clock signals.

The selected voltage level from the multiplexer is applied to the non-inverting node of the clock amplifier that has a nominal gain of 7.7. With the DAC reference set to 3.04v and a gain of 7.7, this allows a dynamic range of 23.4 volts. With bipolar operation selected (normal configuration), the offset reference voltage is applied to the inverting node of the clock output amplifier through resistor **TBD15**. This potential causes the amplifier output signal to be biased to –12v when the selected DAC voltage level is 0v (1.8v at inverting node x gain of -6.7). This offset allows the clock signals to swing between –12v and +11.4v. If unipolar operation of the clocks is required, the TBD16 resistors should be replaced by 4.93K Ohm 0.5% values and the associated offset jumper pins 1 and 2 shorted. This will reduce the clock amplifier gain to 4.1 and allow a clock swing between 0v and 12.4v.
The clock voltage values may be monitored through the corresponding telemetry channels (**CLK_TELCLOCKDATA**). This functionality is provided by U96, U97, U98, and U99. The method of access is as per the description in the power supply and bias supply sections. A typical clock driver circuit is shown in Figure 17.
The three groups of clock signals can be isolated from the detector by an electronic switch controlled via MONSOON software. One enable bit in the **CLK_GLOBAL_ENBL** register controls this function. An additional function is available for monitoring the clock waveforms. This is provided by the devices U42, U54, U65, U78, U90, and U189. These devices form a two x 32-channel multiplexer that allows the selection of any two clock signals to be output onto the P1 and P2 SMA connectors mounted at the front panel of the board. Selection of the two clock signals to be monitored is provided by decoding the value written to the **CLK_MUXSLCT** register.



Clock Driver Circuit
Figure 17

2.3 Jumper Descriptions

Table 15 - Configuration Jumper Descriptions

Jumper Number	Label Name	Default Condition	Default Function
JP1	BIASVREF1	2 ⇔ 3	Bipolar operation
JP2	FBIASVREF	1 ⇔ 2	Unipolar operation
JP3	BIASVREF0	2 ⇔ 3	Bipolar operation
JP4	CLKVREF2	2 ⇔ 3	Bipolar operation
JP5	CLKVREF0	2 ⇔ 3	Bipolar operation
JP6	CLKVREF1	2 ⇔ 3	Bipolar operation
JP7	AGNDPOINT0	SHORTED	GNDA Connected to DGND hard point
JP8	AGNDPOINT1	SHORTED	GNDC Connected to DGND hard point
JP9	3.3vSUPPLYSLCT	1 ⇔ 2	Select external 3.3v supply
JP10	LOC3.3vENABLE	OPEN	Disable local 3.3v regulator
JP11	LOCOSCENABLE	1 ⇔ +3.3v	Disable local oscillator (not used)

Table 16 - Test Point Functions

Test Point Number	Label Name
TP1	GNDA
TP2	GNDA
TP3	GNDA
TP4	GNDA
TP5	-5VA
TP6	+5VA
TP7	GNDC
TP8	RST 3.3V
TP9	+3.3VA
TP10	GNDC
TP11	+1.8V
TP12	~ADC_SHDN
TP13	~ADC_CS2
TP14	~ADC_CS5
TP15	~ADC_CS8
TP16	~ADC_CS11
TP17	~ADC_CS14
TP18	~ADC_CS0
TP19	~ADC_CS1
TP20	~ADC_CS4
TP21	~ADC_CS3
TP22	~ADC_CS7
TP23	~ADC_CS

Table 16 - Test Point Functions (Cont.)

Test Point Number	Label Name
TP24	~ADC_CS9
TP25	~ADC_CS10
TP26	~ADC_CS13
TP27	~ADC_CS12
TP28	~ADC_CS16
TP29	~ADC_CS15
TP30	SCLK
TP31	SDI
TP32	SDO
TP33	OB3.3RST
TP34	GND
TP35	FBIAS_WRT7
TP36	~DAC_SHDN
TP37	~DAC_CS1
TP38	~DAC_RST
TP39	~DAC_CS0
TP40	~TPS_RESET
TP41	FBIAS_WRT6
TP42	FBIAS_WRT5
TP43	FBIAS_WRT4
TP44	FBIAS_WRT3
TP45	FBIAS_WRT2
TP46	FBIAS_WRT0
TP47	FBIAS_WRT1
TP48	FBIAS_SLEEP
TP49	GND
TP50	GND
TP51	~DAC_CS8
TP52	~DAC_CS5
TP53	~DAC_CS7
TP54	~DAC_CS4
TP55	~DAC_CS6
TP56	~DAC_CS2
TP57	~DAC_CS3

3.0 Board Specifications

Table 17 – Specifications

Power Consumption	8 Watts
Clock signals	32 x Bi-level + 8 x 256 level clocks (Fast bias Dacs)
Clock signal voltage adjustment range	Jumper for –12.5v to 0v, 0v to +12.5v, and Bipolar –12v to +12.5v
Clock signal voltage setting resolution	50mv / 100mv – Voltage adjustment via software command
Clock signal current source/sink	30ma - Provision for detector protection schemes
Clock signal noise (BW < 20MHz)	< 2mv rms
Clock rise / fall time	Configurable, minimum 50ns
Bias signals	36
Bias signal voltage adjustment range	Jumper for –12.5v to 0v, 0v to +12.5v, and Bipolar –12v to +12.5v
Bias signal current source / sink	10 ma
Bias signal voltage setting resolution	50mv / 100mv – Voltage adjustment via software command
Bias Signal Noise (BW <20MHz)	< 250µv rms
Diagnostic Channels	Power + reference voltages + clocks voltages + biases voltages and currents + board temperature + serial number + firmware rev.
Auxiliary Functions	2 x channel front panel clock monitor ports
Physical Specifications	Bare board: Height - 233 mm (6U) Depth - 160 mm Thickness - 1.6 mm Fully populated: Height - 233 mm (6U) Depth - 208 mm Thickness - 20 mm
Mating Backplane	Per MNSN-AD-01-0006 (Linked Here)

4.0 Appendix I - Clock and Bias Board MONSOON to NEWFIRM

Each MONSOON system opreating an NOAO Extremely Wide Field Infrared Imager (NEWFIRM) instrument contains two Clock and Bias boards. These boards are unique to the NEWFIRM system and are identified with specific serial numbers. Please ensure that your Clock and Bias boards are specifically designed for the NEWFIRM system.

CAUTION: **Installing any Clock and Bias board other than one specifically designated for the NEWFIRM system can potentially damage the system or the board itself.**

Refer to NOAO Bill of Materials (BOM) MNSN-EL-04-4004-NFM for Clock and Bias board configurable components and their values that apply to the NEWFIRM system. Figure 18 is a sample of a BOM page.

This column indicates the designation for individual groups of components. For example, OA FBIAS tells you that the integrated circuits called out in the REFDES column are all associated with the Output Amplifier for the Fast Biases. TBD and a number indicate that the group of components in the REFDES column is associated with a value that will be determined by the user.

Configurable Items

Bill of Materials
Clock and Bias, NEWFIRM
SN003-SN005

Dwg#: MNSN-EL-04-4004-003
4/21/2005

ITEM	QTY	TBD des	REFDES	VALUE	P/N	MFR	P/N DIGIKEY	DESCRIPTION
1	8	OA_FBIAS	U93, U94, U102, U103, U193, U194, U196, U198		LT1357CS8	Linear Technology		IC, Op Amp 25MHz, 600V/us
2	32	OA_VCLK	U43, U44, U45, U46, U47, U48, U49, U50, U55, U56, U57, U58, U59, U60, U61, U62, U66, U67, U68, U69, U70, U71, U72, U73, U79, U80, U81, U82, U83, U84, U85, U86		LT1357CS8	Linear Technology		IC, Op Amp 25MHz, 600V/us
3	1	OPEN	R688		NOT INSTALLED	N/A	N/A	Resistor, 0805 OPEN
4	1	OPEN	R693		NOT INSTALLED	N/A	N/A	Resistor, 0805 OPEN
5	6	TBD1	R37, R44, R81, R316, R353, R396	10	ERJ-6ENF10R0V	Panasonic	P10.0CCT-ND	Resistor, 10 1% 1/10 Watt 0805
5A	6	TBD1-1	R36, R45, R88, R318, R346, R387	1	9C08052A1R00FGHFT	Yageo	311-1.00CCT-ND	Resistor, 1.0 ohm 1% 1/8W 0805
6	8	TBD1A	R10, R19, R52, R61, R94, R321, R322, R360	10	ERJ-6ENF10R0V	Panasonic	P10.0CCT-ND	Resistor, 10 1% 1/10 Watt 0805
6A	4	TBD1A-1	R53, R329, R330, R405	1	9C08052A1R00FGHFT	Yageo	311-1.00CCT-ND	Resistor, 1.0 ohm 1% 1/8W 0805
7	10	TBD1B	R28, R70, R71, R106, R337, R338, R368, R376, R413, R421	10	ERJ-6ENF10R0V	Panasonic	P10.0CCT-ND	Resistor, 10 1% 1/10 Watt 0805
7A	2	TBD1B-1	R62, R100	1	9C08052A1R00FGHFT	Yageo	311-1.00CCT-ND	Resistor, 1.0 ohm 1% 1/8W 0805
8	16	TBD10	R113, R118, R122, R127, R139, R145, R152, R158, R167, R174, R181, R188, R196, R202, R208, R214,	OPEN	NOT INSTALLED	N/A	N/A	Resistor, RC0603 OPEN
			R434, R440, R446, R452, R462, R468, R474,					

Sample Bill of Materials
Figure 18

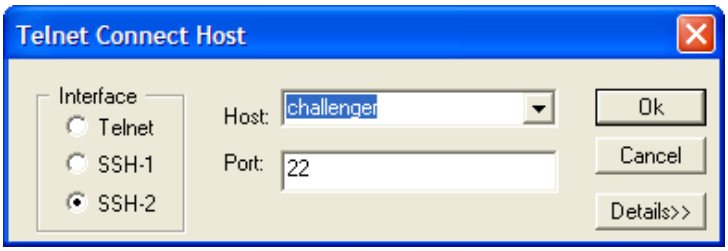
Appendix II - Front Panel Test Point Programming

Test Point Programming

The following instructions will allow programming of the test points as required by system configuration.

Starting WinaXe_Plus, PAN and MEC Software (Windows)

1. Click on **>START<** and **>ALL PROGRAMS<.** From the program list select XSession. The XSession icon will be displayed minimized on the task bar.
2. Right click on the XSession icon on the task bar and select Run and then Telnet on the displayed menus.
3. In the Telnet Connect Host window, enter host computer and port. Press **>OK<.** An Authentication window will be displayed. Enter the user name and passphrase. Press **>OK<** and an xterm window will open. See Figures 19 and 20.



Telnet Connect Host Window
Figure 19

Authentication Window
Figure 20

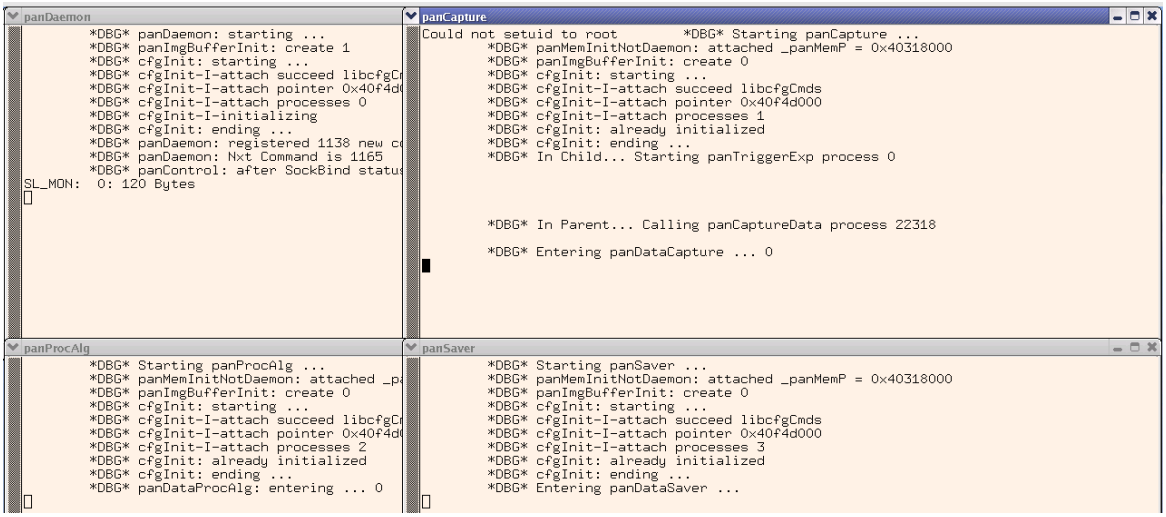
4. Open two xterm windows on the PAN. In the first xterm window, type **fs0** and look at the fiber link status. The status will probably show data in the receive FIFO buffer and should show the DHE to be in reset mode by having the *dir*(ection) bit true in the IO register (*i=01xx0*). The status command should return something similar to the following:

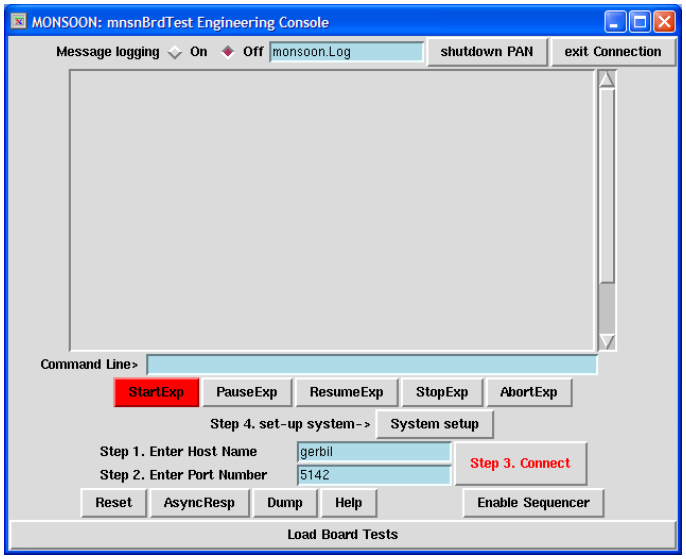
NOTE: Before proceeding with the next step, know what the PAN network name is and either create or identify an existing data directory in which to store the acquired data for test analysis. The PAN network name and the data directory name are then substituted in the command for the panMachineName and data variables.

5. In the xterm window, start the PAN software and MEC using the command:

mecStart ccdlab panMachineName localFITS 65

The four PAN process windows and the MEC window will be displayed as shown in Figure 21.

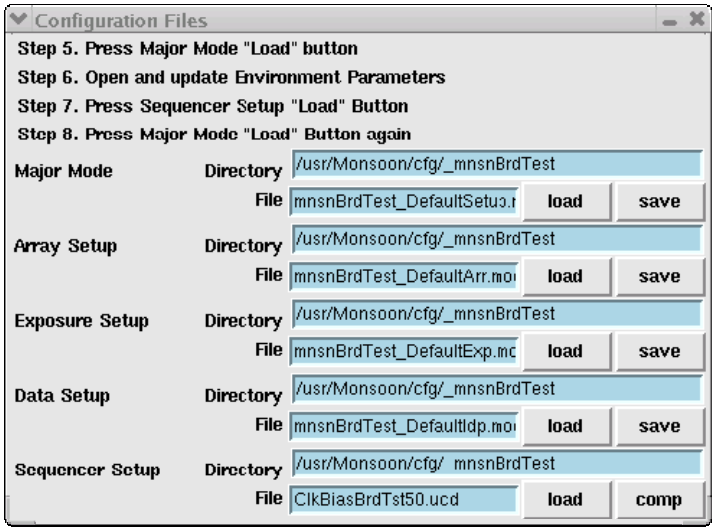




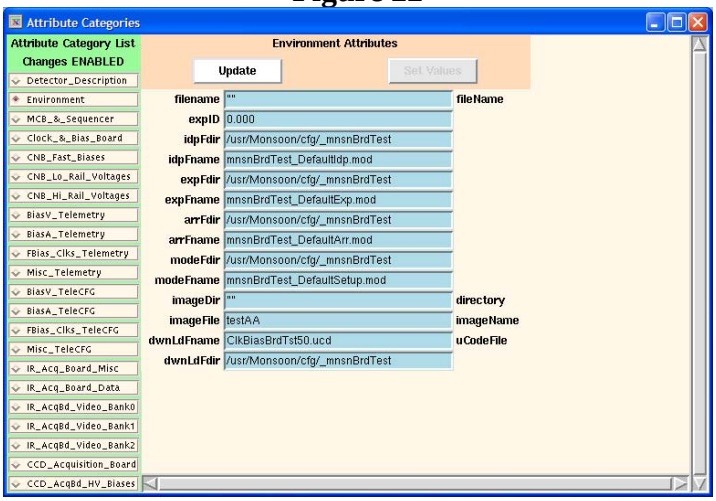
PAN and MEC Windows
Figure 21

6. Verify that the text fields "`Step 1. Enter Host Name`" and "`Step 2. Port Number`" contain the correct PAN machine name and port number (5142). If these items are not filled in, enter the correct information. Press the **>*STEP 3. CONNECT*<** button on the MEC. The ATTRIBUTE CATEGORIES page will appear. Next press the **>*RESET*<** then the **>*ASYNCRESP*<** buttons on the MEC. Synchronization of the communication link will occur and the "PIX" and "SEQ" LEDs on the MCB will turn off.

7. Press the **>*SYSTEM SETUP*<** button and execute "`step 5.`" In the Configuration Files window by pressing the **>*MAJOR MODE LOAD*<** button. This opens the ATTRIBUTE CATEGORIES screen. Press **>*ENVIRONMENT*<** and **>*UPDATE*<**. See Figures 22 and 23.



Configuration Files Window
Figure 22



Attribute Categories Window
Figure 23

8. In the Configuration Files window (Figure 21), press **>*SEQUNCER SETUP LOAD*<** and **>*MAJOR MODE LOAD*<** again.

9. In the Attribute Categories window select **>*CLOCKS*<**. In the right column of the list select **>*CLKP2MUXSLCT*<**. Enter appropriate information and press **>*UPDATE*<** button at the top of the columns. Repeat this procedure for **>*CLKP1MUXSLCT*<**.

NOTE: For complete Clock and Bias board testing procedures, see document MNSN-TS-01-0004. It can be found on the MONSOON website, http://www.noao.edu/ets/new_monsoon/index.htm