NATIONAL
OPTICAL
ASTRONOMY
OBSERVATORY

MAJOR INSTRUMENTATION GROUP
950 N. Cherry Ave.
P. O. Box 26732
Tucson, Arizona 85726-6732
(520) 318-8000 FAX: (520) 318-8303

MONSOON
Requirements for the Image Buffer Module

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Authored by:
Peter Moore
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Please send comments:
pmoore@noao.edu

Revision History

Version	Date Approved	Sections Affected	Remarks
1.0	2/12/2007	All	Original
2.0	2/10/2009	All	Reformatted to conform to current documentation standards.

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1.0 Introduction

This is a proposal for design and construction of an **Image Buffer Module** (**IBM**) for the MONSOON Image Acquisition System. The IBM is conceived as an add-on module to the existing MONSOON Master Control Board in the form of a plug in daughter board. The daughter board will be fitted to the existing CMC module mount point number one where the Systran SL100 fiber communication link now resides. The Systran link will be moved to the CMC module mount point number two.

1.1 Purpose

The purpose of this design is to implement a deep pixel data buffer to be fitted to the Master Control Board (MCB) of the NEWFIRM instrument Detector Head Electronics (DHE). This buffer shall remove the real time data acquisition constraint of the existing SL100 Systran data link and the Pixel Acquisition Node (PAN) computer. This work will correct the problem of Systran link data loss. We attribute the data loss to the inability of the Systran product to maintain an adequate data flow capability that is required by the data rate and data volume of the NEWFIRM instrument.

To provide a versatile hardware platform in the pixel data stream of MONSOON capable of being programmed in the future to provide limited pixel data processing capabilities.

2.0 Description

The MONSOON architecture describes two major physical sub-systems (Ref Figure I):

- The **Pixel Acquisition Node** (**PAN**) which is a normal computer running the MONSOON software on top of LINUX.
- The **Detector Head Electronics** (**DHE**) which is a chassis with a CPCI back plane that supports the major MONSOON functional cards.

Communication between these two sub-systems is implemented using a very simple bi-directional communications protocol between the PAN and the **Master Control Board** (**MCB**) that is physically plugged in to the DHE back plane in slot 1. The MCB controls the DHE back plane signaling via two separate busses, the sequencing of commands to other DHE circuit boards used in the acquisition of data, and the communication link to the PAN computer.

The protocol used to communicate to the PAN is physically implemented on a COTS fiber optic subsystem manufactured by Systran and designated SL100. The physical interface to the Systran subsystem is a PCI card at the PAN computer end and CMC IEEE P1386 card at the DHE end. The DHE electrical interface is ANSI/VITA 17-1998, more commonly described as an FPDP interface.

It is planned to insert the Image Buffer Module (IBM) into the communication stream at the point where the current Systran CMC card interfaces to the Master Control Board of the DHE via the FPDP interface at CMC mount point 1 (Ref Figure II).

This implies that the IBM will look like an MCB from the point of view of the PAN and look like a PAN from the point of view of the MCB.

The IBM will physically replace the current Systran SL100 CMC module mounted in CMC mount point 1 and connected to the MCB via connectors J3A, J4A, and J6A. The Systran shall be moved to the 2nd physical CMC mount point on the MCB. Connectivity between the IBM and the Systran is supplied via the connectors J7 and J8, and connectors J4B, J6B (Ref Figure II and III).

The location of the IBM allows the module to access all communication data passing between the PAN and DHE. These data are classified into the following classes.

PAN Commands – Sent from the PAN to command / control the behavior of the DHE. Command words can be echoed back to the PAN by the DHE as a response to ensure correct DHE reception.

Asynchronous Command – Sent from the PAN to synchronize communication between the PAN and the DHE.

DHE Command Response – Sent from the DHE to the PAN and can be either the echo of a Pan Command word, the result of a read command, or an Asynchronous Response.

Start Exposure Command – Sent by the PAN to initiate the acquisition of pixel data by the DHE. This command is never echoed back to the PAN.

Pixel Data – These data are the result of the acquisition of data by the DHE and need to be transmitted in a real time manner to the PAN.

2.1 The Primary Objective of the IBM Design

To accept all Pan Commands and Start Exposure Commands from the Systran FPDP interface at J7 and J8 and pass these to the MCB via the CMC mount point 1 FPDP interface at J4A and J6A and,

To accept all DHE Command Responses and Pixel Data from the MCB in a real time manner (i.e. as commanded by the MCB), buffer these data in local memory and then pass this data to the Systran FPDP interface *as allowed to* by the Systran ready and busy signals.

Thus the primary requirement of the IBM is to implement a deep FIFO element in the DHE to PAN data stream.

2.2 The Secondary Objective of the IBM Design

To allow block access to Pixel Data stored in the local memory by way of specific commands sent to the IBM from the PAN. These commands would allow specific Pixel Data to be sent to the PAN via the Systran FPDP interface. This allows for two additional modes of operation.

a). The PAN can request a resend of data that has been lost and / or can acquire Pixel Data as it requires it rather than having to accept data when the acquisition is taking place. This significantly changes the acquisition mode from a synchronous operation between the PAN and DHE to an asynchronous operation and, in addition,

b). Pixel Data can be readout in a sequence that is in image order rather than time order i.e. the Pixel Data can be de-scrambled as it is read from the DHE which relieves the computational load of the PAN.

This secondary objective implies a method in which the IBM can be configured with parameter lists that describe the required operation. This can be achieved in the same manner as the MONSOON DHE configuration is carried out i.e. by the use of internal registers in a control element coupled to the IBM local memory.

2.3 The Tertiary Objective of the IBM Design

To allow very fast computation of Pixel Data as to allow these data to be used in computing 2 dimensional centroid positions of objects within small sets of Pixel Data and to have sufficient computing power to use the results of these calculations to formulate commands to inject back to the MCB to control DHE acquisition process. Although this objective tends to infer the use of a programmable element such as a DSP device it is thought that such an asynchronous device would contribute an uncontrollable noise source to the sensitive video acquisition circuitry. Therefore, the preferred manner to implement this objective would be to allow sufficient capacity within an FPGA device to be able to program such functions in VHDL.

This tertiary objective is stated here only for the purpose of directing the architectural design process of the product. The exact definitions of the processing algorithms required by this objective have yet to be defined. This requirement only asks that consideration be taken during the design phase so that sufficient resources may be reserved to implement the 3rd objective in the future.

The IBM should look something like Figure IV.

3.0 Reference Documents

See the Related Materials information in Section 6 for a complete list of reference documents and other information.

3.1 Standard Terminology

To avoid confusion and to make very clear what the requirements for compliance are, many of the paragraphs in this standard are labelled with keywords that indicate the type of information they contain. The keywords are:

- RULE
- RECOMMENDATION
- SUGGESTION
- PERMISSION
- OBSERVATION

These keywords are used as follows:

RULE

<Paragraph Number> Subject Describing Text **RULE**

Rules form the basic framework of this draft standard. They are sometimes expressed in text form and sometimes in the form of figures, tables or drawings. All rules shall be followed to ensure compatibility between components. All rules use the “shall” or “shall not” words to emphasize the importance of the rule.

Example:

3.5 Status and Data Stream Interface **RULE**

RECOMMENDATION

<Paragraph Number> Subject Describing Text **RECOMMENDATION**

Wherever a recommendation appears, designers would be wise to take the advice given. Doing otherwise might result in some awkward problems or poor performance. It is possible to design a system that complies with all the rules but has poor performance. Recommendations found in this standard are based on this kind of experience and are provided to designers to speed their traversal of the learning curve. All recommendations use the "should" or "should not" words to emphasize the importance of the recommendation.

Example:

2.5.1 GPX Names **RECOMMENDATION**

SUGGESTION

<Paragraph Number> Subject Describing Text **SUGGESTION**

A suggestion contains advice that is helpful but not vital. The reader is encouraged to consider the advice before discarding it. Some design decisions that should be made are difficult until experience has been gained. Suggestions are included to help a designer who has not yet gained this experience.

Example:

2.5.2 Long Variables Names **SUGGESTION**

PERMISSION

<Paragraph Number> Subject Describing Text **PERMISSION**

In some cases, a rule does not specifically prohibit a certain design approach, but the reader might be left wondering whether that approach might violate the spirit of the rule or whether it might lead to some subtle problem. Permissions reassure the reader that a certain approach is acceptable and will cause no problems. All permissions use the "may" word to emphasize the importance of the permission.

Example:

2.6 Long Variables Names **PERMISSION**

OBSERVATION

<Paragraph Number>Subject Describing Text **OBSERVATION**

Observations do not offer any specific advice. They usually follow naturally from what has just been discussed. They spell out the implications of certain rules and bring attention to things that might otherwise be overlooked. They also give the rationale behind certain rules so that the reader understands why the rules shall be followed.

Example:

2.7 Long Variables Names **OBSERVATION**

In addition, within this document, two key words are used to define exact quantities with respect to requirements. These are:

- REQUIREMENT
- GOAL

REQUIREMENT

Requirements are expressed as a minimum acceptable value that will allow the performance characteristics of the system to be met. This term differs from the definition of a RULE in that a requirement specifies a 'quantity' that does not connect to anything (i.e. is not an interface) but rather provides a measure of the level of performance of a component of the interface.

GOAL

Goals are expressed as a desired improvement to a requirement that would enhance the system level performance in a significant way.

3.2 Glossary

The definitions of terminology are used in the following paragraphs are defined here:

/SIGNAL_NAME	Electrical signals that use negative logic are preceded by a '**/**' character.
COTS	Commercial Off The Shelf
Data Frame	The data that represents one complete read of the physical detectors attached to one DHE i.e. one read of all pixels in the focal plane segment attached to a DHE.
DHE	Detector Head Electronics
EM	Electro-Magnetic
EMI	Electro-Magnetic Interference
FPA	Focal Plane Assembly
Image Frame	The data that represents any number of Data Frames that are associated with the acquisition of one image by a DHE.
IR	Infrared
LAN	Local Area Network
ICD	Interface Control Document
N/A	Not Applicable
OTA	Orthogonal transfer array
PCB	Printed Circuit Board
PWM	Pulse Width Modulated
PAN	Pixel Acquisition Node
SCA	Sensor Chip Assembly
TBD	To Be Determined

4.0 Functional Requirements

Please refer to drawing MNSN-EL-04-2001R3 (see Section 6, Related Material) and Figure II and III.

4.1 Physical

4.1.1 RULE: Size of printed circuit board:

REQUIREMENT 2.91 inches x 5.87 inches conforming to CMC IEEE P1386 space envelope.

4.1.2 RULE: P6 Connector:

REQUIREMENT An additional connector called P6 shall be installed as to enable connectivity to the MCB. This connector shall be a MOLEX PART 71436-2864 or equivalent. The placement of this connector will be compatible with the footprint of J6A as defined in the MCB Assembly document MNSN-EL-04-0001_rA.

4.1.2 RULE: P7 and P8 Connector:

REQUIREMENT An additional two connectors called p7 and p8 shall be installed to enable connectivity to the Systran module. These connectors shall be MOLEX PART 71436-2864 or equivalent. The placement of this connector will be compatible with the footprint of J7 and J8 as defined in the MCB Assembly document MNSN-EL-04-0001_rA.

4.2 Power

4.2.1 RULE: Voltage of primary power source:

REQUIREMENT All circuitry shall be powered from a nominal 3.3Volt +/- 5% primary voltage source.

4.2.2 RULE: Primary power source access:

REQUIREMENT The primary power source shall be taken from connector J3 pins 9, 21, 39, and 57.

4.2.3 RULE: Power source peak current limit:

REQUIREMENT The maximum peak current to be drawn from the primary power source shall be three amps.

4.2.4 RECOMENDATION: Power source average current:

Concern should be taken as to the average current drawn from the primary power source. The DHE electronics chassis is usually mounted in close proximity to the telescope optical path and undue power dissipation will contribute to image quality degradation.

4.2.5 RECOMMENDATION: Power supply derivation:

Where power supplies other than 3.3Volts are required, designers should use linear regulators to provide them. The use of switch mode supply generation techniques will generally contribute to an increase of noise in the system.

4.2.6 PERMISSION: Alternate primary supply access:

The nominal pin outs for the connectors J4A, J6A, J7, and J8 specify the availability of a 5V +/-5% power source. These pins marked as +5VD may be strapped to the 3.3V supply rail on the MCB and used as additional primary power source access if required. There is no guarantee that these pins will provide a 5V supply in the future.

4.3 Electrical Interface

4.3.1 RULE: System clock access:

REQUIREMENT: The System Clock signal shall be taken from the provided PECL interface at the CONFIG port at connector J3A pins 29 (**PECL_IN**) and 31 (**/PECL_IN**).

4.3.2 RULE: System reset access:

REQUIREMENT: The System reset signal shall be taken from the provided LVTTL interface at FPTP_RMA port at connector J6A (**/RESET_IN**).

4.3.3 RULE: Data and control signal levels:

REQUIREMENT: All signals not otherwise specified will use LVTTL signaling levels compatible with 3.3V logic families.

4.4 FPDP Interface J4A, J6A

4.4.1 RULE: Interface protocol:

REQUIREMENT: This interface port shall conform to the Front Panel Data Port standard signaling protocol (ANSI/VITA 17-1998).

4.4.2 RULE: J4A interface mode:

REQUIREMENT: The design shall implement a 32 bit FPDP_TM interface on this connector. This port shall be called FPDP_TMA. The data flow on this connector is from the IBM to the MCB board. The physical pin out of this port shall conform to the definitions in Table 1.

4.4.3 RULE: J6A interface mode:

REQUIREMENT: The design shall implement a 32 bit FPDP_RM interface on this connector. This port shall be called FPDP_RMA. The data flow on this connector is from the MCB to the IBM board. The physical pin out of this port shall conform to the definitions in Table 2.

4.4.4 RULE: Use of the /RASUSPEND signal on J6A:

REQUIREMENT: Since the primary objective of this design is to provide a sufficiently deep FIFO buffer, this signal shall not be monitored by the MCB. This implies that when the communication link is "UP" (i.e. the Systran SL100 /RBNRDY signal on J7 is not true) the MCB may transmit data at anytime.

4.4.5 RULE: Use of the /RASYNC signal on J6A:

REQUIREMENT: This signal is used by the communication protocol of MONSOON to indicate to the PAN that the word previously sent on the interface is to be interpreted as a DHE Command Response. The DESIGN shall maintain the timing relationship between the data transferred to the IBM using the **/RASTROBE** signal and the **/RASYNC** signal when it is retransmitted to the Systran module via J7.

4.4.6 RULE: Interface data rate:

REQUIREMENT: The design shall be capable of receiving data from the J6A connector (FPDP_RM interface) at a synchronous rate of forty MWords per second for a maximum burst length of one GigaWord i.e. a twenty-seven second burst at forty Mwords/second. This requirement is based upon a buffer memory depth as specified in section 4.6.1.

4.4.7 RULE: Use of the /RESET_IN signal on J6A:

REQUIREMENT: The design shall be passing this signal through to the equivalent signal (**/RESET_OUT**) on the FPDP_TMB interface (via J8). This signal provides a simultaneous hardware reset to the IBM and to the Systran module.

4.4.8 RULE: Use of the RAPIO1_IN, RAPIO2_IN, and /RADIR signals J6A:

REQUIREMENT: The design shall pass these signals directly to the corresponding **PIO1_IOUT, PIO2_OUT,** and **/TBDIR** signals at connector J8. These signals are used to send asynchronous status signals from the MCB to the PAN. By routing these signals through the IBM design, this functionality shall be retained.

4.5 FPDP Interface J7, J8

4.5.1 RULE: Interface protocol:

REQUIREMENT: This interface port shall conform to the Front Panel Data Port standard signaling protocol (ANSI/VITA 17-1998).

4.5.2 RULE: J7 interface mode:

REQUIREMENT: The design shall implement a 32 bit FPDP_RM interface on this connector. This port shall be called FPDP_RMB. The data flow on this connector is from the Systran module to the IBM board. The physical pin out of this port shall conform to the definitions in Table 3.

4.5.3 RULE: J8 interface mode:

REQUIREMENT: The design shall implement a 32 bit FPDP_TM interface on this connector. This port shall be called FPDP_TMB. The data flow on this connector is from the IBM board to the Systran SL100 module. The physical pin out of this port shall conform to the definitions in Table 4.

4.5.4 RULE: Use of the Systran /RASUSPEND signal J8:

REQUIREMENT: The design shall respect the signaling on this signal so as to throttle the data transfer activity to the PAN computer via the Systran link module.

4.5.5 RULE: Use of the PIO1_IN, PIO2_IN, and /RBDIR signals on J7:

REQUIREMENT: The design shall pass these signals directly to the corresponding **PIO1_IOUT, PIO2_OUT,** and **/TADIR** signals at connector J4. These signals are used to decode a remote reset function from the PAN in the logic of the MCB. By routing these signals through the IBM design, this functionality shall be retained.

4.6 Logical Function

4.6.1 RULE: Depth of FIFO buffer:

The depth of the FIFO buffer implemented by the design shall be one Gigaword (32 bits / word) of data appearing on the J6A (FPDP_RM) interface. This is sufficient buffer memory to store one complete Image frame of NEWFIRM array data taken with sixty-two Fowler samples (i.e. reset -> 62 x Data Frame –> integrate –> 62 x Data Frame).

4.6.2 SUGGESTION: Depth of FIFO buffer:

The design could incorporate provision for a variable amount of FIFO memory by exploiting COTS plug in memory card options. This would allow the cost, and perhaps the power requirements of the module to be better tailored to future applications of the design.

4.6.3 RULE: Power up timing:

REQUIREMENT: The design shall power up and become operational within 100ms of the primary power source becoming stable.

4.6.4 RULE: Power up functionality:

REQUIREMENT: The design shall immediately enter a mode of operation that complies with the primary objective stated in section 2.1. In this mode, the IBM is essentially transparent to the PAN computer and to the MCB. This mode directly relieves the PAN computer and Systran interface of responding to the real time demands of the MCB. This mode shall persist until the design is powered down or the mode is changed by a configuration written by the PAN. This mode shall be called “basic mode”.

4.6.5 RULE: Reset functionality:

REQUIREMENT: The design shall retain all mode and configuration data previously established. The reset signal shall cause the FIFO buffer contents to be cleared and all state machines in the design to enter their respective idle states.

4.6.6 RULE: None blocking requirement:

REQUIREMENT: The design shall implement a non-blocking acquisition strategy. This requires that the design shall not inhibit the extraction of buffered data and the transmission of this data to the PAN computer (Via the interface at J8) while the acquisition of data is taking place on the interface at J6A). This rule applies to all modes of operation for the design. This rule infers that at the acquisition rate limit specified in section 4.4.6 the memory buffer appears to be a true two-port device allowing simultaneous writing and reading to the memory.

4.6.7 RULE: 2nd Objective implementation strategy:

REQUIREMENT: The design shall interpret PAN Commands written and addressed to the design by the PAN as per MONSOON Interface Control Document ICD 6.1 contained in document MNSN-AD-01-0005 section 5. Specifically the design shall be assigned a block of unique addresses from the available address space of the MCB. This implies that the design shall be selected when the least significant bit of the **BOARD SELECT BITS** is true (i.e. board one, the MCB, is selected) and the address contained in the **BOARD REGISTER ADDRESS** field lies between the values of 0x8000 and 0x8FFF.

4.6.8 RULE: 2nd Objective implementation strategy:

REQUIREMENT: The design shall respond to PAN Commands as described in sections 5.3 and 5.4 of the ICD 6.1 document.

4.6.9 RECOMENDATION: 2nd Objective implementation strategy:

The design should implement a 16 bit control register structures that can be written to and read from by the PAN as per 4.6.6. This register should be named the **CONTROL REGISTER**. The purpose of this register is to establish mode and operational control of the design by designating fields of bits appropriate to the purpose. The mode of operation designed to implement the 2nd objective should be called “Block Mode”.

4.6.10 RULE: 2nd Objective implementation strategy:

REQUIREMENT: When the design is configured to operate in block mode the design shall discriminate between DHE Command Response data and Pixel Data by the presence of the **/RASYNC** signal following a normal FPDP write operation on the interface at connector J6A. Data classified as DHE Command Response data shall be passed directly to the Systran FPDP interface without passing through the buffer. This allows normal communications to continue between the MCB and the PAN. Pixel Data (i.e. data received that is not followed by a **/RASYNC** signal) should be stored in the designs buffer memory.

4.6.11 RULE: 2nd Objective implementation strategy:

REQUIREMENT: When the design is configured to operate in block mode the design shall respond to PAN "Start Exposure" command as described in section 5.2.2 of the ICD 6.1 document. The design shall reset the mechanism used in the acquisition of Pixel Data so that the first Pixel Data word received by the design is placed at the buffer memory logical address 0x00000000. Each subsequent word of Pixel Data shall be stored in successive address locations. The latency between the time that the "Start Exposure" command is received and the design ready to acquire the first Pixel data word shall be less than one microsecond.

4.6.12 RULE: 2nd Objective implementation strategy:

REQUIREMENT: When the design is configured to operate in block mode and the amount of Pixel Data acquired exceeds the depth of the memory buffer, the design shall stop acquiring further data i.e. the design shall not wrap around.

4.6.13 RECOMENDATION: 2nd Objective implementation strategy:

The design should implement a set of 128 register structures. Each structure should contain one 16 bit register and two 32 bit registers with the following significance:

32 bits **BASE ADDRESS** of block read

32 bits **NUMBER OF WORDS** to read

16 bits **ADDRESS INCREMENT** value

An additional register should be established to act as a trigger to initiate a block read operation in the design. The **TRIGGER REGISTER** is written to by the PAN with the index (0:127) of the structure to initiate the block read. When this occurs, the design should clear a **LOOP COUNT** register value to zero and initiate a loop that reads a word from memory using the **BASE ADDRESS** + (**LOOP COUNT** * **ADDRESS INCREMENT**) as the logical address, write this word to the Systran FPDP interface, and increments the **LOOP COUNT**. This loop persists until the value of a **LOOP COUNT** reaches the value of the **NUMBER OF WORDS** in the structure pointed to by the **TRIGGER REGISTER**. When this occurs the **TRIGGER REGISTER** value is incremented and the loop restarted. This process should continue until the value of the **NUMBER OF WORDS** register in the structure pointed to by the **TRIGGER REGISTER** contains a value of zero.

4.6.14 RULE: 3rd Objective implementation strategy:

REQUIREMENT: Since the exact definition of the pre-processing algorithms required for the 3rd objective is not available at this time, the design shall consider the requirements of such an implementation by reserving sufficient resources for their future implementation. An indication of the application that these resources might be used for is shown in Figure V.

4.6.15 RECOMENDATION: 3rd Objective implementation strategy:

The design should implement set of firmware "hooks" to allow such future pre-processing code modules to interface to the memory data and to the acquisition process. At the minimum these hooks should consist of the following access points:

a) A 32 bit Pixel Data word acquisition counter that is reset-able by the internal logic after a pre-processing process has terminated. The output of this counter should be compared to a PAN write-able register called the **ACQUISITION COUNT** register. The output (result) of the comparison will be used to initiate pre-processing processes.

b) Read access to the buffer memory via the "Block read" logic outlined in section 4.6.13 to allow selection of Pixel Data to be made. No write access to the Block mode structures is required.

c) Write access to a block of the buffer memory using a PAN configurable register (**PROCESS BASE ADDRESS**) as an address pointer.

d) Access to the FPDP interface at connector J4A to allow feedback to be made to the MCB.

e) Access to the FPDP interface at connector J8 to allow coefficients and pre-processed data to be sent to the PAN computer.

f) Access to device internal block memory resources as shall be available.

4.6.16 RECOMENDATION: 3rd Objective implementation strategy:

The design should implement the pre-processing capability as a "black box" within the firmware that has access to the resources detailed in section 4.6.15.

4.7 Physical Implementation

4.7.1 RECOMMENDATION: Programmable logic devices:

Wherever possible, any programmable logic devices should be sourced from the Xilinx line of products.

4.7.2 RULE: Firmware design language constraint:

Firmware developed for the design shall be coded in VHDL and shall be sufficiently commented and annotated for future reference and maintenance.

4.7.3 RECOMMENDATION: Firmware design methodology:

If possible, firmware developed for the design should use a "Top Down" methodology to separate the overall functional design into connected functional modules. This should follow the MONSOON methodology of using a top level schematic design sheet to interconnect functional VHDL modules. An example of this methodology is given in the "Related Materials" section.

4.8 Auxiliary Requirements

4.8.1 RULE: Design ownership:

The IBM design, in its entirety, shall become the property of the National Optical Astronomy Observatory (NOAO). AURA-NOAO shall release the design under the open source license agreement as stated in the following link:
http://www.noao.edu/ets/new_monsoon/home/legal/MonsoonLicense.pdf

4.8.2 RULE: Encumberment of design:

Design tools and intellectual property used in the development of the design shall not encumber the design with any third party royalty agreements.

4.8.3 RULE: Deliverables of design:

The deliverable design shall include the following items.

a) A minimum of three fully functional IBM hardware modules.

b) Sufficient documentation to understand the use and configuration of options of the hardware modules.

c) Full schematic diagram as built.

d) PCB layout design as built.

e) Firmware source code as built.

f) Firmware loader files as built.

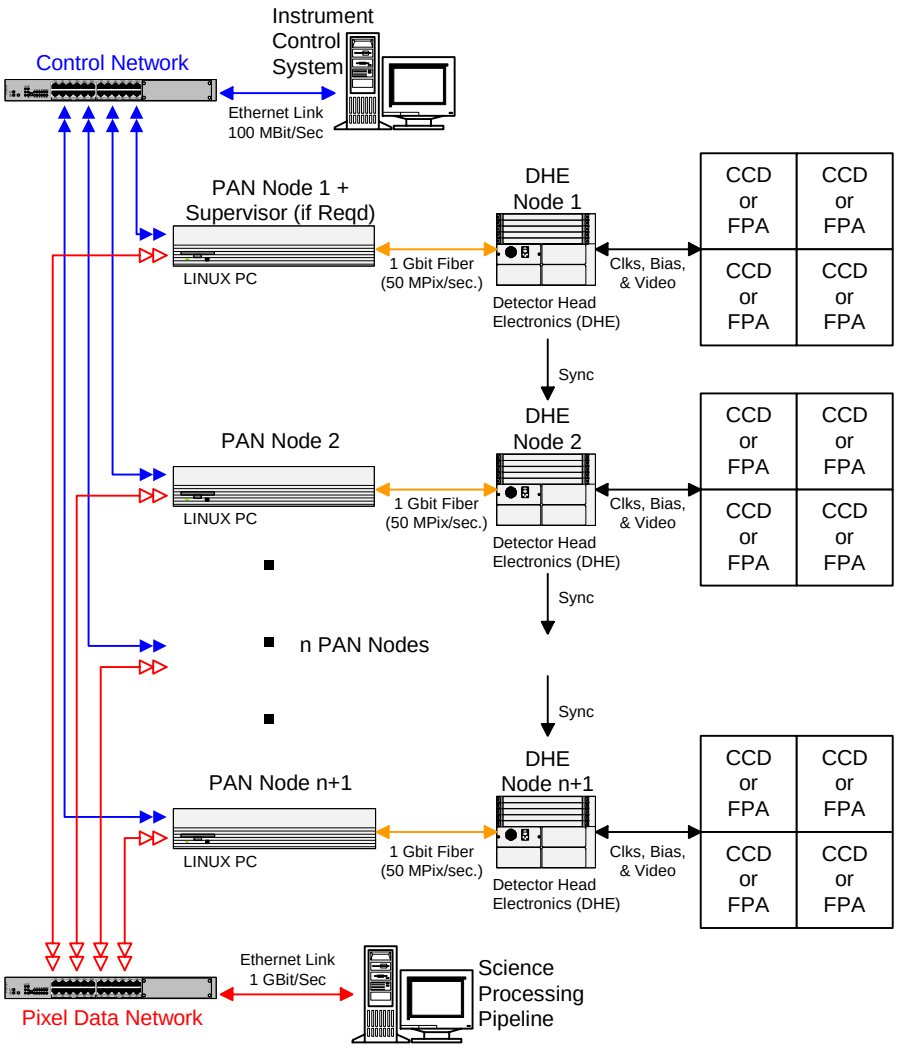
g) Firmware test bench source files as tested.

h) License of any Intellectual proprietary material used in the design.

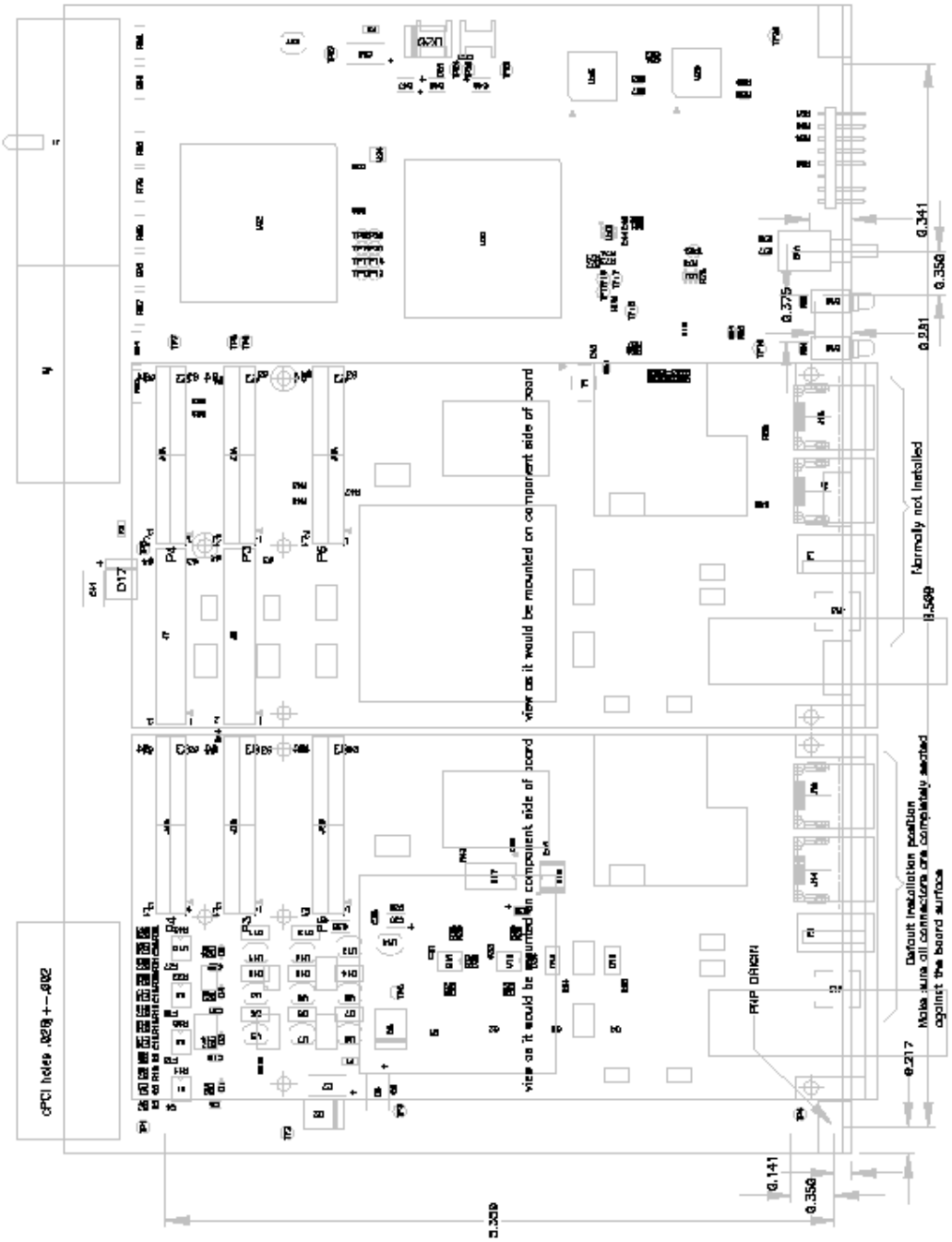
4.8.4 OBSERVATION: Deliverable hardware modules:

The immediate need is for two hardware modules to be installed, tested and operational on the NEWFIRM instrument by the 1st June 2007. When this has been accomplished, it is planned to purchase at least one module as a spare for NEWFIRM and additionally one or two modules to be used for the development of 3rd objective.

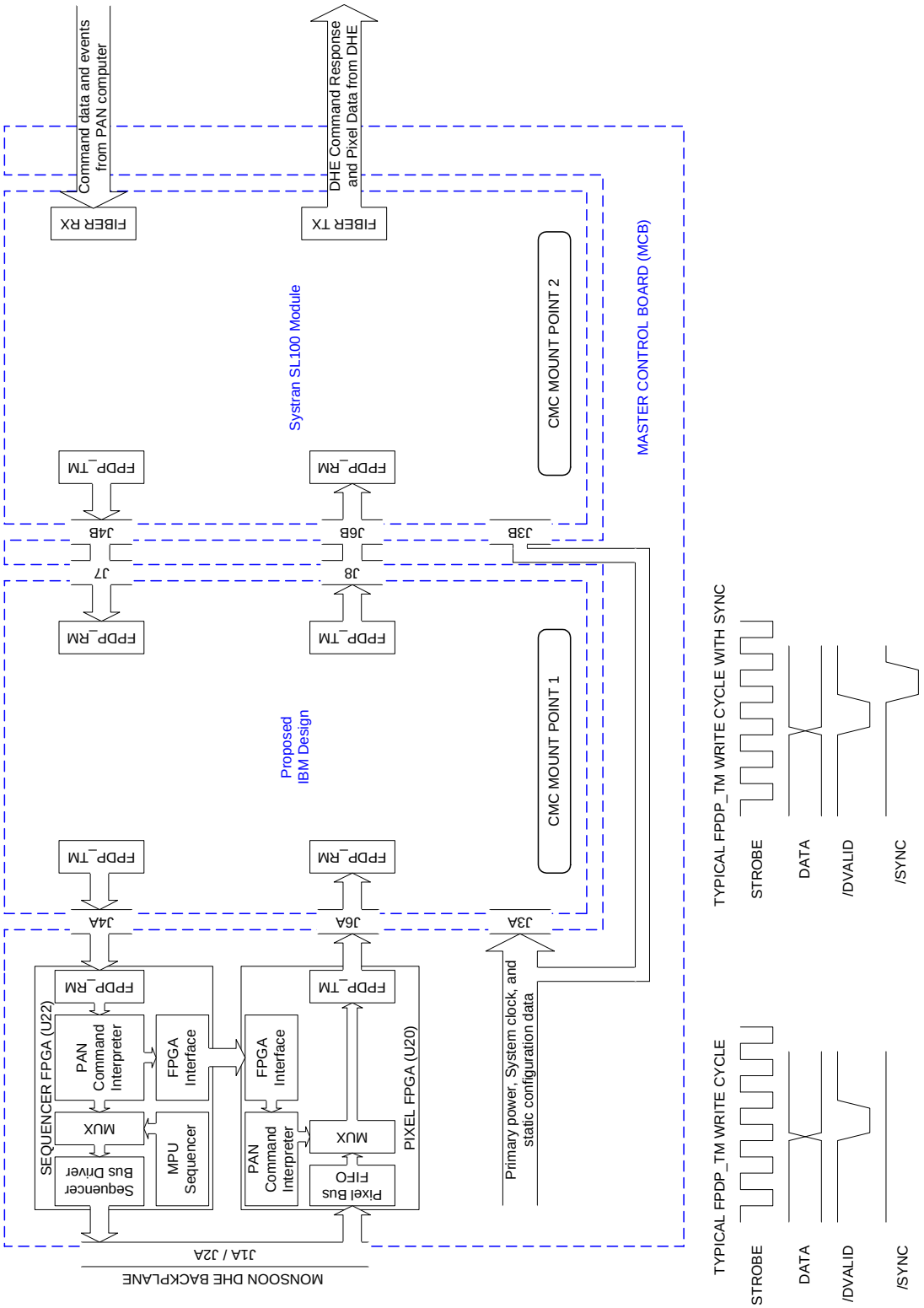
5. Figures



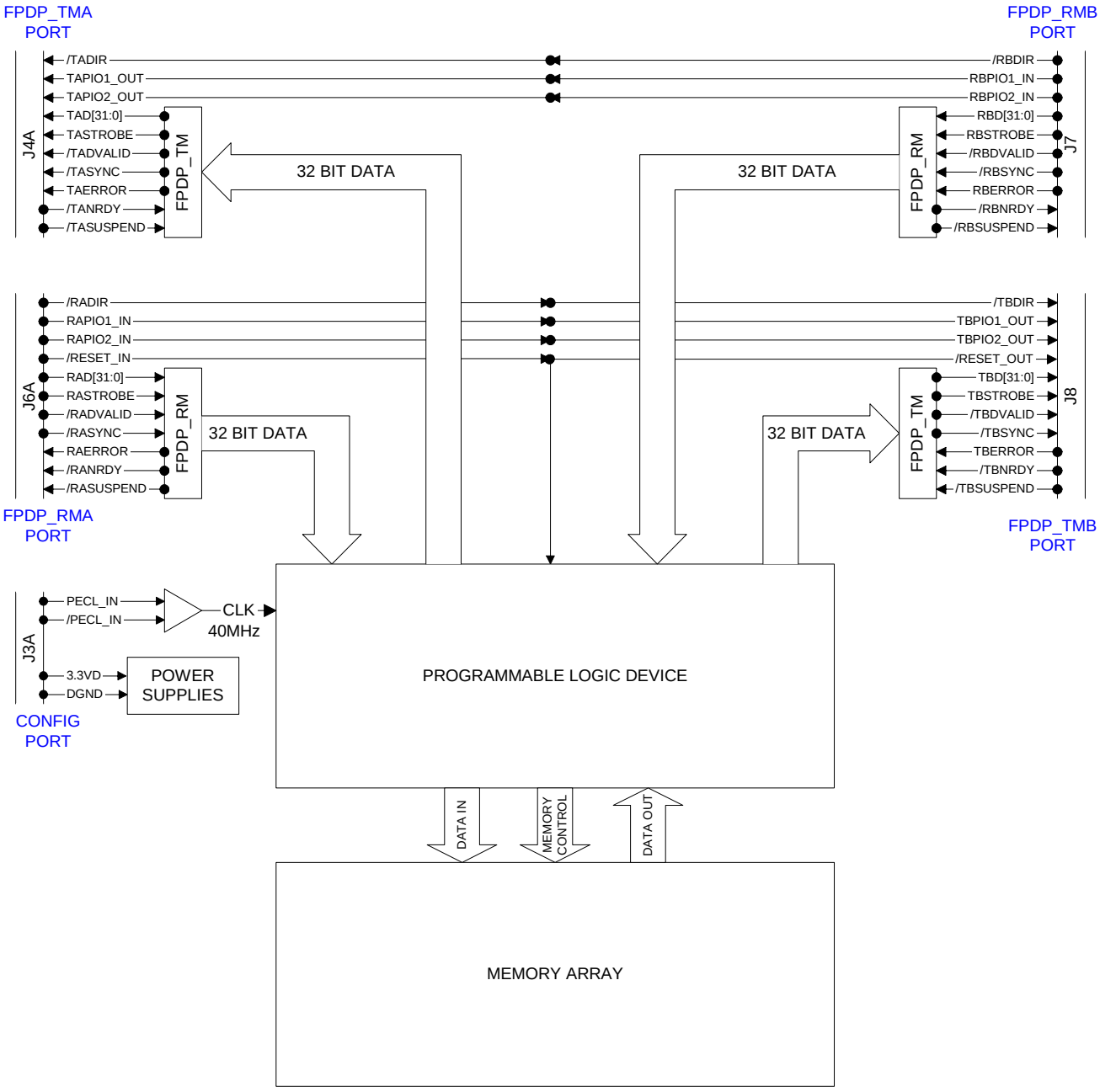
Nominal MONSOON System Architecture
Figure I



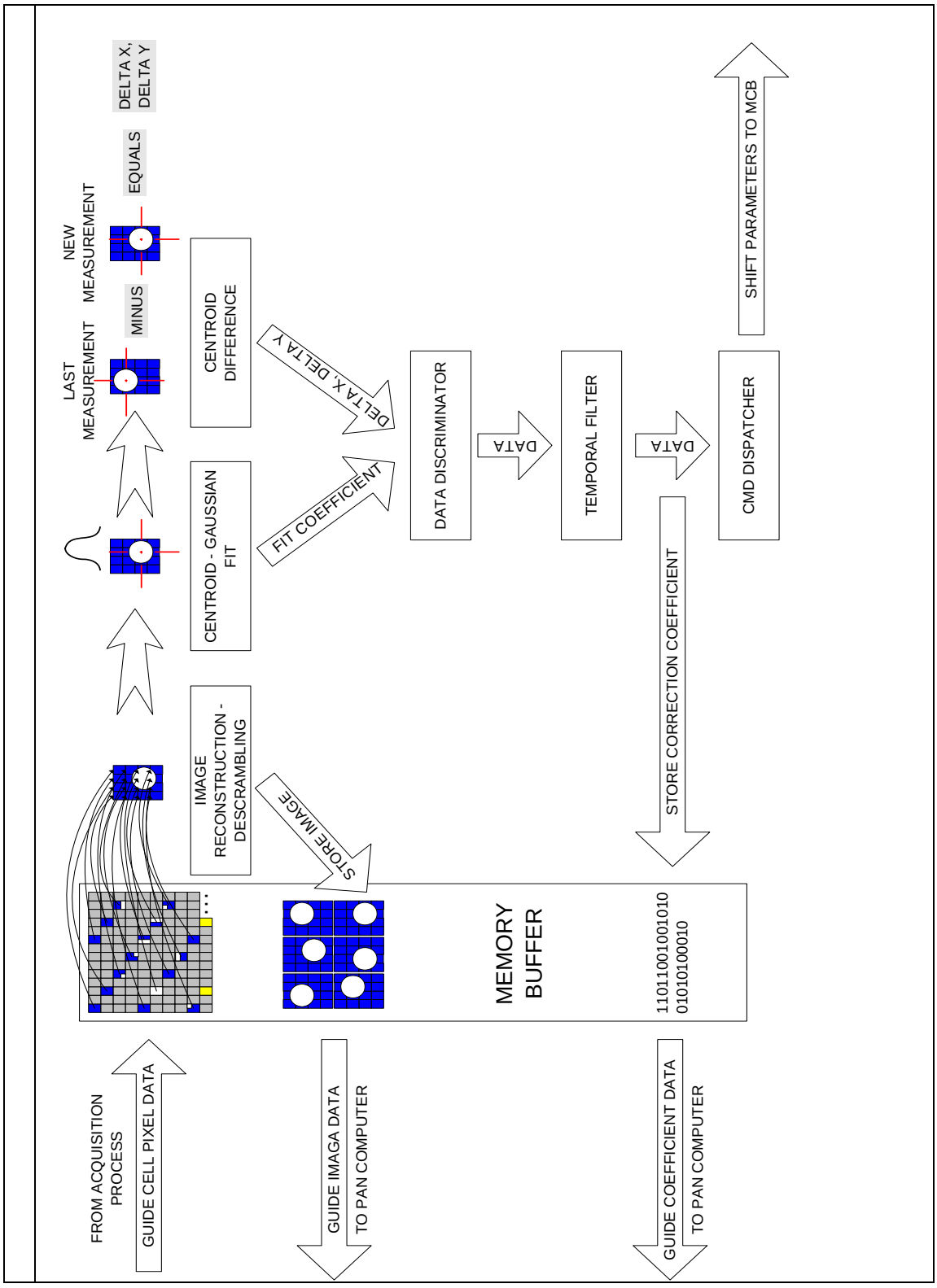
Master Control Board Physical Layout
Figure II



IBM Connectivity Diagram
Figure III



Generic Concept of IBM Design
Figure IV



Example of Proposed Future Processing Requirement
Figure V

6. Related Material

1. MONSOON Web Page:

   http://www.noao.edu/ets/new_monsoon

2. Systran Data Link Information:

   http://www.cwcembedded.com/products.php?mid=1&id=19

3. MONSOON Master Control Board (MCB) Schematic - MNSN-EL-04-2001R3

   http://www.noao.edu/ets/new_monsoon/technical/hardware/mcb/MNSN-E-04-2001_rA.pdf

4. MONSOON Master Control Board (MCB) Assembly Drawing – MNSN-EL-04-0001_rA.

   http://www.noao.edu/ets/new_monsoon/technical/hardware/mcb/MNSN-EL-04-0001_rA.pdf

5. Molex Connectors J3A, J4A, J6A, J7, J8 (MOLEX PART **71436-2864**)

   http://www.molex.com/cgi-bin/bv/molex/jsp/products/datasheet.jsp?ProductID=73278&BV_SessionID=@@@@@1332681989.1170699506@@@@@&BV_EngineID=ccceaddkdjfmmmicflgcehedffgdfmk.0&channel=Products&Lang=en-US

6. MONSOON Firmware style and methodology example. MCB Firmware suite.

   http://www.noao.edu/ets/new_monsoon/technical/firmware/mcb/0016/McbSeqFpgaV461.zip

   http://www.noao.edu/ets/new_monsoon/technical/firmware/mcb/0017/McbPixFpgaV461.zip

7. MONSOON ICD 6.1 document

   http://www.noao.edu/ets/new_monsoon/technical/architectural/MNSN-AD-01-0005_ICD_6.1_v1.0.pdf

7. I/O Port and Connector Pin Definitions

Table 1 – FPDP_TMA Port Connector J4A from Perspective of IBM Design

Pin	In / out	Signal		Pin	In / out	Signal
1	OUTPUT	TAD0		2		N.C
3	OUTPUT	TAD1		4	POWER	DGND
5	POWER	+5VD		6	POWER	+5VD
7	OUTPUT	TAD2		8	OUTPUT	TAD3
9	OUTPUT	TAD4		10	OUTPUT	TAD5
11	OUTPUT	TAD6		12	OUTPUT	TAD7
13	OUTPUT	TAD8		14	OUTPUT	TAD9
15	POWER	DGND		16	OUTPUT	TAD10
17	POWER	DGND		18	POWER	DGND
19	OUTPUT	TAD11		20	OUTPUT	TAD12
21	OUTPUT	TAD13		22	OUTPUT	TAD14
23	OUTPUT	TAD15		24	OUTPUT	TAD16
25	OUTPUT	TAD17		26	OUTPUT	TAD18
27	OUTPUT	TAD19		28	POWER	DGND
29	POWER	+5VD		30	POWER	+5VD
31	OUTPUT	TAD20		32	OUTPUT	TAD21
33	OUTPUT	TAD22		34	OUTPUT	TAD23
35	POWER	DGND		36	OUTPUT	TAD24
37	POWER	DGND		38	OUTPUT	TAD25
39	OUTPUT	TAD26		40	OUTPUT	TAD27
41	OUTPUT	TAD28		42	POWER	DGND
43	POWER	DGND		44	OUTPUT	TAD29
45	OUTPUT	TAERROR		46	OUTPUT	TAD30
47	INPUT	/RESET		48	OUTPUT	TAD31
49	POWER	+5VD		50	OUTPUT	TAPIO2_OUT
51	OUTPUT	/TASYNC		52	POWER	DGND
53	OUTPUT	/TADIR		54	POWER	+5VD
55	OUTPUT	/TADVALID		56		N.C
57	INPUT	/TASUSPEND		58	OUTPUT	TAPIO1_OUT
59	POWER	DGND		60	POWER	DGND
61	INPUT	/TANRDY		62	POWER	DGND
63	OUTPUT	TASTROBE		64		N.C

Table 2 – FPDP_RMA Port Connector J6A from Perspective of IBM Design

Pin	In / out	Signal		Pin	In / out	Signal
1	INPUT	RAPIO2_IN		2		N.C
3	POWER	+5VD		4	INPUT	RAPIO1_IN
5	OUTPUT	RAERROR		6		N.C
7	OUTPUT	/RANRDY		8	POWER	DGND
9	POWER	DGND		10	OUTPUT	/RASUSPEND
11	INPUT	RASTROBE		12	POWER	DGND
13	POWER	DGND		14	INPUT	/RADVALID
15	INPUT	/RESET		16	POWER	DGND
17		N.C		18	INPUT	/RADIR
19	INPUT	/RASYNC		20		N.C
21	INPUT	RAD31		22	POWER	+5VD
23	POWER	DGND		24	INPUT	RAD30
25	INPUT	RAD29		26	INPUT	RAD28
27	INPUT	RAD27		28	POWER	DGND
29	INPUT	RAD26		30	INPUT	RAD25
31	POWER	DGND		32	INPUT	RAD24
33	INPUT	RAD23		34	INPUT	RAD22
35	INPUT	RAD21		36	POWER	DGND
37	INPUT	RAD20		38	INPUT	RAD19
39	POWER	+5VD		40	INPUT	RAD18
41	INPUT	RAD17		42	INPUT	RAD16
43	INPUT	RAD15		44	POWER	DGND
45	INPUT	RAD14		46	INPUT	RAD13
47	POWER	DGND		48	INPUT	RAD12
49	INPUT	RAD11		50	INPUT	RAD10
51	INPUT	RAD9		52	POWER	+5VD
53	INPUT	RAD8		54	INPUT	RAD7
55	POWER	DGND		56	INPUT	RAD6
57	INPUT	RAD5		58	INPUT	RAD4
59	INPUT	RAD3		60	POWER	DGND
61	INPUT	RAD2		62	INPUT	RAD1
63	POWER	+5VD		64	INPUT	RAD0

Table 3 – FPDP_RMB Port Connector J7 from Perspective of IBM Design

Pin	In / out	Signal		Pin	In / out	Signal
1	INPUT	RBD0		2		N.C
3	INPUT	RBD1		4	POWER	DGND
5	POWER	+5VD		6	POWER	+5VD
7	INPUT	RBD2		8	INPUT	RBD3
9	INPUT	RBD4		10	INPUT	RBD5
11	INPUT	RBD6		12	INPUT	RBD7
13	INPUT	RBD8		14	INPUT	RBD9
15	POWER	DGND		16	INPUT	RBD10
17	POWER	DGND		18	POWER	DGND
19	INPUT	RBD11		20	INPUT	RBD12
21	INPUT	RBD13		22	INPUT	RBD14
23	INPUT	RBD15		24	INPUT	RBD16
25	INPUT	RBD17		26	INPUT	RBD18
27	INPUT	RBD19		28	POWER	DGND
29	POWER	+5VD		30	POWER	+5VD
31	INPUT	RBD20		32	INPUT	RBD21
33	INPUT	RBD22		34	INPUT	RBD23
35	POWER	DGND		36	INPUT	RBD24
37	POWER	DGND		38	INPUT	RBD25
39	INPUT	RBD26		40	INPUT	RBD27
41	INPUT	RBD28		42	POWER	DGND
43	POWER	DGND		44	INPUT	RBD29
45	INPUT	RBERROR		46	INPUT	RBD30
47	OUTPUT	/RESET		48	INPUT	RBD31
49	POWER	+5VD		50	INPUT	RBPIO2_IN
51	INPUT	/RBSYNC		52	POWER	DGND
53	INPUT	/RBDIR		54	POWER	+5VD
55	INPUT	/RBDVALID		56		N.C
57	OUTPUT	/RBSUSPEND		58	INPUT	RBPIO1_IN
59	POWER	DGND		60	POWER	DGND
61	OUTPUT	/RBNRDY		62	POWER	DGND
63	INPUT	RBSTROBE		64		N.C

Table 4 – FPDP_TMB Port Connector J8 from Perspective of IBM Design

Pin	In / out	Signal		Pin	In / out	Signal
1	OUTPUT	TBPIO2_OUT		2		N.C
3	POWER	+5VD		4	OUTPUT	TBPIO1_OUT
5	INPUT	TBERROR		6		N.C
7	INPUT	/TBNRDY		8	POWER	DGND
9	POWER	DGND		10	INPUT	/TBSUSPEND
11	OUTPUT	TBSTROBE		12	POWER	DGND
13	POWER	DGND		14	OUTPUT	/TBDVALID
15	OUTPUT	/RESET_OUT		16	POWER	DGND
17		N.C		18	OUTPUT	/TBDIR
19	OUTPUT	/TBSYNC		20		N.C
21	OUTPUT	TBD31		22	POWER	+5VD
23	POWER	DGND		24	OUTPUT	TBD30
25	OUTPUT	TBD29		26	OUTPUT	TBD28
27	OUTPUT	TBD27		28	POWER	DGND
29	OUTPUT	TBD26		30	OUTPUT	TBD25
31	POWER	DGND		32	OUTPUT	TBD24
33	OUTPUT	TBD23		34	OUTPUT	TBD22
35	OUTPUT	TBD21		36	POWER	DGND
37	OUTPUT	TBD20		38	OUTPUT	TBD19
39	POWER	+5VD		40	OUTPUT	TBD18
41	OUTPUT	TBD17		42	OUTPUT	TBD16
43	OUTPUT	TBD15		44	POWER	DGND
45	OUTPUT	TBD14		46	OUTPUT	TBD13
47	POWER	DGND		48	OUTPUT	TBD12
49	OUTPUT	TBD11		50	OUTPUT	TBD10
51	OUTPUT	TBD9		52	POWER	+5VD
53	OUTPUT	TBD8		54	OUTPUT	TBD7
55	POWER	DGND		56	OUTPUT	TBD6
57	OUTPUT	TBD5		58	OUTPUT	TBD4
59	OUTPUT	TBD3		60	POWER	DGND
61	OUTPUT	TBD2		62	OUTPUT	TBD1
63	POWER	+5VD		64	OUTPUT	TBD0

Table 5 – CONFIG Port Connector J3A from Perspective of IBM Design

Pin	In / out	Signal		Pin	In / out	Signal
1				2	POWER	DGND
3	POWER	DGND		4		
5				6		
7				8	POWER	DGND
9	POWER	+3.3VD		10		
11				12		
13				14	POWER	DGND
15	POWER	DGND		16		
17				18		
19				20	POWER	DGND
21	POWER	+3.3VD		22		
23				24		
25				26	POWER	DGND
27	POWER	DGND		28		
29	INPUT	PECL_IN		30		
31	INPUT	/PECL_IN		32	POWER	DGND
33	POWER	DGND		34		
35				36		
37				38	POWER	DGND
39	POWER	+3.3VD		40		
41				42		
43				44	POWER	DGND
45	POWER	DGND		46		
47				48		
49				50	POWER	DGND
51	POWER	DGND		52		
53				54		
55				56	POWER	DGND
57	POWER	+3.3VD		58		
59				60		
61				62	POWER	DGND
63	POWER	DGND		64		