Register Summary for the 12 Channel Board

CCD_CDSREG
0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Logical Channel Address Bits								EXT2	EXT1	RESET	DC REST	INT	NON INV	INV	CTC

RD/WR32 — direct access to CDS switches

CCD_DOPREG
0x0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

RD/WR32 — a 32 bit dummy register

CCD_BURST
0x0004

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

RD/WR32 — write anything here to trigger burst

CCD_SEQTRIG
0x0005

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
								Logical Channel Address Bits							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		Run Length of Sequence								Starting Address of Sequence					

RD/WR32 — write to trigger sequencer

CCD_ADCDATA
0x0100-0x010B

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
														D17	D16

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

R/O — Raw ADC data available after conversion

CCD_ADCCFG
0x0200-0x020B

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				TEST1	TEST0				CDS Logical Channel Address				CDS GAIN	WARP	PD

RD/W16 — ADC physical channel configuration

CCD_VOFFSETS
0x0210-0x021B

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

RD/W16 — Offset DACs

CCD_HVBIASES
0x0220-0x024F

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

RD/W16 — Bias DACs

CCD_TELMODE
0x0250-0x027F

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												RNG	BIP	PD1	PD0

RD/W16 — Telemetry configuration
note: set the RNG and BIP bits

CCD_AUXCFGREG
0x0280

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
													BIAS EN0	BIAS EN12	CDS ENABLE

RD/W16 — Misc configuration bits

CCD_REDIRECT
0x0300-0x0317

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												D3	D2	D1	D0

RD/W16 — Physical channel

CCD_XFERCOUNT
0x0340

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								D7	D6	D5	D4	D3	D2	D1	D0

RD/W16 — Specify the number of channels to transmit to the MCB

CCD_TELEMETRY
0x0440-0x046F

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

RD/W16 — write to trigger update

CCD_PATT_MEM
0x1000-0x103F

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Delay Value in units of 25ns								EXT2	EXT1	RESET	DC REST	INT	NON INV	INV	CTC

RD/W16 — Sequencer pattern memory

CCD_NVDAT
0x2000-0x20FF

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

RD/W16 — Non-Volatile RAM bufer

CCD_NVCTL
0x2100

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

W16 — Non-Volatile EEPROM control register

updated 3/9/2011

Jamieson Olsen

Register Summary for the 12 Channel Board

CCD_CAPCTRL
0x3000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR (WO)	W16 (RO)	W32 (RO)				PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0

RD/ W16 — Backplane Capture Control and Status register

CCD_CAPADDR
0x3001

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

R/O — Backplane Capture Address register

CCD_CAPDAT0
0x3002

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

R/O — Backplane Capture LOW data word

CCD_CAPDAT1
0x3003

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16

R/O — Backplane Capture HIGH data word

CCD_CTC_COUNT
0xC000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTC Count															

R/O — Audit Register (CCD_AUDIT_REG)

CCD_REQ_COUNT
0xC001

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Backplane Pipeline Request Count															

R/O — Audit Register (CCD_AUDIT_REG)

CCD_XFER_COUNT
0xC002

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Pixel Data Clock Cycle Count															

R/O — Audit Register (CCD_AUDIT_REG)

CCD_EVENT_REG
0xFFF0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START EXP															START FRAME

W16 — NOTE: this register is WRITE ONLY

CCD_VSUB
0xFFF8

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															ENABLE

RD/ W16 — Vbias enable. Ramp rate and upper limit are controlled by VBIAS channels 0 and 1.

CCD_LEDCTL
0xFFF9

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												FRONT PANEL	LED 2	LED 1	LED 0

RD/ W16 — used to blink the LEDs

CCD_SERNUM
0xFFFA

47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
SN47	SN46	SN45	SN44	SN43	SN42	SN41	SN40	SN39	SN38	SN37	SN36	SN35	SN34	SN33	SN32
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SN31	SN30	SN29	SN28	SN27	SN26	SN25	SN24	SN23	SN22	SN21	SN20	SN19	SN18	SN17	SN16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SN15	SN14	SN13	SN12	SN11	SN10	SN9	SN8	SN7	SN6	SN5	SN4	SN3	SN2	SN1	SN0

RD/ W16 — write to trigger update. the serial number is returned as a 48-bit value however only the lower 32-bits may be returned due to restrictions in the master control board, serial link, or Monsoon software.

CCD_TEMP
0xFFFB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

RD/ W16 — write to trigger update

CCD_CTLREG
0xFFFC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TESTPOINT CHANNEL SELECT					PRIORITY					DATA SELECT			BURST ENABLE	PIPE ENABLE	RESET DCM

RD/ W16 — Misc control bits

CCD_STATUSREG
0xFFFD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					SHUT DOWN	OWD ERR	SEQ BUSY	PIX BUSY	S/N CRC	OWD BUSY	TEMP BUSY	TEL BUSY	DAC BUSY	ADC BUSY	DCM LOCK

R/O — Misc board status bits

CCD_IDENTREG
0xFFFE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0

RD/ W16 — write to force a hard reset

CCD_FIRMVERS
0xFFFF

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

RD/ W16 — write to erase and reload the FPGA

updated 3/9/2011

Jamieson Olsen