

DesignStatus_01.txt

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Expedition PCB - Pinnacle - Version EXP2005.1_060615.00 2005.1
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Job Directory:

\\hep-ntserver\engines\DES\tcmoore\Technical_Documentation\DHE_Internal_Crate_C
ontrol_Ier\Vi cor_Fan_RPM_OK_PCB\Vi cor_Fan_RPM_OK\PCB\

Design Status Report:

\\hep-ntserver\engines\DES\tcmoore\Technical_Documentation\DHE_Internal_Crate_C
ontrol_Ier\Vi cor_Fan_RPM_OK_PCB\Vi cor_Fan_RPM_OK\PCB\LogFiles\DesignStatus_01.txt

Tue Sep 15 14:40:47 2009

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DESIGN STATUS
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Board Size Extents 1 X 0.65 (in)
Route Border Extents 0.4 X 0.6 (in)
Actual Board Area 0.65 (in)
Actual Route Area 0.24 (in)

Placement Areas: Name	Avai l ab l e	Requi red	
Requi red/Avai l ab l e			
Enti re Board	1.3 Sq. (in)	0.07 Sq. (in)	5.44 %

Pi ns 15
Pi ns per Route Area 62.5 Pi ns/Sq. (in)

Layers 4
Layer 1 is a signal layer
Trace Widths 10
Layer 2 is a signal layer
Trace Widths 10
Layer 3 is a signal layer
Trace Widths 10
Layer 4 is a Posi ti ve Plane Layer wi th nets
CATHODE
Trace Widths None.

Nets 6
Connecti ons 10
Open Connecti ons 0
Di fferenti al Pairs 0
Percent Routed 100.00 %

Netline Length 0 (in)
Netline Manhattan Length 0 (in)
Total Trace Length 2.02 (in)

Trace Widths Used (th) 10
Vi as 1
Vi a Span Name Quanti ty
1-4 026VIA 1

Teardrops..... 0
Breakouts..... 0

Vi rtual Pi ns..... 0
Gui de Pi ns 0

Parts Placed 5
Parts Mounted on Top 5

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DesignStatus_01.txt
SMD ..... 3
Through ..... 2
Test Points ..... 0
Mechanical ..... 0
Parts Mounted on Bottom ... 0
SMD ..... 0
Through ..... 0
Test Points ..... 0
Mechanical ..... 0
Embedded Components ..... 0
Capacitors ..... 0
Resistors ..... 0
Edge Connector Parts ..... 0

Parts not Placed ..... 0

Nested Cells ..... 0

Jumpers ..... 0

Through Holes ..... 9
Holes per Board Area ..... 13.85 Holes/Sq. (in)
Mounting Holes ..... 0

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