MONSOON
Clock Board

Clock Board Description
With Clock Board Transition Version 2.x

Firmware
With Version 4.x Firmware

Revision: 3

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Preface

This document has relevance to the hardware implementation of the DES MONSOON Clock Board that boots the FPGA firmware revision 3.x and later. Minor revisions and modifications to the capabilities and functionality of this board can be added as an appendix to this document. Major modifications to the functionality of the board that would require extensive modification to this document must originate a new and separate board description document.

Document Scope

This document provides an overall description, as well as detailed information on the architecture, configuration, testing and functionality of the DES MONSOON Clock Board. The intention is that this document be read by anyone who is considering, building, using or testing a DES MONSOON system that requires this hardware module.

Document Legend

Within this document, hardware signals are highlighted using an upper case bold black 12-point script typeface (e.g. **CLK_SIGNAL**). Hardware signals that are negative true are preceded by a slash character (e.g. **/SIGNAL**). Firmware control registers and internal device signals are highlighted using an upper case purple 12-point typeface (e.g. FIRMWARE_SIGNAL). Negative true firmware signals are denoted by a '_N' suffix (e.g. TRUE_N).

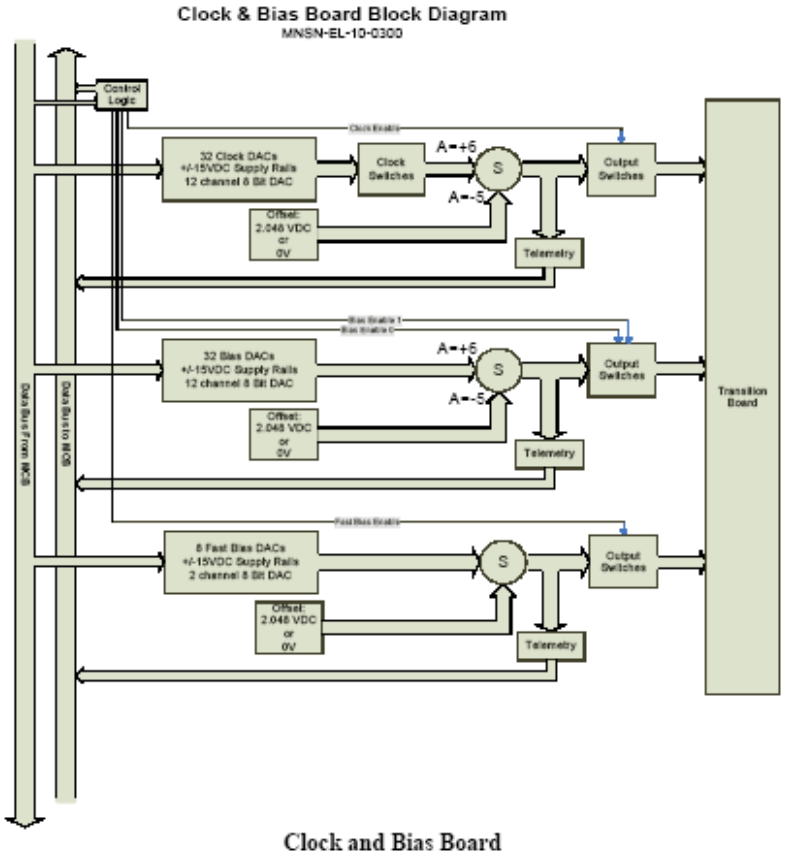
1.0 Board Functional Description

1.1 Purpose of Board

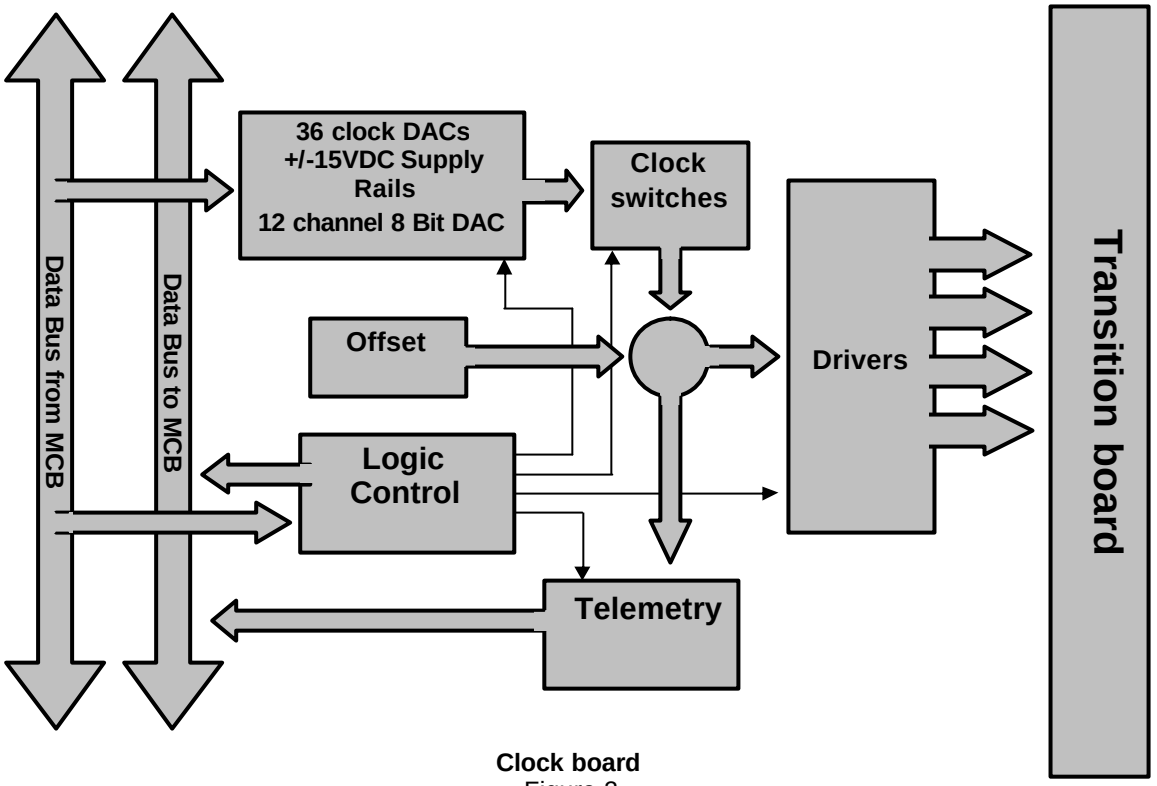
The Clock Board (CB) is designed to stimulate IR and CCD optical detectors. It provides the signals needed to clock data out of the CCD in readout cycle. The readout cycle consists of a transfer of the data from the image area to the frame-store area, followed by a readout and a digitization of the data in the framestore area.

The CB was designed at CIEMAT [1] and is compatible with the Monsoon [2] system developed at the National Optical Astronomy Observatory (NOAO) [3].

The CB is one of a series of peripheral boards using the MONSOON open source specification to allow medium and large arrays of detector elements to be controlled using a generic architecture. It is based in the Clock and Bias board (CBB) but it has been modified in order to use in the Dark Energy Survey experiment (DES)[4]. Both CBB and CB boards are 6U 160mm CompactPCI cards. In the Monsoon system a CompactPCI backplane is used however most of the pin functions have been reassigned. Both CBB (Figure 1) and CB (Figure 2) can be located into a standard MONSOON Detector Head Electronics (DHE) backplane. The Clock Transition Board (CTB) connects, across backplane, the CB and the CCDs.



Clock and Bias Board
Figure 1



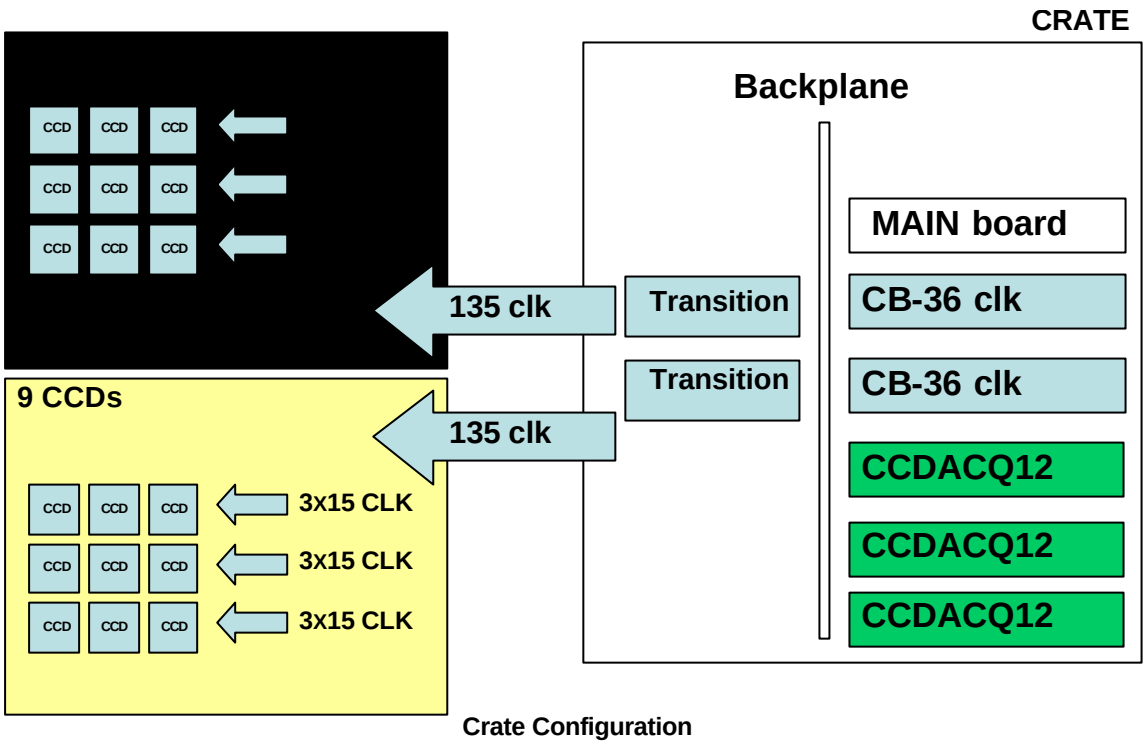
Clock board
Figure 2

The Clock Bias Board (CBB) provides 32 independent clocks, 32 Bias and 8 Fast Bias, while the Clock board (CB) provides 36 independent clocks which are replicated up to 135 clocks. Bias components have been removed from the CBB board and it has been replaced with new drivers in order to have enough clock lines for all the CCDs. The 12-channel CCD Acquisition board (CCDACQ12) designed at Fermilab[5] now controls Bias management.

As you can see in Figure 2, Bias and Fast Bias blocks are removed from the CBB scheme and the released space is occupied by the Drivers block in the CB. Three groups of 12 independent signals are replicated (x3 or x6) in the Drivers block for generating 3 groups of 45 signals summing up to 135 clock lines directed by exclusive channel drivers. Thus 9 CCD (15 clocks signals per CCD) can be readout by only one CB. Note that CCDs are grouped in 3 groups of 3CCDs.

In the CB clock generation stage, clock voltages are controlled by writing to DACs. There are 6 12-channels DACs. Each DAC is 12-bits so values from 0x000 to 0xFFF are allowed.

Figure 3 shows the 6-slot crate structure. The Crate is composed of several boards allocated in slots. The Master Control Board (MCB) always occupies the board select address one and occupies slot one of the backplane. Slot positions are numbered from the MCB position in linear fashion up to a maximum of 8. Three 12-channel CCD Acquisition (CCDACQ12) and two CBs disposed in a 6-slot crate provide the control of 18 CCDs.



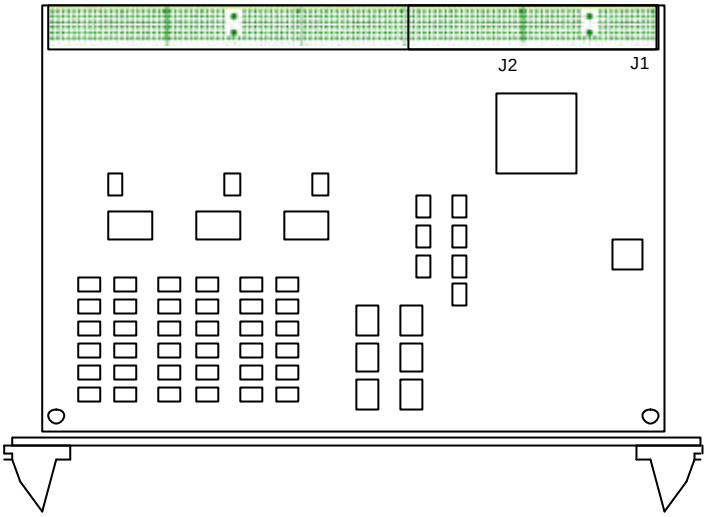
Crate Configuration
Figure 3

1.2 Interface Description

1.2.1 cPCI Connectors J1 and J2

J1 and J2 are two hard metric CB connectors interfacing with the MONSOON backplane. Digital lines (control lines, communication buses and digital supplies) come over these connectors. The Master Control board (MCB) sends instructions to all the boards of the crate through the backplane.

These connectors support the signal bus structures described in the sub paragraphs below. The complete physical description of these connectors is contained in the document ICD 7.0 DHE Backplane Definition (MNSN-AD-01-0006_V13).



Connectors J1 J2 situation

Figure 4

1.2.1.1 Board Clock and Board Select Signals

Each board fitted to the MONSOON backplane has a separate clock feed that is sourced from the MCB and received on connector J1 pin D6 (J1:D6). This clock is fed to the Clock Control FPGA U231. It provides for the synchronization of all bus transactions and clocks all internal functions of this board. The appropriate bit of the MCB clock control register (MCB_CLKENABLES) corresponding to the physical slot where the CB is located enable the clock. The nominal frequency of this system clock is 40.0 MHz and events are synchronized to the positive transition of the clock.

All bus transactions on the sequencer bus and destined for the Clock and Bias board are accompanied by the board **/SEL2** signal (J1:E5) going true for the duration of the transaction. There is a corresponding /ACK2 signal (J1:A6) that is currently not used.

1.2.1.2 Sequencer Bus Interface

All data and control transactions involving the CB are performed via the Sequencer Bus. There are four basic transaction types to control the board. They are described in more detail in document ICD 7.0 DHE Backplane Definition. The four transactions are reset, write 32-bit data, write 16-bit data, and read data (all reads are 32-bit). Bus activity is synchronous and timed to the rising edge of the board clock.

The Sequencer Bus is made up from four groups of signals: eight board select signals (**/SEL2 => /SEL8**), two bits of mode (**SEQ_MODE [1:0]**), six bits of device address (**DEV_ADDR [5:0]**), and thirty two bits of data (**SEQ_DATA [31:0]**).

The select board bits (**/SEL2 => /SEL8**) are used to activate a board for a bus transaction. Each slot of a CPCI backplane has a unique signal line that comes from the master slot. The actual signal that selects the board will depend on which backplane slot the board is

physically located in. It is legal for multiple board select lines to be active for either a reset or write transaction, however; only a single board select can be active for a read transaction.

The **SEQ_MODE [1:0]** signals define the four types of bus transactions and are detailed in Table 1.

Table 1 - Sequencer Bus Mode Bit Definitions

Mode	Transaction	Mode	Description
00	Reset	Hard or Soft	Reboot FPGA or soft reset the addressed board depending on SEQ_DEVADDR bits
01	Read	32 bits	Read a word from the addressed board
10	Write	16 bits	Write a 16-bits word to the addressed board
11	Write	32 bits	Write a 32-bits word to the addressed board

Note: A reset or write transaction takes one clock cycle to complete. A read transaction occupies three clock cycles.

Reset transactions: Reset mode timing is similar to a write transaction. If all bits of the **SEQ_DEVADDR [5:0]** signals are high, the board will reboot the firmware of FPGA and all configuration data is set to their default values. Approximately 30 milliseconds are required after a power cycle or reboot command before the board becomes functionally active. If all bits of the **SEQ_DEVADDR [5:0]** signals are low during a reset transaction, the board performs a 'soft reset' where only functionality is reset (i.e., state machines, etc.). Current configuration data is preserved. **Read transactions**: During a read transaction, the board interprets the required address from the least significant 16 bits of the sequencer bus signals (**SEQ_DATA [15:0]**) while the board select signal (**/SEL2**) is true. One bus clock cycle later, the data from the decoded address is placed on the pixel data bus. On the next bus clock cycle, the MCB latches this data and the board releases the pixel data bus. The board select signal remains true for the complete three clock cycle period. **Write transactions**: By specification, only the lowest sixty-four memory locations (0x0000 => 0x003F) of a peripheral board can be written using the 32-bit mode. In 32-bit write mode, the **SEQ_DEVADDR [5:0]** signals define the address information to the board. Data is defined on signals **SEQ_DATA [31:0]**. The data is written into the appropriate register of the board on the rising edge of the bus clock when the board select signal is true. When a 16-bit write transaction takes place, the address is defined by the most significant 16 bits of the sequencer data bus (**SEQ_DATA [31:16]**) signals and data is defined by the least significant sequencer data bus bits (**SEQ_DATA [15:0]**). The timing is equivalent to the 32-bit mode. An additional signal is defined in the sequencer bus interface specification called the Acknowledge Strobe (**/ACK2** => **/ACK8**). This signal is not used in this implementation.

1.2.1.3 Microsequencer Bus Interface

A new feature of CB is the implementation of a Microsequencer. The Microsequencer was designed in order to reduce substantially the data flow between all the boards in the backplane.

In the CBB board, the FPGA performs all instructions in real time. **CLK_CLKPORT** function orders the MCB to set the 32 clock signals levels in real time. The new CB FPGA can execute instructions in real time as the CBB or can also store a microinstruction list and execute it later when receiving the appropriated command. The microinstruction list also stores the period of time (D7-D0) each microinstruction should be applied. The CB uses 8 bits to encode the delay in 25 ns slot units (maximum 6400 ns). **CLKSEQ_PAT_MEM** function sends to the CB FPGA memory the microinstructions corresponding to high periodicity signals (H2, SW, RG, H3 and H1). When the Start Microsequencer function (**STARTMICRO**) is performed, the CB executes each microinstruction in the stored list according to the programmed timing.

1.2.1.4 Pixel Data Bus Interface

The Pixel Data Bus (**PIX_DATA [47:0]**) exists to transfer data from peripheral boards to the MCB and from there to the PAN via the optic link, Systran or S-link. It is a unidirectional 48-bit bus that connects to a 128-word FIFO (Pixel Bus FIFO) within the MCB pixel FPGA. The bus width allows three 16-bit, two 24-bit, or one 32-bit data value to be transferred to the MCB in one clock cycle. In 32-bit transfers, when responding to a read transaction, 32-bit data is latched into the MCB on the rising edge of the bus clock when commanded to do so by the MCB sequencer FPGA. This mode of operation (normal mode) is used exclusively to read individual addresses (registers) of the board under command of the PAN. All timing is controlled by the MCB firmware logic and results in three bus clock cycles being required for each 32-bit data value read.

1.2.2 JTAG Interface, Reset and Power on Boot

The CBB board had two CPLDs while in the CB those components were removed and their code was integrated in the device U231 (Xilinx Spartan II XC2s200 FPGA). The CB uses one FPGA to implement the logic functions. The FPGA has a 456 pin ball grid array (BGA) package. Using one large FPGA simplify many things at the firmware level since functional blocks are now inter-connected with parallel buses. The FPGA contains all essential timing and interface logic between the CB and backplane.

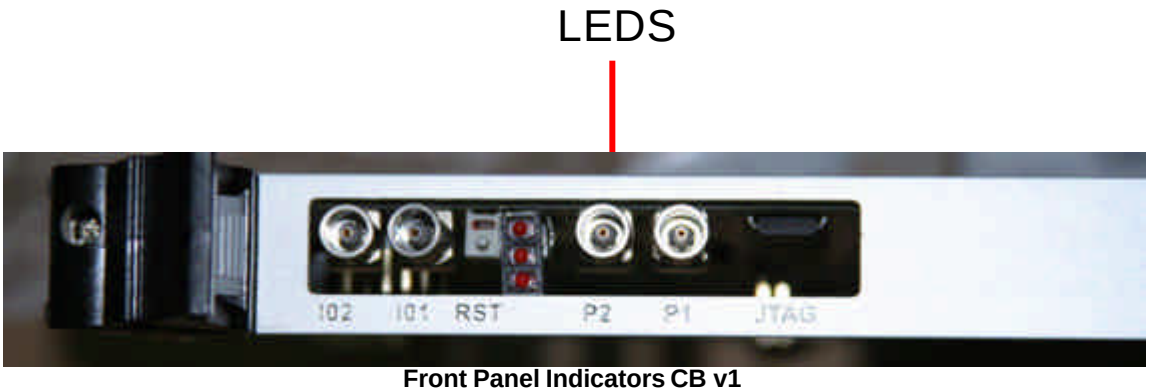
The boot EEPROM at U231 is programmed via the JTAG interface with the configuration data for the FPGA. This configuration data is automatically sent to the FPGA whenever a boot operation is performed. The interface can also be used to read the checksum of the EEPROM contents against a known value for each firmware version. Code stored in the EEPROM is loaded into the FPGA during power up, when the front panel reset switch is used (depends on firmware) or during a board reboot command from the PAN. The time to boot the code and perform power up initialization is approx. 30 milliseconds. It is normally not necessary to configure this device through the JTAG interface. The interface can however, be used to verify that the correct configuration is loaded to the FPGA during a boot. In addition, the JTAG interface can be used to read back the ‘User Code’ stored into the FPGA at boot time to verify the correct version and build date. The FPGA firmware configuration establishes the logic functionality of the entire CB and the interface to the MONSOON backplane.

The CB firmware is written completely in VHDL and functionally simulated using MODELSIM. Models of board components (ADCs, DACs, sensors, etc.) where created and connected to the FPGA in the VHDL testbench code. In the VHDL testbench the user applies stimulus to the Monsoon sequencer bus and can exercise all of the functionality of the board.

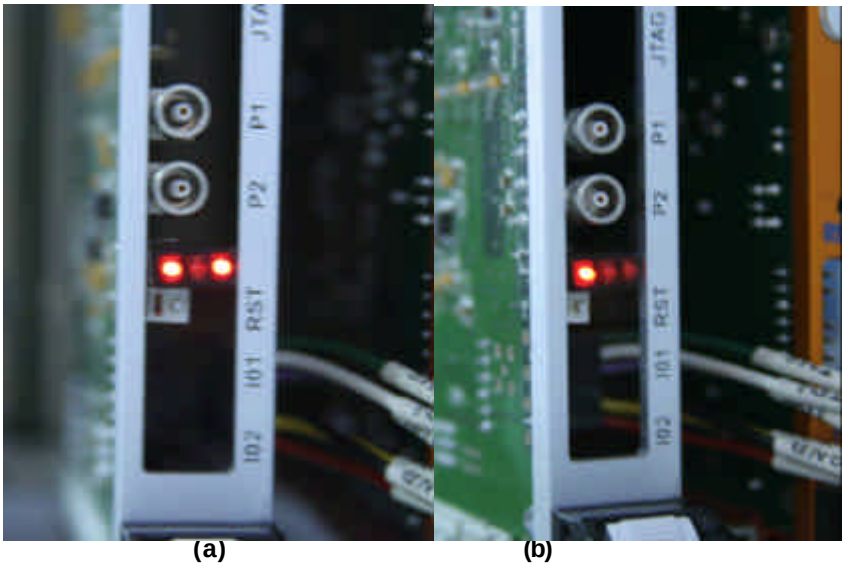
The JTAG chain is: J7:**TDI** => U232 FPGA boot EEPROM (type 18V02) => U119 Clock control FPGA (type Spartan II) => J7:**TDO**.
See Table 23.

1.2.3 Front Panel Indicators

There are three leds in CBv2.0 controlled by the FPGA firmware (Figure 6). During reset (push reset button) all indicators are off until the firmware has been booted. Left and right leds are switched on (Figure 7a) once firmware is initialized. The led on the left is controlled with bit 12 of mux register (**LED_MUX**). After booting right led is on. The indicator remains on until a first valid bus transaction is received from the MCB. Furthermore, this led is on while any valid bus transaction is received from the MCB. Central Led is on when reset command delivered by Monsoon. In addition all leds can be disabled with bit 13 of mux register.



Front Panel Indicators CB v1
Figure 6



(a) (b)

Front Panel LEDs in CB v2
Figure 7

1.2.4 Front Panel Test Points

P1 and P2 ports (Figure 8) provide access to any of the 36 clock signals by independent multiplexors (CLK_P1_SLCT, CLK_P2_SLCT). The function CLK_GLOBAL_ENBL works with switches before multiplexors. The clock signals are available in ports only when switches are closed.

Front Panel Test Points
Figure 8

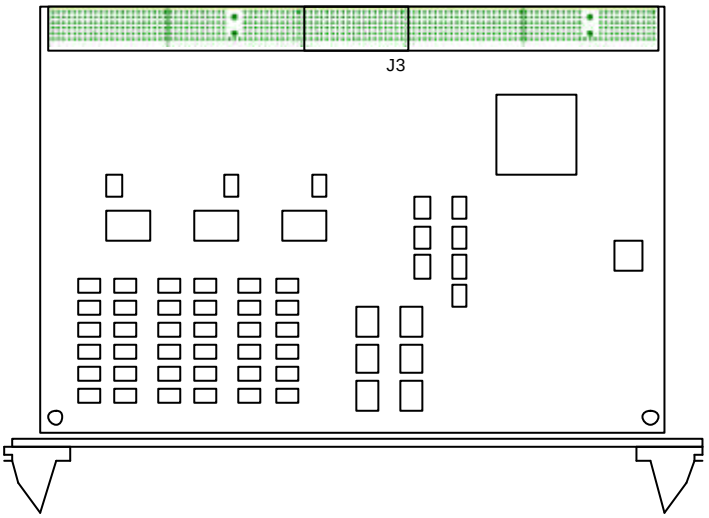
1.2.5 Front Auxiliary I/O Ports

IO1 and IO2 are programmable digital I/O ports (Figure 9). These lines are connected directly to the FPGA I/O ports in DESCBv1 while they are buffered in DESCBv2. These ports are configured as output by default and are connected to bits 14 and 15 of multiplexer register.

Front Auxiliary I/O Ports situation
Figure 9

1.2.6 cPCI Connectors J3, J4 and J5

These three hard metric connectors form the analog signal interface between the Clock and the Transition board. This board is allocated in the back side of the crate and connect directly to the directly detector(s) of an instrument.



Connector J3 situation
Figure 10

1.2.6.1 cPCI Connector J3

Connector J3 provides for clean analog power supplies and analog ground references to be connected. The specifications for J3 are contained in the document ICD 7.0 DHE Backplane Definition (MNSN-AD-01-0006_V13). These specifications are shown in Table 2 for convenience.

Table 2 - J3 Connector Pinout Description

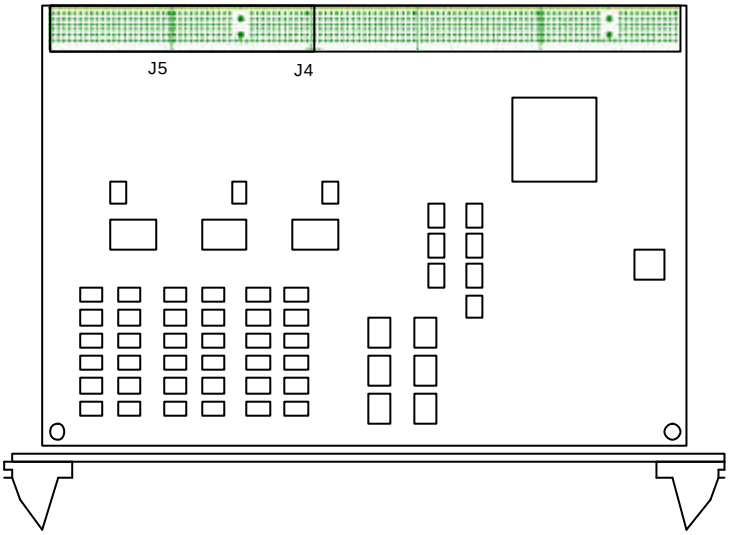
Pin	Z	A	B	C	D	E	F
19	AGND	+Vaux	+Vaux	+Vaux	+Vaux	+Vaux	AGND
18	AGND	-Vaux	-Vaux	-Vaux	-Vaux	-Vaux	AGND
17	AGND	+/-Vaux Return	+/-Vaux Return	+/-Vaux Return	+/-Vaux Return	+/-Vaux Return	AGND
16	AGND	+16.5VA	+16.5VA	+16.5VA	+16.5VA	+16.5VA	AGND
15	AGND	+/-16.5VA Return	+/-16.5VA Return	+/-16.5VA Return	+/-16.5VA Return	+/-16.5VA Return	AGND
14	AGND	-16.5VA	-16.5VA	-16.5VA	-16.5VA	-16.5VA	AGND
13	AGND	-6.5VA	-6.5VA	-6.5VA	-6.5VA	-6.5VA	AGND
12	AGND	+/-6.5VA Return	+/-6.5VA Return	+/-6.5VA Return	+/-6.5VA Return	+/-6.5VA Return	AGND
11	AGND	+6.5VA	+6.5VA	+6.5VA	+6.5VA	+6.5VA	AGND
10	AGND	Chassis GND	Chassis GND	Chassis GND	Chassis GND	Chassis GND	AGND
9	AGND	+5VA	+5VA	+5VA	+5VA	+5VA	AGND
8	AGND	+/-5VA Return	+/-5VA Return	+/-5VA Return	+/-5VA Return	+/-5VA Return	AGND
7	AGND	-5VA	-5VA	-5VA	-5VA	-5VA	AGND
6	AGND	-15VA	-15VA	-15VA	-15VA	-15VA	AGND
5	AGND	+/-15VA Return	+/-15VA Return	+/-15VA Return	+/-15VA Return	+/-15VA Return	AGND
4	AGND	+15VA	+15VA	+15VA	+15VA	+15VA	AGND
3	AGND	+/- HV Return	+/- HV Return	+/- HV Return	+/- HV Return	+/- HV Return	AGND
2	AGND	-HV	-HV	-HV	-HV	-HV	AGND
1	AGND	+HV	+HV	+HV	+HV	+HV	AGND

NOTE: +/-Vaux is reserved for auxiliary power.

NOTE: +/-HV is a user-defined high voltage power supply, nominally +/-30V.

1.2.6.2 cPCI Connectors J4 and J5

Connector J4 provides the interface to the 64 output clock channe ls. Clock voltages have an output range of ±10 Volts. These ranges are determined by digital to analogic converter (DAC). Clock voltages can be configured for either unipolar or bipolar in Clock and Bias board. These ranges are determined by hard configuring reference voltage jumpers. The clock board can not be configured, Clock board output ranges are bipolar but it is possible to change the reference voltage from 1.25 to 0 Volts by jumper.



Connectors J4 J5 situation
Figure 11

Connector J4 provides clock outputs and shutdown.

The **/SHUTDOWN** signal is provided as an input to the Clock board to allow supply and/or critical condition monitoring circuitry on a transition board to isolate the detector. Taking this signal true will open all the clock output enable switches from the Clock board and isolate the detector from these supplies.

The pinout of the J4 connector is provided in Table 3.

Table 3 - J4 Connector Pinout Description

Pin	Z	A	B	C	D	E	F
25	AGND	AGND	AGND	AGND	AGND	AGND	N/C
24	AGND	DCCD6_H3L	DCLKOUT25	DCLKOUT38	/SHTDWN	DCLKOUT63	N/C
23	AGND	DCCD6_V2	DCLKOUT24	DCLKOUT37	DCLKOUT50	DCLKOUT62	N/C
22	AGND	AGND	AGND	AGND	AGND	AGND	N/C
21	AGND	DCCD4_H3L	DCLKOUT23	DCLKOUT36	DCLKOUT49	DCLKOUT61	N/C
20	AGND	DCCD6_RGL	DCLKOUT22	DCLKOUT35	DCLKOUT48	DCLKOUT60	N/C
19	AGND	AGND	AGND	AGND	AGND	AGND	N/C
18	AGND	DCCD5_V1	DCLKOUT21	DCLKOUT34	DCLKOUT47	DCLKOUT59	N/C
17	AGND	DCCD4_V1	DCLKOUT20	DCLKOUT33	DCLKOUT46	DCLKOUT58	N/C
16	AGND	AGND	AGND	AGND	AGND	AGND	N/C
15	AGND	DCCD5_TG	DCLKOUT19	DCLKOUT32	DCLKOUT45	DCLKOUT57	N/C
14	AGND	Key	Key	Key	Key	Key	N/C
13	AGND	Key	Key	Key	Key	Key	N/C
12	AGND	Key	Key	Key	Key	Key	N/C
11	AGND	DCCD5_RGU	DCLKOUT18	DCLKOUT31	DCLKOUT44	DCLKOUT56	N/C
10	AGND	AGND	AGND	AGND	AGND	AGND	N/C
9	AGND	DCCD2_H3U	DCLKOUT17	DCLKOUT30	DCLKOUT43	DCLKOUT55	N/C
8	AGND	AGND	AGND	AGND	AGND	AGND	N/C
7	AGND	DCCD3_V2	DCLKOUT16	DCLKOUT29	DCLKOUT41	DCLKOUT54	N/C
6	AGND	AGND	AGND	AGND	AGND	AGND	N/C
5	AGND	DCCD1_H3U	DCLKOUT15	DCLKOUT28	DCLKOUT41	DCLKOUT53	N/C
4	AGND	AGND	AGND	AGND	AGND	AGND	N/C
3	AGND	DCCD1_H1U	DCLKOUT14	DCLKOUT27	DCLKOUT40	DCLKOUT52	N/C
2	AGND	AGND	AGND	AGND	AGND	AGND	N/C
1	AGND	DCCD1_H1L	DCLKOUT13	DCLKOUT26	DCLKOUT39	DCLKOUT51	N/C

Pin	Z	A	B	C	D	E	F
25	AGND	AGND	AGND	AGND	AGND	AGND	N/C
24	AGND	DCLKOUT12	DCLKOUT25	DCLKOUT38	/SHTDWN	DCLKOUT63	N/C
23	AGND	DCLKOUT11	DCLKOUT24	DCLKOUT37	DCLKOUT50	DCLKOUT62	N/C
22	AGND	AGND	AGND	AGND	AGND	AGND	N/C
21	AGND	DCLKOUT10	DCLKOUT23	DCLKOUT36	DCLKOUT49	DCLKOUT61	N/C
20	AGND	DCLKOUT9	DCLKOUT22	DCLKOUT35	DCLKOUT48	DCLKOUT60	N/C
19	AGND	AGND	AGND	AGND	AGND	AGND	N/C
18	AGND	DCLKOUT8	DCLKOUT21	DCLKOUT34	DCLKOUT47	DCLKOUT59	N/C
17	AGND	DCLKOUT7	DCLKOUT20	DCLKOUT33	DCLKOUT46	DCLKOUT58	N/C
16	AGND	AGND	AGND	AGND	AGND	AGND	N/C
15	AGND	DCLKOUT6	DCLKOUT19	DCLKOUT32	DCLKOUT45	DCLKOUT57	N/C
14	AGND	Key	Key	Key	Key	Key	N/C
13	AGND	Key	Key	Key	Key	Key	N/C
12	AGND	Key	Key	Key	Key	Key	N/C
11	AGND	DCLKOUT5	DCLKOUT18	DCLKOUT31	DCLKOUT44	DCLKOUT56	N/C
10	AGND	AGND	AGND	AGND	AGND	AGND	N/C
9	AGND	DCLKOUT4	DCLKOUT17	DCLKOUT30	DCLKOUT43	DCLKOUT55	N/C
8	AGND	AGND	AGND	AGND	AGND	AGND	N/C
7	AGND	DCLKOUT3	DCLKOUT16	DCLKOUT29	DCLKOUT41	DCLKOUT54	N/C
6	AGND	AGND	AGND	AGND	AGND	AGND	N/C
5	AGND	DCLKOUT2	DCLKOUT15	DCLKOUT28	DCLKOUT41	DCLKOUT53	N/C
4	AGND	AGND	AGND	AGND	AGND	AGND	N/C
3	AGND	DCLKOUT1	DCLKOUT14	DCLKOUT27	DCLKOUT40	DCLKOUT52	N/C
2	AGND	AGND	AGND	AGND	AGND	AGND	N/C
1	AGND	DCLKOUT0	DCLKOUT13	DCLKOUT26	DCLKOUT39	DCLKOUT51	N/C

Connector J5 provides the interface to the 75 output clock channels. Clock voltages have an output range of ±10 Volts. These ranges are determined by digital to analogic converter (DAC).

Table 4- J5 Connector Pinout Description

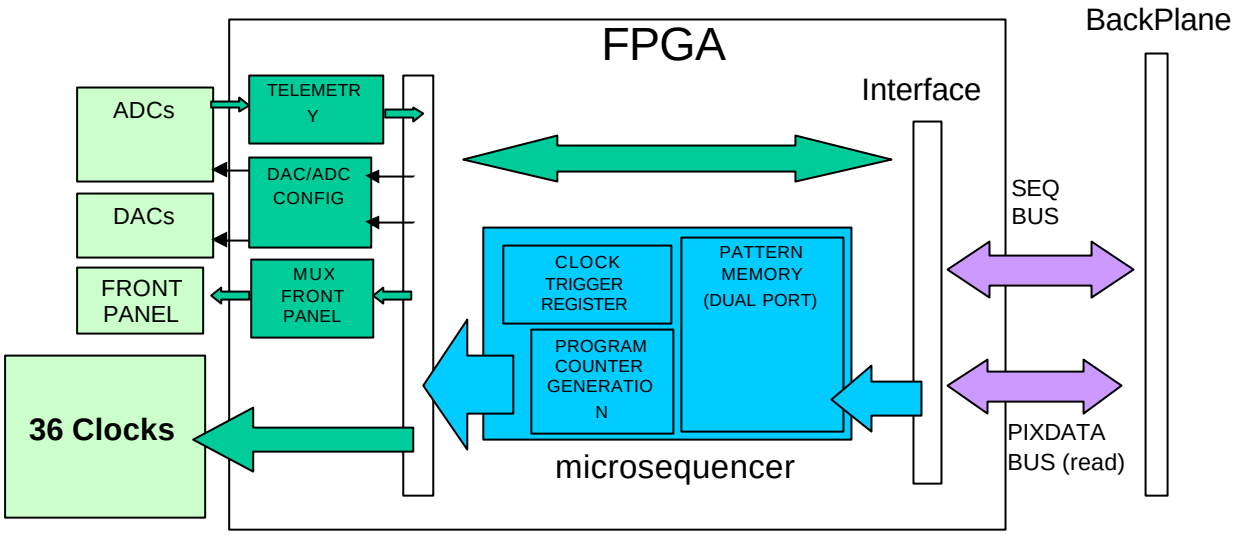
Pin	Z	A	B	C	D	E	F
22	AGND	DCLKOUT78	DCLKOUT93	DCCD7_H2L	DCCD9_H2L	DCCD5_H2U	N/C
21	AGND	AGND	AGND	AGND	AGND	AGND	N/C
20	AGND	DCCD9_H3U	DCLKOUT92	DCCD7_H2L	DCCD8_H2L	DCCD8_H2U	N/C
19	AGND	DCCD7_H3U	DCCD8_H3U	DCLKOUT106	DCCD6_H2U	DCCD6_H2L	N/C
18	AGND	AGND	AGND	AGND	AGND	AGND	N/C
17	AGND	DCCD4_H2L	DCCD4_H2U	DCCD9_H3L	DCCD5_H2L	DCCD9_H2U	N/C
16	AGND	DCCD8_SWL	DCCD8_SWU	DCCD8_H3L	DCCD9_SWL	DCCD9_SWU	N/C

15	AGND	AGND	AGND	AGND	AGND	AGND	N/C
14	AGND	DCCD9_RGL	DCCD7_H3L	DCCD9_N+	DCCD7_SWU	DCCD9_RGU	N/C
13	AGND	DCCD8_H1U	DCCD9_H1U	DCCD8_RGU	DCCD9_V1	DCCD8_N+	N/C
12	AGND	AGND	AGND	AGND	AGND	AGND	N/C
11	AGND	DCCD8_RGL	DCCD7_V1	DCCD7_N+	DCCD7_SWL	DCCD8_V1	N/C
10	AGND	DCCD8_H1L	DCCD9_H1L	DCCD7_H1U	DCCD7_RGL	DCCD7_RGU	N/C
9	AGND	AGND	AGND	AGND	AGND	AGND	N/C
8	AGND	DCCD3_H2L	DCCD2_TG	DCCD9_V3	DCCD8_TG	DCCD3_H2U	N/C
7	AGND	DCCD7_H1L	DCCD6_H3U	DCCD7_TG	DCCD8_V3	DCCD2_H2U	N/C
6	AGND	AGND	AGND	AGND	AGND	AGND	N/C
5	AGND	DCCD6_SWU	DCCD1_H2U	DCCD2_H2L	DCCD7_V3	DCCD3_TG	N/C
4	AGND	DCCD5_H3U	DCCD6_SWU	DCCD9_TG	DCCD5_H1U	DCCD6_H1U	N/C
3	AGND	AGND	AGND	AGND	AGND	AGND	N/C
2	AGND	DCCD4_H3L	DCCD1_H2L	DCCD5_SWU	DCCD1_TG	DCCD4_H1U	N/C
1	AGND	DCCD9_V2	DCCD5_H1L	DCCD4_SWU	DCCD6_H1L	DCCD5_SWL	N/C

Pin	Z	A	B	C	D	E	F
22	AGND	DCLKOUT78	DCLKOUT93	DCLKOUT108	DCLKOUT123	DCLKOUT138	N/C
21	AGND	AGND	AGND	AGND	AGND	AGND	N/C
20	AGND	DCLKOUT77	DCLKOUT92	DCLKOUT107	DCLKOUT122	DCLKOUT137	N/C
19	AGND	DCLKOUT76	DCLKOUT91	DCLKOUT106	DCLKOUT121	DCLKOUT136	N/C
18	AGND	AGND	AGND	AGND	AGND	AGND	N/C
17	AGND	DCLKOUT75	DCLKOUT90	DCLKOUT105	DCLKOUT120	DCLKOUT135	N/C
16	AGND	DCLKOUT74	DCLKOUT89	DCLKOUT104	DCLKOUT119	DCLKOUT134	N/C
15	AGND	AGND	AGND	AGND	AGND	AGND	N/C
14	AGND	DCLKOUT73	DCLKOUT88	DCLKOUT103	DCLKOUT118	DCLKOUT133	N/C
13	AGND	DCLKOUT72	DCLKOUT87	DCLKOUT102	DCLKOUT117	DCLKOUT132	N/C
12	AGND	AGND	AGND	AGND	AGND	AGND	N/C
11	AGND	DCLKOUT71	DCLKOUT86	DCLKOUT101	DCLKOUT116	DCLKOUT131	N/C
10	AGND	DCLKOUT70	DCLKOUT85	DCLKOUT100	DCLKOUT115	DCLKOUT130	N/C
9	AGND	AGND	AGND	AGND	AGND	AGND	N/C
8	AGND	DCLKOUT69	DCLKOUT84	DCLKOUT99	DCLKOUT114	DCLKOUT129	N/C
7	AGND	DCLKOUT68	DCLKOUT83	DCLKOUT98	DCLKOUT113	DCLKOUT128	N/C
6	AGND	AGND	AGND	AGND	AGND	AGND	N/C
5	AGND	DCLKOUT67	DCLKOUT82	DCLKOUT97	DCLKOUT112	DCLKOUT127	N/C
4	AGND	DCLKOUT66	DCLKOUT81	DCLKOUT96	DCLKOUT111	DCLKOUT126	N/C
3	AGND	AGND	AGND	AGND	AGND	AGND	N/C
2	AGND	DCLKOUT65	DCLKOUT80	DCLKOUT95	DCLKOUT110	DCLKOUT125	N/C
1	AGND	DCLKOUT64	DCLKOUT79	DCLKOUT94	DCLKOUT109	DCLKOUT124	N/C

1.3 Data Paths

CB data structure is based in the CBB. CB supports basically the same data paths with the inclusion of a microsequencer. There are three principle data paths associated with the functions of the CB: Control data path, Configuration data path, and Pixel data path. Figure 12 provides a schematic view of these data paths.



Principle Data Paths

Figure 12

1.3.1 Control Data

All control functions are performed using an on-board flat memory (register) address space to provide read and write access to control registers located in the CB FPGA. Generally, the data width of these registers is 16 bits. A few control registers in the lower address space area are 32 bit values. Values written to the registers establish the modes of operation and the synchronization of events. The most important control signals are the switches control lines between voltage levels (ADG713). These switches select between high and low voltage shaping the waves.

1.3.2 Configuration Data

Configuration data is transmitted to the relevant hardware devices through a common synchronous serial link. The serial data stream is generated by the FPGA, where the address of the device is decoded and serial data distributed to the individual hardware component. The main configuration data are DACs values. DACs outputs are high and low voltage levels for clock signals. Before CCD readout, FPGA configures DACs outputs that remain fixed during CCD readout.

1.4 Control Functions

All control and acquisition functions that the CB is capable of are initiated by writing to specific memory locations on the board. There are two parts to forming the 24-bit address to these memory locations. They are the 'board select address' (or slot address), and the 'board register address'.

The 8-bit board select address is defined by the physical position of the Clock board on the DHE backplane. By definition, the Master Control Board (MCB) always occupies board select address 1 and occupies slot 1 of the backplane. Slot positions are numbered from the MCB position in linear fashion up to a maximum of slot 8. Board select addresses are expressed as bit positions in the command word address field during a PAN ⇔ DHE command transaction. See document ICD 6.1 DHE Command and Hardware Interface Definition for additional information. This mechanism allows multiple boards to be accessed in any write or reset transaction. In a similar fashion, the 8-bit board select address is written to the LSR register in the MCB Sequencer register set to access the peripheral boards. Table 5 defines the board select address with respect to the slot position.

Table 5 - Sequencer Bus Address Mapping

Slot Position	Board Select Address	32-Bit Word on Board Register Address Range	16-Bit Word on Board Register Address Range
1	0x010000	0x010000 ⇨ 0x01003F	0x010040 ⇨ 0x01FFFF
2	0x020000	0x020000 ⇨ 0x02003F	0x020040 ⇨ 0x02FFFF
3	0x040000	0x040000 ⇨ 0x04003F	0x040040 ⇨ 0x04FFFF
4	0x080000	0x080000 ⇨ 0x08003F	0x080040 ⇨ 0x08FFFF
5	0x100000	0x100000 ⇨ 0x10003F	0x100040 ⇨ 0x10FFFF
6	0x200000	0x200000 ⇨ 0x20003F	0x200040 ⇨ 0x20FFFF
7	0x400000	0x400000 ⇨ 0x40003F	0x400040 ⇨ 0x40FFFF
8	0x800000	0x800000 ⇨ 0x80003F	0x800040 ⇨ 0x80FFFF

The on-board register address of the Clock board is divided into two areas as indicated in the document ICD 7.0 DHE Backplane Definition. This allows sixty-four 32-bit registers to be defined in the lower board register address space. The rest of the space is occupied by sixteen bit registers. Thirty-two bit space is normally used for functions that are occupied by the MCB Sequencer.

A summary of the memory space for the CB is given in Table 6 followed by a more detailed description of each function.

Table 6 – CB Memory map

Address	Function name	Function description
0x0000	**CLK_CLKPORT**	Set the clocks levels (high / low) for the 32 clock signals
0x0005	**STARTMICRO**	Start microsequencer
0x0100 ⇨ 0x015B	**CLK_HIGHPORT/ CLK_LOWPORT**	Clock rail low or high stage voltage DAC registers for channels. (even high / odd low)
0x01FE	**CLK_GLOBAL_ENBL**	Enables or isolate all clock signal to the backplane connector
0x0170 ⇨ 0x0193	**CLK_TELCLKMODE**	Set the telemetry data mode (ADC MODE) to clock channels
0x01E8 ⇨ 0x01EF	**CLK_TELSUPPLYMODE**	Set the telemetry data mode (ADC MODE) for reading supply voltages
0x01F0 ⇨ 0x01F7	**CLK_TELREFMODE**	Set the telemetry data mode (ADC MODE) for reading refe rences voltages
0x01FF	**CLK_MUXSLCT**	Select which clock signal to be connected to the front panel test ports P1 and P2
0x01FF	**CLK_P1_SLCT**	Select which clock signal to be connected to the front panel test port P1
0x01FF	**CLK_P2_SLCT**	Select which clock signal to be connected to the front panel test port P2
0x0272 ⇨ 0x0277	**CLK_TELSUPPLYDATA**	Telemetry data for supply voltages
0x0278 ⇨ 0x027A	**CLK_TELREFDATA**	Telemetry data for references voltages
0x027C	**CLK_TELCLKREF**	Telemetry data for DAC references voltages
0x0281 ⇨ 0x02A3	**CLK_TELCLKDATA**	Telemetry data for clock channels to read clock voltages
0x1000 ⇨ 0x103F	**CLK_SEQPATMEM**	Load clocks and delays in the microsequencer memory
0xFFF0	**CLK_EVEN_REG**	Global even register used to receive event strobe
0xFFF9	**CLK_LEDCTL**	Front panel LED indicator configuration register
0xFFFA	**CLK_SERNUM**	Electronic serial number read only register
0xFFFB	**CLK_TEMP**	Access to the local board temperature sensor
0xFFFC	**CLK_CTLREG**	Read / write the global control register for the board
0xFFFD	**CLK_STATUS**	Read the board status register
0xFFFE	**CLK_IDENT**	Board function identity register + shadow reset
0xFFFF	**CLK_FIRMVERS**	Board firmware version register + shadow reboot
0xFFFE	**CLK_RESET**	Writing this location causes hard reset Does not affect configuration data
0xFFFF	**CLK REBOOT**	Writing this location causes soft reset (reboot) on the board with default configuration values

1.4.1 Clock Control Register (CLK_CLKPORT)

Writing a 32 bit value to this register establishes the level of the 36 clock signals. Each bit of this register corresponds to one clock signal (Bit 0 = V1, Bit 1 = V2, etc.). When a clock register bit is set high (1) then the voltage programmed by the corresponding clock high level DAC (CLK_HIGHPORT) is output on the clock signal. When a clock register bit is set low (0) the voltage programmed by the corresponding clock low DAC register (CLK_LOWPORT) is output on the clock signal. Note that it is permissible for the clock high DAC register to be programmed with a lower voltage than the clock low DAC register. The register may be written at anytime. However, the Clock Enables Register (CLK_GLOBAL_ENBL) bit 3 must be set true to enable the Clock signals output on connector.

Table 7 - Clock Control Register Description (CLK_CLKPORT)

[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
N_GUARD	H2	SW	RG	H3U	H3L	H1U	H1L	SW	RG	H3U	H3L	H1U	H1L	SW	RG
[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
H3U	H3L	H1U	H1L	TG	V3	V2	V1	TG	V3	V2	V1	TG	V3	V2	V1

Color code

Group A
Group B
Group C
common

The bits of Clock Control register are divided in groups. The red group ([0:3] and [12:17]) along with N_Guard and H2 ([30:31]) (common signals for all groups) controls one CCD. Green group ([4:7] and [18:23]) and common signals controls other CCD. Finally last group, blue one ([8:11] and [24:29]) and common signals controls the third CCD. In addition, the signals of each group are replicated by means of drives, so each group can controls two additional CCDs. Thus, one group of signals can control up to three CCDs with the same timing and voltage levels. The bit order selected is motivated by how signal may be shared between both sides of CCD.

N_Guard is a digital signal who controls all N_guard switches. N_Guard switches either to connect or isolate N_Guard lines to ground.

H2 bit is used to controls 3 different clocks, one of each group. Each H2 may be configured with different voltage levels, but only one bit [31] controls the H2 clock timing.

1.4.2 Clock board Microsequencer Trigger Command Register (STARTMICRO)

Writing to this port initiates a sequence of horizontal clocks to control the charge displacement. The clocks are generated by a micro-sequencer built into the CB FPGA. The state sequence is previously stored as a list in the CB_PAT_MEM area as individual states that define the bit vectors to control the transitions and associated delay for the states. To initiate the sequence a 16-bit data word with both the start address (expressed as an offset

from the first register address space) and the run length of the sequence is written to this register. Table 8 shows the bit field position in the data word.

Table 8 – CB (micro) sequencer trigger register (STARTMICRO)

	MICROSEQUENCER TRIGGER COMMAND DATA WORD		
BIT	[15]	[14:8]	[7:0]
signal	UNUSED	RUN LENGTH OF SEQUENCE	START ADDRESS OF SEQUENCE

When reading this register the RUN LENGH OF SEQUENCE field will reflect the last address issued by the sequencer after the most recent write to this register i.e. it is the effective address where the sequencer stopped after the last run.

1.4.3 Clock High/Low Voltage Registers (CLKNAME_HIDAC/ CLKNAME_LOWDAC)

The clock high/low DACs can be programmed by means of these sixty six 8-bit registers (Tables 9a, 9b). Reading these registers returns the last value written to them. The selection between high and low DACs for each clock is performed by means of Clock Control Register (1-high, 0-low).

Table 9 - Clock High/Low Voltage Registers addresses (CLKNAME_HIDAC) / (CLKNAME_LOWDAC) description

Group A											
Signal	V1	V2	V3	TG	RG	H3U	SW	H1U	H3L	H1L	H2
CKL_HIGH	0x0140	0x0142	0x0144	0x0146	0x0158	0x0156	0x015A	0x014A	0x0150	0x0148	0x0154
CKL_LOW	0x0141	0x0143	0x0145	0x0147	0x0159	0x0157	0x015B	0x014B	0x0151	0x0149	0x0155
Group B											
Signal	V1	V2	V3	TG	RG	H3U	SW	H1U	H3L	H1L	H2
CKL_HIGH	0x0120	0x0122	0x0124	0x0126	0x0138	0x0134	0x0136	0x0130	0x0132	0x0128	0x0152
CKL_LOW	0x0121	0x0123	0x0125	0x0127	0x0139	0x0135	0x0137	0x0131	0x0133	0x0129	0x0153
Group C											
Signal	V1	V2	V3	TG	RG	H3U	SW	H1U	H3L	H1L	H2
CKL_HIGH	0x0100	0x0102	0x0104	0x0108	0x010A	0x0110	0x0112	0x0114	0x0116	0x0118	0x012A
CKL_LOW	0x0101	0x0103	0x0105	0x0109	0x010B	0x0111	0x0113	0x0115	0x0117	0x0119	0x012B

1.4.4 Clock channel chain description

The clock voltage register sets low/high voltage level as is shown in Figure 13. The DAC output ranges from 0v to 2.5v. After the switches, two gain stages are applied to the signals. The gain of the first stage (before global enable switch) is 5 and the gain of the second stage is 2. Also, an offset is added in the first gain stage in order to generate an alternate signal. The behavior of each channel is described in next paragraph.

Firstly, the FPGA configures the DAC high and low voltage levels both connected to the switch input. The FPGA controls the switch by means of CLK_CLKPORT register for selecting between high or low voltage levels. By mean of this control the switch will connect alternatively only one voltage level to the output. This alternate signal is amplified (G1 = 5) and subtracted an offset in the first Op. Amp. At this point, the signal is

completely generated (except final gain that multiply signal by 2) and is connected to the telemetry system. The FPGA controls a global switch that allows all clock signals to pass to the next amplification stages by means of the activation of **CLK_GLOBAL_ENBL** signal. Next, the clock signals are replicated up to three and their voltage multiply by 2 (G2=2) in the second Op. Amp Cable drivers. It may be interesting to allocate these switches at the end of the board after the cable drivers. Nevertheless since signals are replicated (x3) much more components are needed. The telemetry can be use in order to confirm voltage levels while the Front Panel Port for monitoring the output signals.

Table 10 - Clock Voltage Values Description

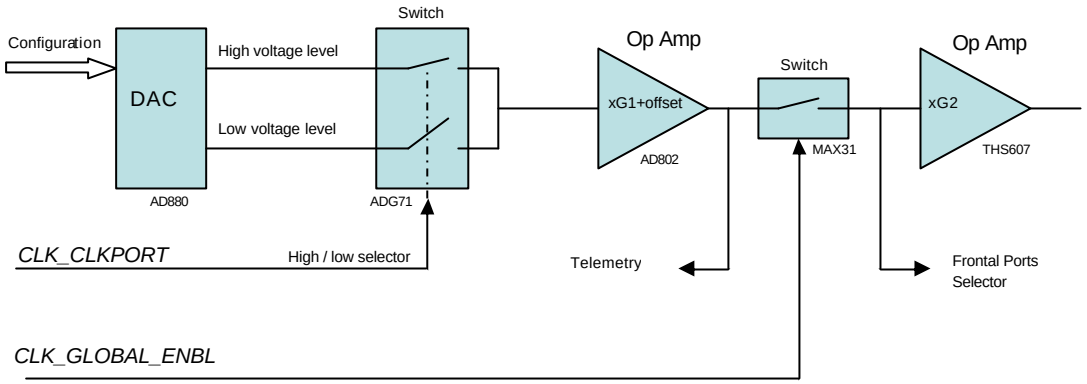
DAC value (hex)	DAC value (dec)	DAC output	Output voltage
0x00	0	0	-12.5
0x16	34	0.333	-10
0x68	132	1.294	0
0xE9	233	2.284	+10
0xFF	255	2.5	+12.5

1.4.5 Clock Enable Register (CLK_GLOBAL_ENBL)

This 16-bit register controls the application (i.e. enabling) of clock voltages to the rear connectors J4 and J5. Table 11 shows the significance of the bits in this register. A bit set true in the register enables that group of voltages to the rear connector. Reading this register returns the value last written to it.

Table 11 - Clock Enables Register Description

[15:4]	[3]	[2]	[1]	[0]
Not used	EN	Not used	Not used	Not used



Vref = DAC output range 0- 2.5 v (8 bits)
CLK = generic clock DAC value.
*Voffset = 6.25v: generated from 1.25v voltage reference. Voffset = 5*1.25= 6.25*
G1 = 5: First stages gain
Vclk = output value after fist gain stage.
G2 = 2: Second stages gain
Vout = final output value.

Formula	*maximum value*	*minimum value*
Vref = 2.5[CKL]/ 255*	*Vref = 2.5 * [255]/ 255 = 2.5v*	*Vref = 2.5 * [0]/ 255 = 0v*
Vclk =G1(Vref) –Voffset*	*Vclk = 5*(2.5) – 6.25 = 6.25v*	*Vclk =5*(0) – 6.25 = -6.25v*
Vout = G2 Vclk*	*Voutmax = 2*(7) =+12.5v*	*Voutmin = 2* (-5) = -12.5v*

Then the resolution may be calculated:
Maximum range ±12.5 = 25v
Linear range ±10 = 20v
DAC Range 200
***Resolution** = 20v/200 = 100 mV*

P.D. : In version 1.0 we use range [-10/+14v] as calibration range. This range produces small accuracy errors in top limits (above +13v) due DAC saturations. DAC loses linearity in higher DAC values. Furthermore bottom limit (-10v) is difficult to overtake.

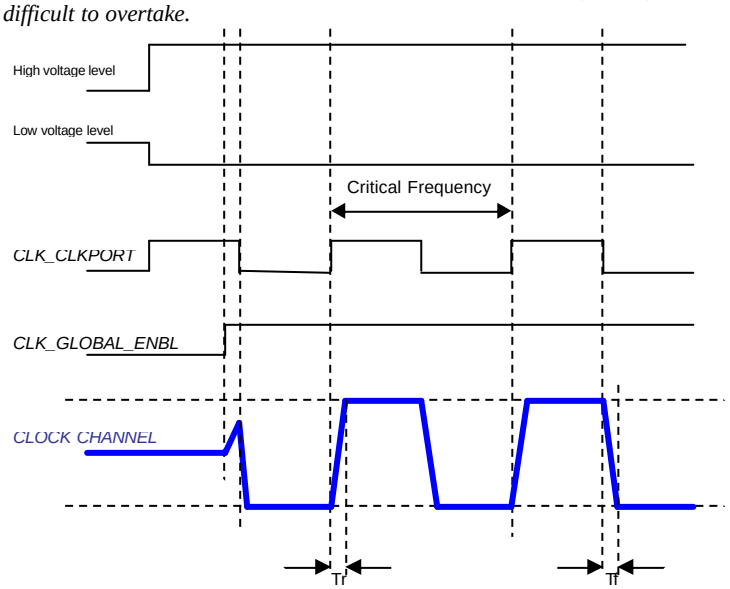


Figure 13. Clockout Signal Path and voltage register

1.4.6 Clock Voltage Telemetry Mode Registers (CLK_TELCLKMODE)

These thirty-six 16-bit registers allow the setting of the voltage range and mode of the telemetry channel ADC associated to the clock voltage telemetry functions. The nominal voltage of the ADC is 5v or 10v full scale. The mode bit is used to control the coding of the ADC to be either 12-bit two-complement bipolar or 12-bit unipolar depending on the voltage range set for the bias voltage signal through the voltage reference jumpers. Table 14 shows the bit significance of these registers. Note that depending on the mode and range selected, the scale and offset values used in the attribute calculations require adjustment to accommodate the data. These registers are set by default to their normal values (0xD i.e. ± 10V Range, external clock mode) after power on or reboot function. Reading these registers returns the value last written to them.

Table 12 - MAX 1207 Bits Description

Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
RNG	BIP	PD1	PD0

Table 13 - MAX 1207 Mode Description

PD1	PD0	Mode
0	**0**	Normal operation (always on) Internal clock mode
0	**1**	Normal operation (always on) External clock mode
1	**0**	Standby Power-Down Mode (STBYPD) Clock mode unaffected
1	**1**	Full Power-Down mode (FULLPD) Clock mode unaffected

Table 14 - MAX 1207 Range and Polarity Description

Input Range	RNG	BIP	Negative Full Scale	Zero Scale (V)	Full Scale
0 to 5V	**0**	**0**	-	**0**	V_{REF} 1.2207
0 to 10V	**1**	**0**	-	**0**	V_{REF} 2.4414
±5V	**0**	**1**	-V_{REF} 1.2207	**0**	V_{REF} 1.2207
±10V	**1**	**1**	-V_{REF} 2.4414	**0**	V_{REF} 2.4414

1.4.7 Supply Voltage Telemetry Mode Registers (CLK_TELSUPPLYMODE)

These eight registers provide the mode and range selection for those telemetry channels dedicated to monitor the power supplies. Similarly, these registers are set by default to the value of 0xD (i.e. +/-10V, external clock) and the range extended by a series resistor in the appropriate signal line. The mode bit significance is shown in Figure Table 12.

Table 15 - Voltage Telemetry Address Description

	Voltage Telemetry Address							
Signal	**GND**	**GND**	**+VAC**	**-VAC**	**P15**	**N15**	**+5VA**	**-5VA**
Write	0x0000	0x0001	0x0002	0x0003	0x0010	0x000F	0x0011	0x000D
read	0x0270	0x0271	0x0272	0x0273	0x0274	0x0275	0x0276	0x0277

1.4.8 Reference Voltage Telemetry Mode registers (CLK_TELREFMODE)

Finally, eight registers that enable the mode and range to be set for those telemetry channels dedicated to monitor the DAC and offset reference supplies. Similarly, these registers are set by default to the value of 0xD (i.e. +/-10V, external clock) but the range is not extended for these signals. The mode bit significance is shown in Table 15.

1.4.9 Front Panel Clock Monitor Port Select Register (CLK_MUXSLCT, CLK_ P1_SLCT, CLK_ P2_SLCT)

Two front panel connectors (P1, P2) are provided to monitor the state of any out of 36 clock signals. These two buffered ports are independent and allow two clocks to be sampled simultaneously. This 16-bit register allows the selection of the clock signals multiplexed to P1 and P2. The signal available at these connectors, located in Front panel in Figure 6, is taken from the rear connector point and is therefore after the enable switches but before the final cable drivers. This means that the clocks should be enabled to allow the clock signal to be monitored. The bit significance of this register is shown in Table 16. In addition, bits 12 and 13 control LED (D5) and DISABLE_LEDS respectively. And bits 14 and 15 configure two digital output channel currently assigned to shutter and trigger. Reading this register returns the value last written to it. Could be used CLK_MUXSLCT for all register or only may be modified partially Port, used CLK_ P1_SLCT for Port P1 and CLK_ P2_SLCT for Port P2.

Table 16 - Front Panel Clock Monitor Port Select Register Description

[15]	[14]	[13]	[12]	[11:6]	[5:0]
IO1	IO2	LEDS_DISABLE	LED	P2 CLOCK MUX SELECT	P1 CLOCK MUX SELECT

Table 17 shows a way for selecting a clock line in Ports P1 and P2 using hexadecimal codification. For example if you want to select H3L of Group C in Port P1 and V2 of Group A in Port P2 the values are 0x001A and 0x0040 respectively. You should send to the CLK_MUXSLCT the OR value as is shown in Table 17: 0x0040 | 0x001A = 0x005A, CLK_MUXSLCT 0x005A.

Table 17 – Front Panel Clock Monitor Port Channel Select Values (hexadecimal)

groupA											
Signal	V1	V2	V3	TG	H1L	H1U	H3L	H3U	RG	SW	H2
P1	0x0000	0x0001	0x0002	0x0003	0x000C	0x000D	0x000E	0x000F	0x0010	0x0011	0x001E
P2	0x0000	0x0040	0x0080	0x00C0	0x0300	0x0340	0x0380	0x03C0	0x0400	0x0440	0x0780
groupB											
Signal	V1	V2	V3	TG	H1L	H1U	H3L	H3U	RG	SW	H2
P1	0x0004	0x0005	0x0006	0x0007	0x0012	0x0013	0x0014	0x0015	0x0016	0x0017	0x001F
P2	0x0100	0x0140	0x0180	0x01C0	0x0480	0x04C0	0x0500	0x0540	0x0580	0x05C0	0x07C0
groupC											
Signal	V1	V2	V3	TG	H1L	H1U	H3L	H3U	RG	SW	H2
P1	0x0008	0x0009	0x000A	0x000B	0x0018	0x0019	0x001A	0x001B	0x001C	0x001D	0x0020
P2	0x0200	0x0240	0x0280	0x02C0	0x0600	0x0640	0x0680	0x06C0	0x0700	0x0740	0x0800

1.4.10 Power Supply Voltage Telemetry Data Registers (CLK_TELSUPPLYDATA)

These eight registers are used to control the telemetry ADC devices and obtain a telemetry data value representative of the voltage value for the selected power supply. To read a value from the telemetry ADC you must first write a value to order conversion register that you desire to read. The actual data value written is not significant and only serves to trigger an ADC conversion cycle. After approx 30us the data value is available to be read from the same location.

1.4.11 Reference Voltage Telemetry Data Registers (CLK_TELREFDATA)

These eight registers are used to control the telemetry ADC devices and obtain a telemetry data value representative of the voltage value for the selected reference supply. To read a value from the telemetry ADC you must first write a value to order conversion register that you desire to read. The actual data value written is not significant and only serves to trigger an ADC conversion cycle. After approx 30us the data value is available to be read from the same location.

Table 18 - Voltage Telemetry Address

	Voltage Telemetry Address							
Signal	REF0	REF2	REF4	2V5DAC	1V25REF	GND	GND	GND
Write	0x0000	0x0001	0x0002	0x0003	0x0010	0x000F	0x0011	0x000D
read	0x0279	0x027A	0x0278	0x027B	0x027C	0x027D	0x027E	0x027F

1.4.12 Clock Voltage Telemetry Data Registers (CLK_TELCLKDATA)

These thirty-six registers are used to control the telemetry ADC devices and obtain a telemetry data value representative of the voltage value for the selected clock channel. To read a value from the telemetry ADC you must first write a value to the order conversion register that you desire to read. The actual data value written is not significant and only serves to trigger an ADC conversion cycle. After approx 30us the data value is available to be read from the same location. If **CLK_GLOBAL_ENBL** are disable then clock signal are not available in backplane but ADCs take samples before switches and show a correct value in registers. Also telemetry data register show the configured levels values (**CLK_ HIGHPORT** or **CLK_LOWPORT**) when **CLK_GLOBAL_ENBL** is enable and **CLK_CLKPORT** is fixed at high or low value (see Figure 13).

1.4.13 Clock board Microsequencer Pattern Memory Register (CLK_SEQPATMEM)

These 256x32-bit memory contains the clock bit patterns and associated timing delay information required to shift horizontally the charge (one pixel position) toward the output of the CCD. Clock sequence is defined by writing successive memory locations with the required clock state and timing information. The transition of one state to the next (i.e. transition to successive memory locations) is controlled by the trigger word written to the CB_SEQTRIG register and the time delay information carried in the least significant eight bits of the memory words. Table 19 shows bit fields for words written to these registers.

Table 19 – CB MicroSequencer Pattern Memory Bit Fields

	CB MICROSEQUENCER PATTERN MEMORY															
CLK	**[31]**	**[30]**	**[29]**	**[28]**	**[27]**	**[26]**	**[25]**	**[24]**	**[23]**	**[22]**	**[21]**	**[20]**	**[19]**	**[18]**	**[17]**	**[16]**
signal	UN.	H2	SW	RG	H3U	H3L	H1U	H1L	SW	RG	H3U	H3L	H1U	H1L	SW	RG
group		A,B,C	C	C	C	C	C	C	B	B	B	B	B	B	A	A

	CB MICROSEQUENCER PATTERN MEMORY					
CLK	**[15]**	**[14]**	**[13]**	**[12]**	**[11:8]**	**[7:0]**
signal	H3U	H3L	H1U	H1L	UNUSED	DELAY value in units of 25 ns
group	A	A	A	A		

Bits from 12 to 30 are assigned to horizontal clock signals dedicated to specifics group of CCDs. The last significant eight bits define the time (delay) the current clock pattern is applied. After this delay the memory address is incremented and the next clock pattern is issued. This sequence is repeated until the number of states issued by the micro-sequencer is equal to the run-length field written in the STARTMICRO register. The micro-sequencer is initiated by writing the index of the first state (of the pattern memory) to the start address

bit field of the STARTMICRO register along with the run length for the sequence. Normally, the state bit patterns and delays are developed to coincide with the sequencer signal pattern generated by the CCDACQ for the CDS signal processing. The pixel acquisition is then performed by synchronizing the CCD micro-sequencer, the CB micro-sequencer and events produced by the MCB sequencer. Using this technique considerably reduces the amount of sequencer bus transactions by eliminating from the MCB sequencer those needed to control the CDS signal processor and horizontal clock sequencing. The 256 memory locations allow sufficient state space to accommodate multiple and distinct sequences that can be triggered by the selection of the start address field in STARTMICRO register.

1.4.14 Global Event Register (CLK_EVENT_REG) (not implemented)

The Global Events register is designed to provide a common and synchronized event signaling mechanism across all peripheral boards in a DHE chassis. Events can be issued by a PAN write to the appropriate board address or from the MCB sequencer. There are currently two such events defined. Table 20 lists the bit fields of this register.

Table 20 - Global Event Register. Bit Fields Bit Event Name Purpose

[15]	[14:1]	[0]
START_EXPOSURE	Not used	START_FRAME

START_EXPOSURE: Issued at the beginning of a pixel acquisition that will result in a new image file being produced.

START_FRAME : Issued at the beginning of a pixel acquisition cycle that will be used to build up the current image file.

NOTE: Currently these events are only used as an aid to function debugging i.e. to identify when such events have occurred.

1.4.15 Front Panel LED Control Register (CLK_LEDCTL)

The least significant three bits of this register control the function of the board front panel indicator LED (D1). This indicator provides base level diagnostic information on the functionality of the board. After power on or a reboot, the indicator will be on permanently until the first valid sequencer bus transaction has occurred. After this, writing to one or more of the control bits will provide a 10ms indicator flash each time the specific function goes true. The functions that can be assigned as triggers to illuminate this LED are as follows:

Bit Function 0 Flash each time the board is selected on the sequencer bus (**/SEL**) 1 Not Used. 2 Not Used.

Front panel Ports

Figure 14

1.4.16 Silicon serial number register (CLK_SERNUM)

Reading this register returns a 32-bit word that is a unique serial number read from U283.

1.4.17 Board temperature register (CCD_TEMP)

Reading this register returns a 10-bit signed number that indicates the current ambient temperature of device U282. This is representative of the operating temperature of the board. Each LSB corresponds to 0.25deg. C. The temperature is read from FPGA by first writing to this register with non-significant data, then waiting for at least 35 microseconds before reading the register that contains the new value.

1.4.18 Board Control Register (CLK_CTLREG)

This 16-bit register controls the major mode of operation of the board. The current firmware does not use this register.

1.4.19 Board Status Register (CLK_STATREG)

This read only 16-bit register contains status information from various functions on the board FPGA. Bit significance is shown in Table 21 below.

Table 21 - Board Status Register

[15:9]	[8]	[7:0]
Not used	SILICON SER NUMBER CRC OK	CFG STATE MACHINE STATUS_FRAME

1.4.20 Board Identity Code Register (CLK_IDENTREG) (CLK_RESET)

Reading from this address will return data that identifies this board as a Clock Board (Code = 0x002, for CBv2.1). Writing to this address will result in the board going through a soft reset cycle. Current configuration data will not be affected and all state machines will be reset to their idle state.

1.4.21 Firmware Code Revision Register (CLK_ FIRMVERS)(CLK_REBOOT)

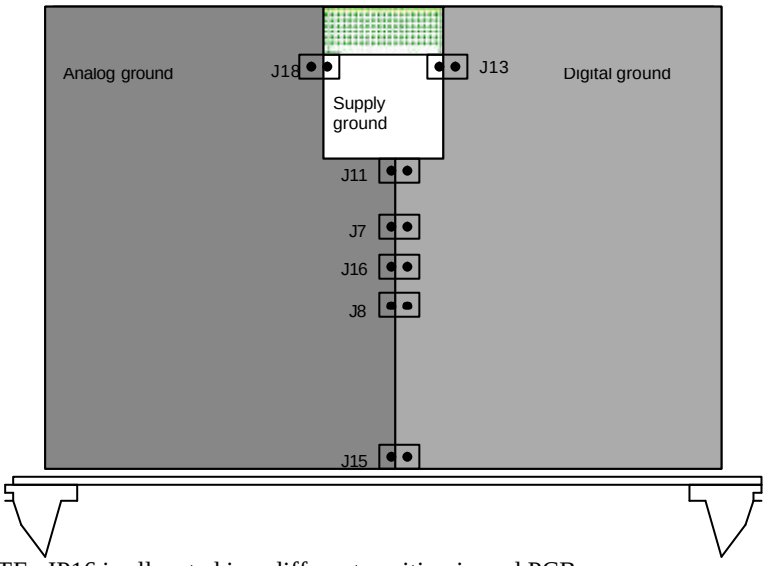
Reading from this address will return data that will identify the version of firmware running on the board. The data is returned in fixed point decimal that should be divided by 100 to find the correct major and minor version number (XX.nn). Writing to this address will result in the board going through a hard reset cycle. This will set to true the firmware signal TPS_RESET_N which results in a reloading of the firmware of the board FPGA. This will reset all configuration data to default power up values.

1.4.22 CLK Leds disable (CLK_LEDS_DISABLE)

All front panel leds can be disable/enable by means of bit 13 of mux register. When programmed, the **CLK_ LEDS_DISABLE** command can be used for this task.

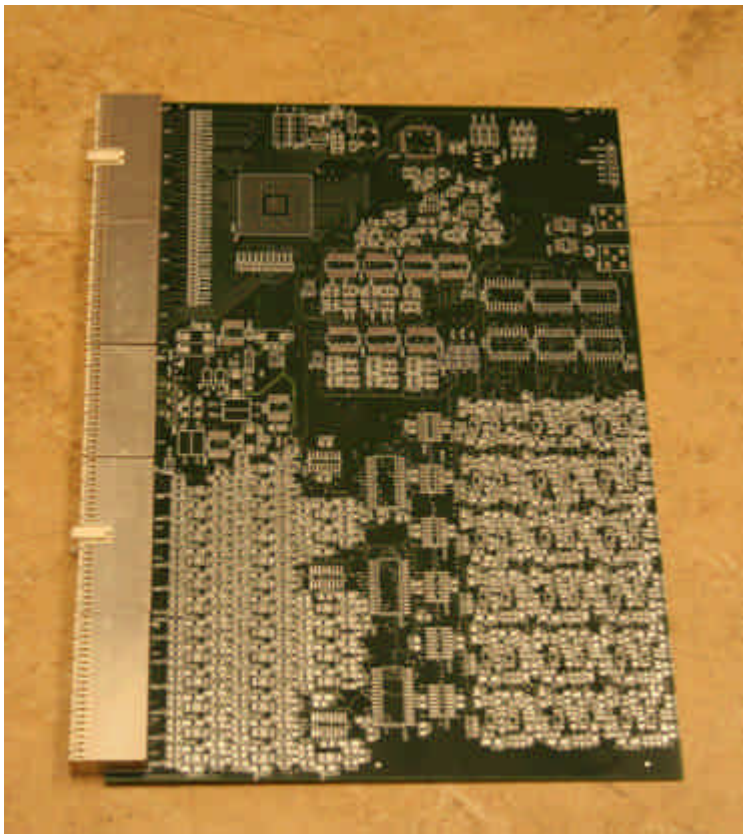
2.0 Board Hardware Description

There are three power supplies required by the CB. The board is divided in two different areas, analog and digital areas. The return of two each area is isolated from the other area. There are some jumpers that make possible to join both areas in different places as can see in Figure 15 (JP7, JP8, JP11, JP13, JP15, JP16, and JP18).



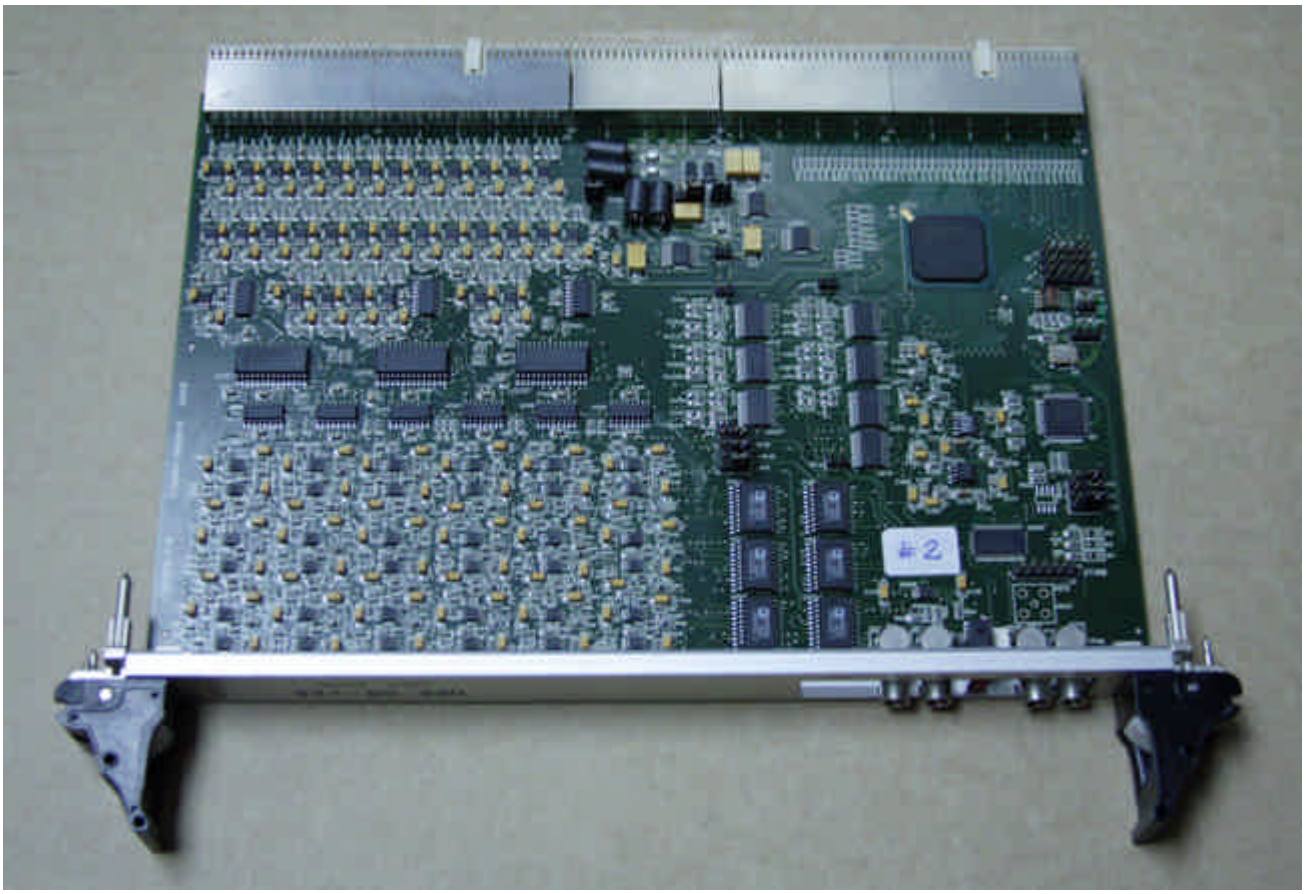
NOTE: JP16 is allocated in a different position in real PCB.

Figure 15. **Ground Jumpers situation**



Clock board V1 picture

Figure 16



Clock board V2 picture

Figure 17

Clock board V2 picture

Figure 18

2.1.1 Digital Supplies

The majority of the logic is powered from a 3.3v supply (**+3.3VD**). This supply can be supplied directly from the backplane (**+3.3VDIN**) or generated on board by U288(TPS75233). U288 is supplied from 5Vd (**+5VDIN**). The jumpers JP6 select the source for this supply. The internal logic cell of the FPGAs requires 2.5v (**+2.5V**) that is generated on board by U289(TPS75225). U289 is supplied internally from the **3.3VD** supply rail. The nominal current drawn on these supplies are shown in Table 22.

2.1.2 Analog Supplies

The analog supplies come to the board directly from the backplane. They power all generation clock components. The nominal current drawn on these supplies are shown in Table 22.

2.1.3 Renamed schematics codification.

The schematic v2.0 is not intuitive and is hard work with it. There is a new schematic version where the names of the signals are renamed with the correspondent CCD signal. CB 2.0 generates clk signals in order to control 9 CCD. The CCD are labeled from 1 to 9 (CCD1,CCD2,…).

FPGA controls digital lines which produces swapping between high and low voltages. These signals are labeled **CLK*X*_"CCDsignal"**. Where X are the CCD names controlled by this signal. Remember that in this step there are 3 CCD controlled by this signal. For example **CLK*123*_V1**. "CCDsignals" are described in 1.4.1 (Clock Control Register). In voltage generation outputs , signals are labeled as **VCCD*X*_"CCDsignal"**. Then in global enable switch output are labeled as **CCD*X*_"CCDsignal"**. The relationship of the signal keep the same name:

CLK*123*_V1 => VCLK*123*_V1 => CCD*123*_V1

Signal are replicated in cable drivers step, and then, they are labeled with the name of CCD For example:

=> CCD*1*_V1
CCD*123*_V1 => CCD*2*_V1
=> CCD*3*_V1

In this case V1 is replicated x3 but RG, SW and H2 are replicated x6.
For example, for H2 signal we have:

=> CCD*7*_H2U
=> CCD*7*_ H2L
=> CCD*8*_ H2U
CCD*789*_H2 => CCD*8*_ H2L
=> CCD*9*_ H2U
=> CCD*9*_ H2L

The path of H2 for CCD4 is:

CLK*456*_H2 => VCLK*456*_H2 => CCD*456*_H2 => CCD*4*_H2U
=> CCD*4*_H2 L

Table 22 - Power Supply Current Draws

Digital Supply Rails	Quiescent	Peak	Watts
+5.0 Vd (with separate 3.3V supply)	0.09 Amp		0.45 W
+3.3 Vd	0.11 Amp		0.36 W
Digital Supply Rails	Quiescent	Peak	
± 5.0 VA	0.04 Amp		0.40 W
±15.0 VA	0.90 Amp		27.00 W

Note: Measure power consumption without load and all clock voltage set to 0 V.

2.2 Logic Section

2.2.1 Reset and FPGA Boot Logic

A power-on reset active low signal is generated by the linear supply U289. This signal (**/PROGRAM**) is asserted for 100ms after the core voltage becomes stable. When this signal is released, the FPGA device begins the boot process that involves sequencing the signals **/INIT** low then high, asserting **/DONE** false and supplying a clock to the **CCLK** pin. This resets the EEPROM (U232) internal address counter, enables the data output through DIN signal, and begins serially transferring the function code to the FPGA core. After the load sequence is complete, the FPGA takes the **DONE** signal high and executes an internal startup sequence that, finally, enables the output pins of the FPGA. This process takes approx 30 ms to complete. The same process as a power on reset can be forced either by a PAN command (writing to the CLK_REBOOT register) or via the jumper (front panel switch in next version) JP9 which merely takes the **/RST_N** signal low while activated and that is coupled internally to the FPGA to the same **/ PROGRAM** signal.

2.2.2 JTAG Interface

The front panel JTAG connector (J6) provides access to the boot EEPROM device and the FPGA. The chain order is FPGA BOOT (XC1802VQ44 EEPROM), FPGA (Spartan II XC2S200-6FG456). The front panel connector pin assignment is designed reduce the lines needed. See Table 23.

Table 23 - JTAG Pin Assignments

Pin	Function	Pin	Function
1	+3.3VD	1	+3.3VD
2	TCLK	2	DGND
3	DGND	3	KEY
4	TDO	4	TCLK
5	TDI	5	N.C.
6	TMS	6	TDO
7		7	TDI
8		8	TMS

2.2.3 Firmware version.

There are several firmware versions available for CB.

V1- 22/10/06 - obsolete (use only with TCB 1.0)
V2v2t2- 22/10/08 – obsolete (use only with TCB 1.0)
V2 – for CBv2.x and TCBv2.0 (compatible with CBv1.0)
V3.4 - for CBv2.x and TCBv2.0 (compatible with CBv1.0)
V4.00 - for CBv2.x and TCBv2.0 (compatible with CBv1.0)

2.3 Options for Building the Clock Board

Not implemented

2.4 Telemetry system

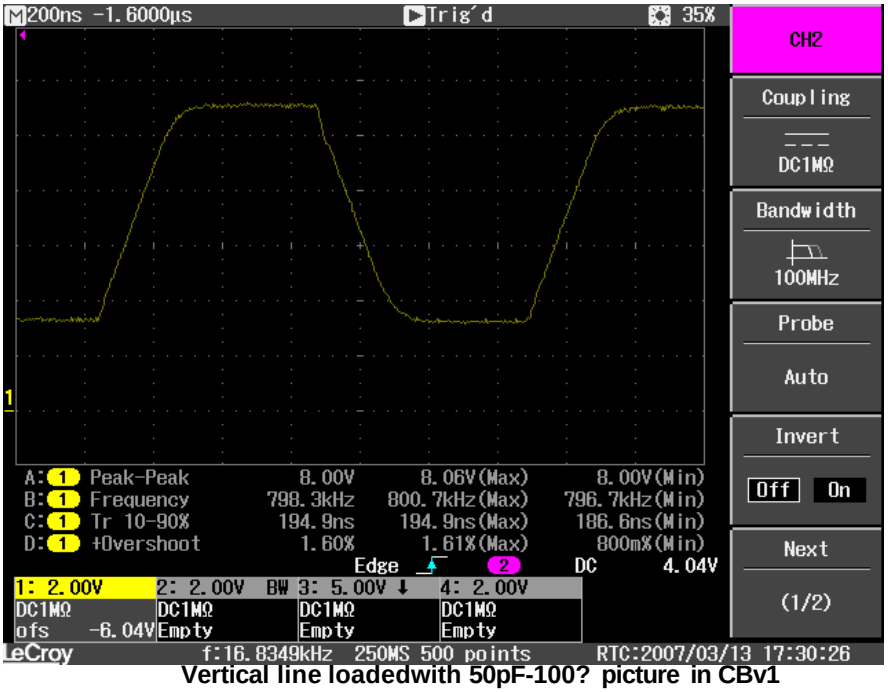
The CB board supports 40 telemetry channels which are used to readback the clock voltages and voltage references. Telemetry ADCs are 12-bits and return data in either straight binary to twos complement form depending on how they are configured. To request that a telemetry ADC begin a new conversion simply write anything to the corresponding telemetry register, as is shown in Table 8. A short time later the requested data will be available to be read from the readout register. While the telemetry module is busy the user should consider all of the telemetry data to be invalid.

2.4.1 Telemetry Channels configuration

Each telemetry channel has four configuration bits which control how the ADC operates. These bits are: Range (RNG), Bipolar (BIP), and two power down control bits (PD1, PD2). These configuration bits are accessible from the Monsoon sequencer bus interface and may be read or written at any time. Refer to the register definitions.

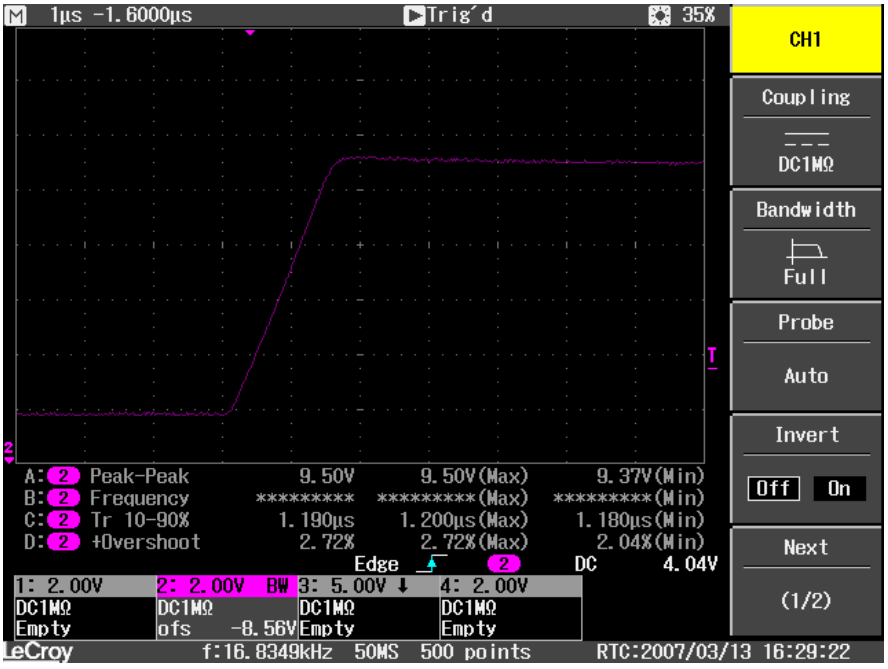
The range and bipolar bits define the ADC analog input voltage range. These bits should both be set to configure the ADC for -10V to +10V operation. Clock channels are digitalized before final gain so all clock channel has for -5V to +5V range. Voltage references are included in the same range, but some of them (supply voltage) are not included in ±10 range, there are resistor dividers on the ADC input that divides by 2 this signals. Calibration files correct adequately each value by software. If the ADC is in bipolar mode the data will be returned in two-complement form. At present time we recommend that the power down control bits (PD1 and PD2) should be cleared, which will leave the telemetry ADC powered up continuously. When the board powers up, these configuration bits are set to zero by default.

A board reset will not change the values of these bits. These configuration bits are transferred to the ADC only when a conversion is requested.



Vertical line loadedwith 50pF-100? picture in CBv1

Figure 19



Horizontal line loaded with 30nF-470? picture in CBv1

Figure 20

2.5 Jumper Descriptions

Table 24 - Configuration Jumper Descriptions

Jumper Number	Label Name	Default Condition
JP1		2-3
JP2		2-3
JP3		2-3
JP4		Off
JP5		1-2
JP6		1-2
JP7		Off
JP8		Off
JP9		Off
JP10		1-2
JP11		Off
JP12		1-2
JP13		On
JP14		
JP15		On
JP16		Off
JP17		Off
JP18		

Table 25 - Test Point Functions

Test Point Number	Label Name	Function

3.0 Board Specifications

Table 26 – Specifications

+5.0V digital @ 0.1 amp average, +3.3V digital @ 0.11 amp average, +15.0V analog@ 0.9 amp average (max. 2.0 amp), -15.0V analog @ 0.9 amp average (max. 2.0 amp), +5.0V analog @ 0.09 amp average.
28.3 Watts
Board temperature + serial number
±10V programmable clock generator, -3.3v and 5v logic-compatible, 100 mV resolution

Bare board: Height - 233 mm (6U) Depth - 160 mm Thickness - 1.6 mm
Fully populated: Height – 233 mm (6U) Depth - 208 mm Thickness - 20 mm

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