MONSOON – Torrent

Firmware User Guide

For firmware version 2.22

Document revision 2.0

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General discussion

The firmware component of Torrent Detector Head Electronics (DHE) resides wholly within a Xilinx Virtex-5 FPGA device (**LCB:U27**) mounted on the Local Control Board (LCB). The firmware (and hence the Virtex-5 device) controls all functionality of the Torrent DHE. This includes control tasks such as system clock generation, communications, command decoding, power supply control, detector clock sequencing, detector bias and clock voltage setting, etc.

To accomplish the control tasks the firmware relies on values that are written to specific memory locations defined within the firmware. Writing to and reading from the DHE memory locations is through one or various available DHE communications channels using a protocol described in the MONSOON Interface Control Document 6.1 section 5.

The protocol allows a Pixel Acquisition Node (PAN) computer to synchronize communications to a DHE, write and read 32-bit words to designated locations in the firmware of the DHE, and start an exposure sequence.

The defined memory locations in the firmware are called ‘Attributes’ and described in the firmware source documents as formatted comments. The value of these attribute are therefore the principle method used to control the firmware function and the hardware of the Torrent DHE.

Architecture

Most of the source documentation for the firmware is written in vhdl code. The top, System level and each intermediate modules are described as schematics to better document the module dependence. There are six main modules and one bus stub associated with the firmware for Torrent. The modules are inter-connected by an internal time multiplexed bidirectional bus. The bus system is adopted from the SOC industry Wishbone standard. There are seven slave devices and two master devices on the bus. Each module is self contained and designed to control a specific area of the Torrent DHE.

The modules are:

Clock Services (CLK_Services) – Controls the configuration process of the clock generator device and responsible for clock switching and multi-DHE synchronization logic.

Local Control Board control (LCB_Control) – which carries responsibility for communications and PAN command parsing. This is a Wishbone bus master.

Power Supply Services module (PSM_Services) – This firmware controls the synchronization, sequencing, safeguarding, and the adjustment and servo functions of the power supply hardware.

Configuration Services (CFG_Services) – has responsibility for identifying the hardware modules, reading and writing to the board calibration eeproms, shutter control, and provides the programmable sequencer for detector readout. This module is a Wishbone bus master.

Analog Front End Control (AFE_Control) – directly controls the analog board hardware and acquires digital pixel data. Controls the setting of bias and clock voltages and the state of the clock and cds circuits.

Pixel Services module (PIX_Services) – provides formatting and local image buffering services for the detector pixel data stream.

Bus stub terminator module (Dummy_Module) – This module acts as a place holder for two unused bus addressing assignments (Slave 5 and 6). The spare assignments may be used in a future firmware releases to supply additional functionality to the Torrent DHE.

The bus architecture looks like this:

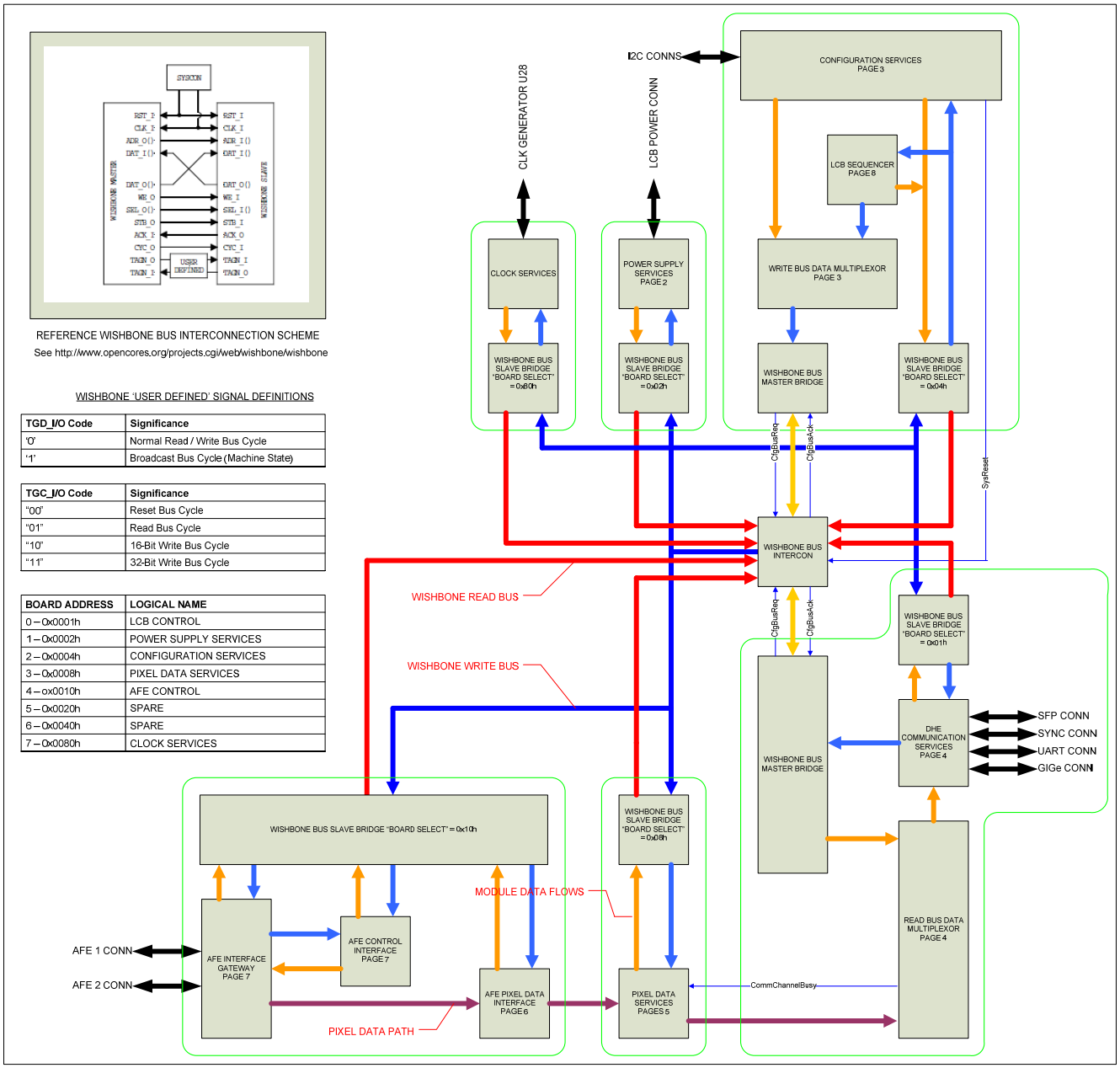

Figure 1 - Wishbone bus structure

The bus runs synchronously at a clock rate of 53.125MHz. This clock rate is also used extensively in the communication and control logic of the firmware. This clock is called SysClk and is generated by dividing the LCB master clock source (**LCB:Y1**) by a factor of 2. This clock is also fed to the clock generator device (**LCB:U28**) to generate other clocks at frequencies required by the acquisition, AFE interface, and SFP fiber interface.

Each module contains a vhdl source code block called [module_name]_RegisterControl. This block interfaces the module to the Wishbone bus and provides address decode and bus transaction processing allowing the module internal registers to be written to or read from by one of the bus masters. It is these registers that receive attribute values that are used to control the functions of the DHE. The two bus masters have the ability to write and read every attribute location available in the firmware design.

The Wishbone bus standard has been modified in this design to allow slow status information to be collected and disseminated when the bus is not involved in an actual read or write transaction. The status information is collected, mapped, and then distributed by the bus system interconnect logic – SYS_Interconnect – as a common 32-bit word to all modules. The individual module output status and the system status may be monitored by reading attributes in each module. The decoding of the individual bits can be found in an annex of this document. The system status allows each module to be aware of configuration and state of other modules in the firmware.

FPGA Configuration

The Virtex-5 device requires a configuration data stream at power on to establish functionality. This boot process takes approximately 50ms and is controlled directly by a boot loader built into the FPGA. The data stream comes from a Xilinx specific eeprom store (**LCB:U43**) that is pre-programmed with the image of the configuration data stream. The eeprom store contains two complete images that can be loaded independently according to the electrical state of the **LCB:AFE_SCL_SRC** signal. Currently we program the two images identically.

The future concept is to use the lower image (**LCB:AFE_SCL_SRC**=low) to configure the FPGA for use with the infrared acquisition cards. The **LCB:AFE_SCL_SRC** signal will be strapped low by a resistor on the appropriate AFE circuit board to automatically select the correct configuration. The eeprom store (and the FPGA itself) may be programmed using the JTAG interface available on **LCB:J3**.

Diagnostics

Select signals internal to the FPGA can be monitored to diagnose problems and to provide synchronization triggers. The diagnostic signals are available on **LCB:J4** as an 8-bit wide debug word. Control over which signals are present on the debug port is by programming the **DbgSigSlct** attribute to an appropriate value. The firmware signals available on this port are detailed in a separate annex to this document.

An independent trigger can be programmed to appear on the **LCB:TSM_PRESENT** hardware signal available on **LCB:J13**. This synchronization trigger is controlled by the **DbgTrigSlct** attribute value.

Additional diagnostic information is available from the two LED mounted on the **LCB:SYNC_IN** and **LCB:SYNC_OUT** J45 connectors. These indicators will briefly flash should the selected signal to monitor is set true. The selection of the signal to monitor is by programming a appropriate values into the **Led1_Slct** and **Led2_Slct** attributes.

Firmware versions

Each firmware module has it's own revision level which is available for inspection by reading the appropriate attribute value. At the system level of the firmware source code, a generic system firmware version value is also specified. This system firmware version value can also be read from an attribute location. This revision level information is sufficient to uniquely identify the source code modules that were used to synthesize and build the boot loader code resident in the eeprom store (**LCB:U43**). The system firmware version value is used by PAN software (collect) to identify the firmware code version loaded to the LCB to enable it to build a valid configuration file for the system.

There is also a date code that is embedded into the eeprom code store at the time of the firmware build. Use a JTAG tool (e.g. Xilinx Impact tool) to connect to the JTAG connector **LCB:J3**. Use the 'Get device signature/usercode" command to read back the FPGA static code identity. The usercode is written as a reverse 6-digit hex date plus a two digit build code e.g. a usecode value of 12062501 means the code was built on the 25th June 2012 and is the first build attempt of that day.

If that is not enough; The checksum values for the eeprom store image and the FPGA are available after build and by reading them from the devices on the JTAG chain. This information can be used to verify that the correct code is loaded to the LCB.

There are three sub levels of the firmware revision value that are used in the basic strategy in generating appropriate firmware revision numbers.

The major level version codes are used to describe the application code purpose (e.g. 1.xx indicates development code, 2.xx are CCD production code versions, 3.xx is IR camera production code, etc.). The range

of major revision levels is 0 to 99 so if you are independently generating code for the LCB please use a different major level code to identify your product and notify us at NOAO so that we can reserve that code level for you.

Semi-major code values (i.e. the first decimal, x.1x) generally change when a functional change is incorporated that require the system tools software (assimilate) to be used to extract new attribute values. This is generally because new functionality has been incorporated into the code (e.g. incorporation of a new image buffer scheme, etc.).

Minor revision levels (i.e. last digit, x.x1) are for bug fixes and/or enhancements without affecting functionality.

Developing firmware

The basic framework for development of the Torrent firmware product is the Xilinx ISE WebPACK software. This is a free of charge product that includes a project editor, a synthesizer, map and place processors, and eeprom and JTAG loader generators. It is sufficiently complete to do end to end development. The WebPACK software version used to generate Torrent firmware is version 10.1.03. The free package was chosen to allow 3rd parties to access and generate the same code products using the open source license agreement. There are other synthesizers and indeed Xilinx products that would generate more optimum loader code but would require licensing individual agreements.

All source code files are commented – some more than others – in an attempt to identify the processes and dependencies. The top level of each module is a schematic that identifies the major functional blocks and interconnects them. Some top layer schematics have additional layers of schematic capture depending on the complexity. Using the Xilinx tools, all levels of the hierarchy can be pushed down into.

Some code that is used frequently (i.e. Wishbone bus slave logic) is kept in a common area. Otherwise each new version of a code module requires a new directory to be created for it. A new or modified code module that is required to be merged into the project requires that a new system level firmware version be created. This is easily done in the Xilinx WebPACK suite by using the “Save Project As ..” command in the file menu and changing the system project name to match the new version number. Once this is done, remove the existing module that is to be replaced (if required) and use the “Add Source ..” command from the source window context menu to include the new code module directory contents. Each new system firmware version requires a new WishboneInterconnect (Intercon) source to be included with the updated system version number.

The source code directory tree used to generate the firmware is:

```
[ROOT]  / Xilinx /SystemBuilds/TorrentFpga_Ver222
                 / ModuleBuilds/AFE_Control_Ver221
                                /CFG_Services_Ver220
                                /CLK_Services_Ver221
                                /DummyModule_V220
                                /LCB_Control_Ver222
                                /PIX_Services_Ver221
                                /PSM_Services_Ver221
                 / Templates    /CommsDemuxPixBuffr_V106
                                /PixDataMuxFifo_V103
                                /SerialFPDPV5V5b
                                /SeqPatMemCore
                                /SeqProgMemCore
                                /SyncPortFifo_V100
                                /Uart_8
                                /UartFifo
                                /WishBoneIntercon_Ver222
                                /WishBoneMasterInterfaceV106
                                /WishBoneSlaveInterface_Ver207
                 /TestBenches   / ….
```

The [ROOT] directory for the NOAO code is “C:/Monsoon/Torrent”. A complete firmware source code package is available by contacting the author.

Building the code results in about 1200 warning messages, mainly from synthesis that result from (mainly) unused resources that are removed automatically from the design. Don’t worry about these – they are normal.

There are three main clock domains internal to the FPGA. The SysClk which is used for all communication logic, Wishbone bus transactions, power supply control, and the sequencer. SysClk runs at 53.125MHz. Acquisition processes are synchronized to the AFE interface and run on D_Clk which is a 79.6875 MHz clock sourced from the clock generator device. Two port memory buffer processes in the PIX_Services module operate at 159.375 MHz. All clocks are synchronous.

A system level constraints file is used to control the firmware build process. This file is kept in system source directory. The constraints file contains the FPGA ball designations for it’s connection to the external hardware, timing and critical placement directives. Experiment with care.

System Level Attributes

These few attributes operate on the system as a whole i.e. they perform their function on all installed firmware modules simultaneously.

The **SysCodeId** attribute is used to identify the overall (system) firmware revision level.

To access these attributes the read or write request must force all eight Board Select Bits to 1 and set the correct Board Register Address (0xFFFF for **SysCodeId** and **SysRebootCmd**, 0xFFFE for **SysResetCmd**). See the ICD document MNSN-AD-01-0005_ICD_6.1_v1.1 for an explanation of the write or read command format.

Attribute name **SysCodeId** **array size** 1

Function Returns the system level firmware revision code

Firmware module SYS **version** 2.22

Description Returns the top level (system level) build version as a decimal value with two decimal points.
Major level version codes are used to describe application levels (e.g. 1.xx indicates development code, 2.xx are CCD production code versions, 3.xx is IR camera production code, etc.).
Semi-major code changes (i.e. the first decimal) generally incorporate functional changes that require software to be used to extract new attribute values and/or incorporate new functionality (e.g. incorporation of a new image buffer scheme, etc.).
Minor revision levels are for bug fixes and/or enhancements without affecting functionality.

Usage Read only.

Address 0xFFFF

Calibration **Units** Version **Slope** 100.0 **Offset** 0.0

Limits **Maximum** 655.35 **Minimum** 0.0 **Default** 2.22

Associations

Attributes None

Hardware None

Notes Asserting this signal does not allow the DHE to power down gracefully so signals to any attached detector are undefined during the reboot. This attribute should be used with caution and only as a last resort. The action of this attribute is identical to pushing the reset button on the LCB hardware.

More information Decoding of this attribute is done by the module CmdDecodeV108.vhd in the //{Torrent root}/Xilinx/ModuleBuilds/LCB_Control_Ver220 directory.

Attribute name **SysRebootCmd** **array size** 1

Function Reboots (cold boot) the FPGA from the associated EEPROM store on the LCB

Firmware module LCB **version** 2.22

Description Writing a 16-bit value of 0xFFFF to this attribute with all board select bits true will perform a cold boot operation on the hardware.

Usage Write only.

Address 0xFFFF

Calibration **Units** N/A **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 65535.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes None

Hardware Signal **LCB_RESET** on schematic TRNT-EL-04-2002, page 1/B:7

Notes Asserting this signal does not allow the DHE to power down gracefully so signals to any attached detector are undefined during the reboot. This attribute should be used with caution and only as a last resort. The action of this attribute is identical to pushing the reset button on the LCB hardware.

More information Decoding of this attribute is done by the module CmdDecodeV108.vhd in the //{Torrent root}/Xilinx/ModuleBuilds/LCB_Control_Ver220 directory.

Attribute name
SysResetCmd **array size** 1

Function
Perform a DHE warm boot to reset all FSM and activity on all firmware modules

Firmware module
LCB **version** 2.22

Description
Writing a 16-bit value of 0xFFFE to this attribute with all board select bits true will perform a warm boot operation (reset) on the hardware.
Writing to this attribute is the equivalent of issuing a separate reset command to each firmware module.
The system level reset is carried out simultaneously on all modules.
The detector is disconnected from the hardware, the sequencer run flag is reset and the communication async flag is set awaiting a synchronization command from the PAN.

Usage
Write only.

Address
0xFFFE

Calibration
Units N/A **Slope** 1.0 **Offset** 0.0

Limits
Maximum 65534 **Minimum** 0.0 **Default** 0.0

Associations
Attributes None

Hardware None

Notes
Try not to use this command. It is intended to recover from a condition when the DHE and/or the PAN is confused. Better to use individual module reset commands to focus on the area that is confused rather than issue a general reset command. Most of the attribute values remain untouched.

More information
Decoding of this attribute is done by the module CmdDecodeV108.vhd in the //{Torrent root}/Xilinx/ModuleBuilds/LCB_Control_Ver220 directory.

Clock Services Module (CLK) Attributes

The Clock services firmware is a Wishbone slave module connected to the FPGA internal Wishbone bus. The attributes of this module control the clock sources that are used to synchronize the firmware logic and hardware functions of the DHE.

There are two primary clock sources. The first primary clock source is generated internally on the LCB circuit board by crystal oscillator Y1 on the LCB schematic document TRNT-EL-04-2002 Revision –B–. This oscillator produces a differential signal at 106.25 MHz. This clock source is normally used when the DHE is operating as a single controller or when the DHE is designated as master of a synchronized group of controllers. The second primary clock source is an externally generated signal that is used to synchronize multiple controllers working in a group. This source is input via a differential input on the LCB SYNC IN connector J9. It is normally operated at 53.125 MHz.

A clock conditioner / generator device, U28 shown on the same LCB schematic document, locks a voltage controlled oscillator to the primary clock in use and generates all of the major clock sources at various frequencies for use in the controller.

The attributes described in this section have controlling and configuring functions that allow for the generation of the major clock sources.

Attribute name **ClkResetCmd** array size 1

Function
Provides a local reset to the CLK firmware module

Firmware module CLK version 2.21

Description
Writing a value of 1.0 (true) to this attribute resets the internal functions of the clock control firmware.

This action sets the default conditions as follows:
Primary clock source is set as Y1 (i.e. internal). **SyncClkSelect** set to zero, **SyncInEqualization** and **SyncOutEqualization** set to zero, and sets **SlaveClkXferEn** false to disable slave clock detection and switching.

In addition the state machine and conditioning logic for the clock conditioner configure functions (ConfigureClockProc, SerialClockProc, ClockConfigTriggerProc) are reset.

Usage
Write only.

Address
0xFFFE

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
SyncClkSelect, **SyncInEqualization**, **SyncOutEqualization**, **SlaveClkXferEn**

Hardware
CLK_CTRL_CLK, CLK_CTRL_DATA, /CLK_CTRL_CS, CLK_CTRL_SYNC, CLK_CTRL_GOE, SNK_EQ0, SNK_EQ1, SRC_EQ0, SRC_EQ1.

Notes

More information

Attribute name **ClkCodeId** array size 1

Function
Returns the CLK Module firmware revision level value

Firmware module CLK version 2.21

Description
Reading this attribute provides the firmware revision level of this module as a major revision level with two decimal places.
Major level revision codes are used to describe application levels (e.g. 1.xx indicates development code, 2.xx are CCD production code versions, 3.xx is IR camera production code, etc.).
Semi-major code changes (i.e. the first decimal) generally incorporate functional changes that require software (assimilate tool) to be used to extract new attribute values and/or incorporate new functionality (e.g. incorporation of a new image buffer scheme, etc.).
Minor revision levels are for bug fixes and/or enhancements without affecting functionality.

Usage
Read only.

Address
0xFFFF

Calibration
Units Revision **Slope** 100.0 **Offset** 0.0

Limits
Maximum 655.35 **Minimum** 0.0 **Default** 0.0

Associations
Attributes None.

Hardware None.

Notes

More information

Attribute name **ClkModuleId** array size 1

Function
Returns the function code of the CLK module to confirm its presence.

Firmware module CLK version 2.21

Description
Reading this attribute enables any interrogating device to confirm the presence of this module at the given module select address. The constant assigned to the CLK identification attribute has the value 208.

Values between 100 and 199 represent MONSOON Orange hardware module identity codes.
Values between 200 and 299 represent MONSOON Torrent firmware module identity codes.

Usage
Read only.

Address
0xFFFE

Calibration
Units Ident **Slope** 1.0 **Offset** 0.0

Limits
Maximum 65535.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes None.

Hardware None.

Notes

More information

Attribute name **ClkModInStatus** array size 1

Function
Returns the System status word as seen by the module

Firmware module CLK version 2.21

Description
The system status word is defined by the interconnect system of the Wishbone bus that interconnects all firmware modules internal to the FPGA. This status word is broadcast to each module and is used to convey state information concerning the configuration and functional state of the controller.

Usage
Read only.

Address
0xFFFD

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 0xffffffff **Minimum** 0.0 **Default** 0.0

Associations
Attributes
LCBModOutStatus, PSMModOutStatus, CFGModOutStatus, PIXModOutStatus, AFEModOutStatus, ClkModOutStatus.

Hardware
See the Wiki page link given below.

Notes

More information
See http://www.noao.edu/wiki/index.php/Firmware_Topics - Wishbone_system_status_signal_assignment

Attribute name **ClkModOutStatus** **array size** 1

Function Provides local status information on the CLK module state

Firmware module CLK **version** 2.21

Description

Reading this attribute provides additional state information internal to the CLK module. In this firmware revision the only significant bit is the LSB (bit zero) which when true indicates that the clock generator device has achieved lock on the primary clock source. This indicates that the clock generator is performing normally. This is equivalent to reading the

Usage Read only.

Address 0xFFFC

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 0xffffffff **Minimum** 0.0 **Default** 0.0

Associations

Attributes None.

Hardware U28 **CLK_LOOP_LOCK** (LCB at TP9)

Notes

More information

LMK03000 data sheet.

Attribute name **ClkCfgRegs** **array size** 16

Function Provides an alternative clock generator configuration – Engineering use only

Firmware module CLK **version** 2.21

Description

These are shadow registers of a 16 x 24-bit array that is loaded to the clock conditioner device on the LCB (U28 - LMK03000). This device provides the major clock sources for all operations in hardware. For each cold boot the values used to program the device are taken from a small ROM store and are therefore constant. After boot these shadow attributes can be modified to provide an alternate configuration to the clock conditioner. Only 13 of the 16 attributes are used. After modifying the appropriate registers the **LoadClkCfg** attribute is set true to load the conditioner with the new values.

Usage Read / Write.

Address 0x0070 => 0x007F

Calibration **Units** Binary **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 4294967295 **Minimum** 0.0 **Default** See notes

Associations

Attributes **loadClkCfg**

Hardware U28 on Schematic TRNT-EL-04-2002 Page 1/D7.

Notes After setting the clock conditioner expect garbage on the optical link since the source clock for this (and other) communication links is generated by this device.

Default values are:
x"00000000", x"00000000", x"00000000", x"4800300F",x"0830040E", x"028D495D", x"0082000B", x"00000807", x"00030206", x"00030405", x"00030304", x"00030803", x"00000802", x"00030301", x"00030800", x"80000000"

More information LMK03000 data sheet.

Attribute name **LoadClkCfg** array size 1

Function
Trigger to initiate a load sequence to configure the clock conditioner U28

Firmware module CLK version 2.21

Description
Writing a value of 1 (true) to this register initiates the configuration of the clock conditioner device via a synchronous serial interface. The values for the configuration are sequentially taken from the **ClkCfgRegs** attributes, serialized and sent to the conditioner device on signals **CLK_CTRL_CLK, CLK_CTRL_DATA, /CLK_CTRL_CS, CLK_CTRL_SYNC**, and **CLK_CTRL_GOE**.

Reading this attribute returns the state of the clock conditioner lock indicator. A true returned value indicates correct configuration and operation of the clock conditioner device U28.

Usage
Write / read

Address
0x0015

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
ClkCfgRegs

Hardware
CLK_CTRL_CLK, CLK_CTRL_DATA, /CLK_CTRL_CS, CLK_CTRL_SYNC, and **CLK_CTRL_GOE**
When read - **CLK_LOOP_LOCK** (LCB at TP9)

Notes

More information
Decoding of this attribute is done by the module LMK03000_Control_V221.vhd in the //{Torrent root}/Xilinx/ModuleBuilds/CLK_Services_Ver221 directory.
LMK03000 data sheet.

Attribute name **SlaveClkMode** array size 1

Function
Reports the clock source from which the DHE is currently operating

Firmware module CLK version 2.21

Description
If the master clock source for the DHE is external (i.e. from the LCB_SYNC_IN port J9) then this attribute will indicate true status. This can only occur if the DHE has been designated as a slave DHE , the **SlaveClkXferEn** attribute has been set true, and the SYNC_IN clock source is present and within the appropriate frequency range.
If this bit is true then the slave DHE is synchronized to the master in the chain and all commands and operations will be carried out synchronously with the master to reduce mutual interference.

Usage Read only.

Address 0x0082

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 1.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **SlaveClkXferEn, DheIsSlave**

Hardware LCB J9 – **INSYNC_CLK, / INSYNC_CLK**

Notes
Currently the ability to switch clocks has been disabled in firmware pending further development.

More information

Attribute name **SlaveClkXferEn** **array size** 1

Function Enables automatic detection and transfer of the primary clock source

Firmware module CLK **version** 2.21

Description

Setting the attribute true enables the clock control logic to detect the presence of a valid external clock source on signals **INSYNC_CLK, / INSYNC_CLK** and, if the DHE has been configured as a slave, switch the primary clock source from the internal oscillator to the external clock source.

Usage Write / read.

Address 0x0081

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 1.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes **DheIsSlave**

Hardware J9 – **INSYNC_CLK, / INSYNC_CLK**

Notes Currently the ability to switch clocks has been disabled in firmware pending further development.

More information

Attribute name **SyncClkSelect** array size 1

Function
Selects the source for the master **OUTSYNC_CLK** signals

Firmware module CLK version 2.21

Description
When the DHE is operating as a master and controlling slave DHEs, this attribute selects between an the FPGA internally generated master clock signal or a clock source generated directly by the clock conditioner device. This choice is for engineering purposes only and allow the sync port data signals to either lead or lag the sync clock signal.

Usage
Write / read.

Address
0x0083

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 15.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes

Hardware
U55 – **SYNC_CLK_SEL0, SYNC_CLK_SEL1, SYNC_CLK_EN0, SYNC_CLK_EN1**

Notes

More information
Torrent wiki page: http://www.noao.edu/wiki/index.php/Firmware_Topics - Clock_Sources_for_Master_sync_clock

Attribute name **SyncInEqualization** array size 1

Function
Selects the degree of de-emphasis applied to the SYNC input signals

Firmware module CLK version 2.21

Description
Allows for tuning the differential receivers used to receive INSYNC signals through J9 for different cable lengths. Applies de-emphasis to higher frequency components of the input signals to compensate fro phase delays in the cable. Only used when the DHE is configured as a slave.

Usage
Write / Read.

Address
0x0085

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 3.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **SyncOutEqualization**

Hardware U76, U77, U81 **SNK_EQ0, SNK_EQ1**

Notes

More information
See data sheet for DS25BR110 device at
http://www.ti.com/product/ds25br110

Attribute name **SyncOutEqualization** **array size** 1

Function Selects the degree of pre-emphasis applied to the SYNC output signals

Firmware module CLK **version** 2.21

Description

Provides pre-emphasis to the OUTSYNC signals of J8. This provision allows tuning for different cable lengths and/or impedances so that the link performs optimally. Only used when the DHE is configured as a master.

Usage Write / Read.

Address 0x0084

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 3.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes **SyncInEqualization**

Hardware U75, U78, U79 – **SRC_EQ0, SRC_EQ1**

Notes

More information

See data sheet for DS25BR120 device http://www.ti.com/product/ds25br120

Local Control Board Module (LCB) Attributes

The Local Control Board firmware is a Wishbone master / slave module connected to the FPGA internal Wishbone bus. The attributes of this module control the system reset, communication, command parsing, synchronization between multiple DHEs, and the firmware debug port.

The WishBone Bus module address for the PIX Services module is 0x01.

Attribute name **LcbResetCmd** array size 1

Function
Provides a local reset to the LCB firmware module

Firmware module LCB version 2.22

Description
Writing a value of 1.0 (true) to this attribute resets the internal functions of the local control board firmware.

This action sets the default conditions as follows:
FpdpPortDisable = 0, **SyncPortDisable** = 1, **UartPortDisable** = 0, **GIGePortDisable** = 0, **FpdpCmdCopyEn** = 0, **SyncCmdCopyEn** = 0, **UartCmdCopyEn** = 1, **GIGeCmdCopyEn** = 0, **WatchDogPeriod** = 10, **WatchDogEnable** = 1, **FpdpLoopBackMode** = 0, **PixSimEnable** = 0, **PixSimDest** = 1, **PixSimRows** = 1024, **PixSimCols** = 1024, **PixSimBurstLen** = 0, **DbgSigSlct** = 0, **DbgTrigSlct** = 0.

Usage
Write only.

Address
0xFFFE

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 1.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes
FpdpPortDisable, **SyncPortDisable**, **UartPortDisable**, **GIGePortDisable**, **FpdpCmdCopyEn**, **SyncCmdCopyEn**, **UartCmdCopyEn**, **GIGeCmdCopyEn**, **WatchDogPeriod**, **WatchDogEnable**, **FpdpLoopBackMode**, **PixSimEnable**, **PixSimDest**, **PixSimRows**, **PixSimCols**, **PixSimBurstLen**, **DbgSigSlct**, **DbgTrigSl**

Hardware
LCB:/WATCHDOG, LCB:U70, LCB:/SFP_TX_EN, LCB:UART_PS, LCB:U54, LCB:CFG_DATA(7:0), LCB:TSM_PRESENT, LCB:/TSM_PRESENT.

Notes
After a reset event, the communication channels are waiting for an ASYNC-CMD command, issued from the PAN to synchronize communication. In this state, the only reply to any command is an ASYNC-RPLY. The communication state of the DHE is changed to active (i.e. async state is exited) by the first successful reception of the ASYN-CMD word on any communication channel. When initiating communication on any channel, regardless of the DHE state, the first command must be an ASYC-CMD.

More information
For communication protocols see the MONSOON ICD 6.1 document at http://www.noao.edu/ets/new_monsoon/technical/general/MNSN-AD-01-0005_ICD_6.1_v1.1.pdf

Attribute name **LcbCodeId** array size 1

Function
Returns the LCB Module firmware revision level value

Firmware module LCB version 2.22

Description
Reading this attribute provides the firmware revision level of this module as a major revision level with two decimal places.
Major level revision codes are used to describe application levels (e.g. 1.xx indicates development code, 2.xx are CCD production code versions, 3.xx is IR camera production code, etc.).
Semi-major code changes (i.e. the first decimal) generally incorporate functional changes that require software (assimilate tool) to be used to extract new attribute values and/or incorporate new functionality (e.g. incorporation of a new image buffer scheme, etc.).
Minor revision levels are for bug fixes and/or enhancements without affecting functionality.

Usage
Read only.

Address
0xFFFF

Calibration
Units Revision **Slope** 100.0 **Offset** 0.0

Limits
Maximum 655.35 **Minimum** 0.0 **Default** 2.22

Associations
Attributes
None.

Hardware
None.

Notes

More information

Attribute name **LcbModuleId** array size 1

Function
Returns the function code of the LCB module to confirm its presence.

Firmware module LCB version 2.22

Description
Reading this attribute enables any interrogating device to confirm the presence of this module at the given module select address. The constant assigned to the LCB identification attribute has the value 201.

Values between 100 and 199 represent MONSOON Orange hardware module identity codes.
Values between 200 and 299 represent MONSOON Torrent firmware module identity codes.

Usage
Read only.

Address
0xFFFE

Calibration
Units Ident **Slope** 1.0 **Offset** 0.0

Limits
Maximum 65535.0 **Minimum** 0.0 **Default** 201.0

Associations
Attributes
None.

Hardware
None.

Notes

More information

Attribute name **LcbModInStatus** **array size** 1

Function Returns the System status word as seen by the module

Firmware module LCB **version** 2.22

Description

The system status word is defined by the interconnect system of the Wishbone bus that interconnects all firmware modules internal to the FPGA. This status word is broadcast to each module and is used to convey state information concerning the configuration and functional state of the controller.

Usage Read only.

Address 0xFFFD

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 0xffffffff **Minimum** 0.0 **Default** 0.0

Associations

Attributes **LCBModOutStatus, PSMModOutStatus, CFGModOutStatus, PIXModOutStatus, AFEModOutStatus, ClkModOutStatus**.

Hardware See the Wiki page link given below.

Notes

More information

See http://www.noao.edu/wiki/index.php/Firmware_Topics - Wishbone_system_status_signal_assignment

Attribute name **LcbModOutStatus** array size 1

Function
Provides local status information on the LCB module state

Firmware module LCB version 2.22

Description
Reading this attribute provides additional state information internal to the LCB module. In this firmware revision the bit significance is:

Bit	Significance	Bit	Significance
0	LCB is in Async State	8	Comms device(s) is(are) busy
9	SFPD loss of carrier signal	10	SFPD transmitter fault
19:16	WB master bus error count	23:20	WB master grant counter
27:24	WB master bus timeout cnt	31:28	WB master event counter

Usage
Read only.

Address
0xFFFC

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 0xffffffff **Minimum** 0.0 **Default** 0.0

Associations
Attributes None.

Hardware **LCB:SFP_TXFAULT**

Notes

More information
For WB master status information see the source file WbMasterInterfaceV106.vhd in the //{Torrent root}/Xilinx/Templates/WbMasterInterfaceV106 directory.

Attribute name **FpdpPortDisable** **array size** 1

Function Disables the Serial Front Panel Data Port (SFPDP) communication channel

Firmware module LCB **version** 2.22

Description

Setting this attribute true disables the SFPDP communication channel (The 'Systran' comms port). This switches off the optical transceiver and clears any buffer data from this port.

Usage Read / Write.

Address 0x0010

Calibration **Units** Binary **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 1.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes **FpdpCmdCopyEn, FpdpLoopBackMode**

Hardware **LCB:/SFP_TX_EN, LCB:SFP_LOS**

Notes

More information

Attribute name **FpdpCmdCopyEn** array size 1

Function
Enables the echo feature for the SFPDP communication port

Firmware module LCB version 2.22

Description
If set true, all commands to the DHE and all messages (replies) from the DHE are echoed onto the SFPDP (Systran) transmitter. This allows you to sample the command and response flow from the DHE. Do not set this attribute true if the SFPDP is the principle command port from the PAN.

Usage
Read / Write.

Address
0x0000

Calibration
Units Binary **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **FpdpPortDisable, FpdpLoopBackMode**

Hardware None.

Notes

More information

Attribute name **FpdpLoopBackMode** **array size** 1

Function Used to test the BER of the SFPDP communication port

Firmware module LCB **version** 2.22

Description

Setting this attribute allows two classes of loopback to be performed in order to test the communications link. The value significance for this attribute is:

Value Function.
0 No loopback – normal communications
1 Parallel loopback – back end of sfpdp tx and rx logic are tied together
2 Serial loopback – Front end of sfpdp tx and rx logic are tied together
All other values are illegal.

Usage Read / Write.

Address 0x0020

Calibration **Units** Binary **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 1.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes

Hardware

.

Notes To use this feature the PAN SFPDP (Systran) interface must set the PIO1 and DIR signals true and signal PIO2 false. Under this condition the loopback value is sent to the transceiver module.

More information

Attribute name **SyncPortDisable** array size 1

Function Disables the Synchronization communications Port (SYNC)

Firmware module LCB version 2.22

Description

Setting this attribute true disables the SYNC-IN and SYNC_OUT communication channels. These ports are used to daisy chain multiple DHE used on an instrument where synchronous operation is required to reduce noise caused by interference between them. The SYNC ports transmit and receive a global clock, a global synchronization strobe, and a bidirectional serial data stream. The serial data streams are used to measure the signal delay for the clock and synchronization strobes so that they may be compensated.

Usage Read / Write.

Address 0x0011

Calibration **Units** Binary **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 1.0 **Minimum** 0.0 **Default** 1.0

Associations

Attributes **SyncCmdCopyEn.**

Hardware None.

Notes The SYNC-IN and SYNC-OUT ports are disabled in this release of firmware pending further development work.

More information

Attribute name **SyncCmdCopyEn** **array size** 1

Function Enables the echo feature for the SYNC-OUT communication port

Firmware module LCB **version** 2.22

Description

If set true, all commands to the DHE and all messages (replies) from the DHE are echoed onto the SYNC-OUT transmitter. This feature will be used in the future to allow multiple DHEs to be controlled from one PAN.

Usage Read / Write.

Address 0x0001

Calibration **Units** Binary **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 1.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes **SyncPortDisable.**

Hardware None.

Notes The SYNC-IN and SYNC-OUT ports are disabled in this release of firmware pending further development work.

More information

Attribute name **UartPortDisable** **array size** 1

Function Disables the UART Port (RS232)

Firmware module LCB **version** 2.22

Description

Setting this attribute true disables the UART port that is available on connector **LCB:J12** . This port is principally used for debugging purposes when the main communication channel (SFPDP) is down. The UART port accepts simple commands and responds with ascii reply values.

Usage Read / Write.

Address 0x0012

Calibration **Units** Binary **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 1.0 **Minimum** 0.0 **Default** 1.0

Associations

Attributes **UartCmdCopyEn.**

Hardware **LCB:UART_PS, LCB:U54.**

Notes The UART port is programmed by firmware for 9600 Baud, 1 stop bit, 8 data bits, and no parity.

More information

For the command structure used on this port see
http://www.noao.edu/wiki/index.php/Firmware_Topics#RS232_Communication_Channel_Command_Codes

Attribute name **UartCmdCopyEn** **array size** 1

Function Enables the echo feature for the UART communication port

Firmware module LCB **version** 2.22

Description

If set true, all commands to the DHE and all messages (replies) from the DHE are echoed onto the UART transmitter. This feature is enabled by default.

Usage Read / Write.

Address 0x0002

Calibration **Units** Binary **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 1.0 **Minimum** 0.0 **Default** 1.0

Associations

Attributes **UartPortDisable.**

Hardware None.

Notes

More information

Attribute name **GIGePortDisable** **array size** 1

Function Disables the GIGe Port (Ethernet)

Firmware module LCB **version** 2.22

Description

Setting this attribute true disables the GIGe port that is available on the RJ45 connector mounted to the side of the fan casing. The GIGe port has two communication channels; a bidirectional command / message channel and a pixel data transmitter. The command / message channel accepts simple ascii commands and responds with simple ascii message string values (exactly the same as the UART port).

Usage Read / Write.

Address 0x0013

Calibration **Units** Binary **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 1.0 **Minimum** 0.0 **Default** 1.0

Associations

Attributes **GIGeCmdCopyEn.**

Hardware **LCB:J7**

Notes

More information

For the command structure used on this port see http://www.noao.edu/wiki/index.php/Firmware_Topics#RS232_Communication_Channel_Command_Codes
See the GIGe vendor site for client side details at http://www.pleora.com/our-products/iport-video-transmitters/iport-ntx-mini

Attribute name **GIGeCmdCopyEn** **array size** 1

Function Enables the echo feature for the GIGe communication port

Firmware module LCB **version** 2.22

Description

If set true, all commands to the DHE and all messages (replies) from the DHE are echoed onto the GIGe command / message channel. This feature is enabled by default.

Usage Read / Write.

Address 0x0003

Calibration **Units** Binary **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 1.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes **GIGePortDisable.**

Hardware None.

Notes

More information

Attribute name **GIGeDataWidthSlct** **array size** 1

Function
Selects which 16-bit pixel data product is transmitted to the PAN

Firmware module LCB **version** 2.22

Description
The GIGe interface is only capable of transporting 16-bit pixel values. When the pixel width is selected as 18-bits (using attributes **SCDataPrecision** or **QLDataPrecision**) the **GIGeDataWidthSlct** attribute selects the 16-bit value sent to the PAN using the GIGe pixel data communication channel. The value significance is:

Value	Selection of pixel data bus product
0	Pixel data (15:0)
1	Pixel data (16:1)
2	Pixel data (17:2)
3	Illegal value – pixel data value clamped to 0x4242

Usage Read / Write.

Address 0x0030

Calibration **Units** Value **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 3.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes None.

Hardware None.

Notes

More information

Attribute name **PixSimEnable** array size 1

Function
Enables the generation of synthetic pixel data for communication channel testing

Firmware module LCB version 2.22

Description
There are two synthetic pixel generators incorporated in the firmware; one in the LCB module and one in the AFE module. This generator is mainly orientated at testing the pixel data path from the DHE to the PAN. Setting this attribute true enables a pixel stream to be generated according to the associated attributes that is sent to the destination communication channel as a 32-bit value. The upper 16-bits express the row number and the lower 16-bits show the column number. The generation of the pixel data stream is initiated in the normal manner i.e. after the reception of a START EXPOSURE command. The start vector is not important. Be sure to disable any other pixel data generation before using this function.

Usage
Read / Write.

Address
0x0100

Calibration
Units Binary **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
PixSimDest, PixSimBurstLen, PixSimRows, PixSimCols.

Hardware
None.

Notes

More information
For START EXPOSURE command details see the MONSOON ICD 6.1 document at
http://www.noao.edu/ets/new_monsoon/technical/general/MNSN-AD-01-0005_ICD_6.1_v1.1.pdf

Attribute name **PixSimDest** array size 1

Function
Sets the destination communication port for synthetic pixel data

Firmware module LCB version 2.22

Description
This attribute allows you to send the synthetic pixel data stream to any of the available communication channel ports. The bit significance for this attribute is:

Bit	Destination port
0	SFPDP (Systran) communication port
1	SYNC-OUT communication port
2	UART communication port
3	GIGe pixel stream communications port

Note that a value of 0 indicates No port i.e. bit bucket

Usage
Read / Write.

Address
0x0101

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 15.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **PixSimEnable, PixSimBurstLen, PixSimRows, PixSimCols.**

Hardware .

Notes

More information

Attribute name **PixSimBurstLen** array size 1

Function
Selects the pixel data stream burst length to emulate different video channel depths

Firmware module LCB version 2.22

Description
The CCD variant of the Torrent hardware can acquire data from 16 video channels. The IR variant can acquire data from 32 video channels.

When this attribute is set false, the generator produces bursts of sixteen pixels interspersed with delays of approx. 2us to emulate a 500KPixel/channel/sec data stream which equals 8 MPixel data rate. This approximates the data rate from a maximum Torrent CCD variant.

When this attribute is set true, the generator produces bursts of 32 pixels interspersed by approx. 1us to emulate a 1 MPix/channel/sec data stream which equals 32 MPixel data rate. This approximates the maximum data rate achievable by an IR Torrent variant.

Usage Read / Write.

Address 0x0104

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 1.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes **PixSimEnable, PixSimDest, PixSimRows, PixSimCols.**

Hardware .

Notes

More information

Attribute name **PixSimRows** array size 1

Function
Sets the number of rows to simulate in the synthetic pixel data stream

Firmware module LCB version 2.22

Description
Set this attribute to the required row value to emulate a particular detector topology.

The resulting pixel data stream values will contain the row number in the high order 16-bits of the 32-bit pixel data value.

Usage
Read / Write.

Address
0x0103

Calibration
Units Rows **Slope** 1.0 **Offset** 0.0

Limits
Maximum 65535.0 **Minimum** 0.0 **Default** 1024.0

Associations
Attributes **PixSimEnable, PixSimBurstLen, PixSimDest, PixSimCols.**

Hardware .

Notes

More information

Attribute name **PixSimCols** array size 1

Function
Sets the number of columns to simulate in the synthetic pixel data stream

Firmware module LCB version 2.22

Description
Set this attribute to the required column value to emulate a particular detector topology.

The resulting pixel data stream values will contain the column number in the low order 16-bits of the 32-bit pixel data value.

Usage
Read / Write.

Address
0x0102

Calibration
Units Cols **Slope** 1.0 **Offset** 0.0

Limits
Maximum 65535.0 **Minimum** 0.0 **Default** 1024.0

Associations
Attributes **PixSimEnable, PixSimBurstLen, PixSimRows, PixSimDest.**

Hardware .

Notes

More information

Attribute name **WatchDogEnable** array size 1

Function
Enable the firmware / clock source hardware watchdog function

Firmware module LCB version 2.22

Description
The watchdog is used to detect when the system clock fails. This should never occur when the DHE is configured as a master, however, when the DHE is setup as a slave the system clock is supplied by from the DHE master via cable. If the connection to the slave fails the watchdog system will trigger. This action will shutdown the detector (i.e. disconnect the detector) and re-boot the DHE in an attempt to protect the detector and recover functionality.

This attribute must be set to allow the detector to be connected to the bias and clock voltages.

Usage
Read / Write.

Address
0x0021

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 1.0

Associations
Attributes
WatchDogPeriod.

Hardware
LCB:/WATCHDOG, LCB:U70, LCB:/WATCHDOG_FAIL, LCB:WDREBOOT, LCB:PROGRAM, LCB:/PROG_B

Notes
Note that this attribute is set true by default. Disabling the watchdog function will result in an apparent clock failure which will reboot the DHE. Therefore this attribute should not normally be used.

More information

Attribute name **WatchDogPeriod** array size 1

Function
Set the firmware / clock source hardware watchdog refresh rate

Firmware module LCB version 2.22

Description
The watchdog is refreshed by a programmable counter running from the system clock source. This attribute sets the divider ratio and therefore the period between refresh pulses that are sent to the watchdog retriggerable monostable. The hardware monostable device has a time constant of approx. 50us. The refresh period should be shorter that this value to assure the watchdog system does not trigger.

Usage
Read / Write.

Address
0x0022

Calibration
Units Microsec. **Slope** 1.0 **Offset** 0.0

Limits
Maximum 255.0 **Minimum** 0.0 **Default** 10.0

Associations
Attributes **WatchDogEnable.**

Hardware **LCB:/WATCHDOG, LCB:U70, LCB:/WATCHDOG_FAIL, LCB:WDREBOOT, LCB:PROGRAM, LCB:/PROG_B**

Notes
Note that this attribute is set to 10us period by default. Changing the watchdog refresh period to greater than approx. 50us will result in an apparent clock failure which will reboot the DHE. Therefore this attribute should not normally be adjusted.

This attribute is depreciated and will be removed from future firmware releases.

More information

Attribute name **Led1_Slct** array size 1

Function
Select the function to indicate on the rear panel LED 1 display.

Firmware module LCB version 2.22

Description
There are two LED indicators built into the SYNC_IN and SYNC_OUT RJ45 connectors mounted to the rear panel of the controller. LED 1 is the lower LED of J8, the SYNC-OUT port. The value set to this attribute controls the function that is indicated by this LED. The bit significance of this attribute is:

Bit	Function	Bit	Function
0	LCB WB Master cycle request	1	CFG WB Master cycle request
2	LCB WB Slave error return	3	PSM WB Slave error return
4	CFG WB Slave error return	5	PIX WB Slave error return
6	AFE WB Slave error return	7	Bus reset active

These signals correspond to the operation of the WishBone bus system (WB) within the FPGA.

Usage
Read / Write.

Address
0x0040

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 255.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes

Hardware

Notes
More than one bit can be selected simultaneously to provide multiple indications of activity.

More information

Attribute name **Led2_Slct** array size 1

Function
Select the function to indicate on the rear panel LED 2 display.

Firmware module LCB version 2.22

Description
There are two LED indicators built into the SYNC_IN and SYNC_OUT RJ45 connectors mounted to the rear panel of the controller. LED 2 is the lower LED of J9, the SYNC-IN port. The value set to this attribute controls the function that is indicated by this LED. The bit significance of this attribute is:

Bit	Function	Bit	Function
0	**/MCLK_SEL_N**	1	**VFAN_PWR_EN**
2	**VANA_PWR_EN**	3	**VCB_PWR_EN**
4	**VHV_POLARITY**	5	**VCC_SYNC_OUT**
6	**SRC_SYNC_OUT**	7	**SNK_SYNK_OUT**

These signals correspond to hardware signals controlled by the FPGA

Usage Read / Write.

Address 0x0041

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 255.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes

Hardware

/MCLK_SEL_N, VFAN_PWR_EN, VANA_PWR_EN, VCB_PWR_EN, VHV_POLARITY, VCC_SYNC_OUT, SRC_SYNC_OUT, SNK_SYNK_OUT.

Notes
More than one bit can be selected simultaneously to provide multiple indications of activity.

More information

Attribute name **DbgSigSlct** array size 1

Function
Selects which module provides signals to the firmware debug port

Firmware module LCB version 2.22

Description
Connector **LCB:J4** is used to breakout groups of internal FPGA signals to allow diagnostics. There are eight separate signals available on the connector. This attribute selects which module has control of the signals on this connector. The value significance is:

Value	Module Debug sigs	Value	Module Debug sigs
0	Debug signals off	1	LCB Control Module signals
2	PSM Services signals	3	CFG Services Module signals
4	PIX Services signals	5	AFE Control Module signals
6	Not used – Future AFE2	7	Not used – Spare
8	CLK Services Module signals	9	System WB Bus signal group
10	Auxiliary signal group.		

Usage
Read / Write.

Address
0x0042

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 10.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes

Hardware
LCB:J4, LCB:CFGDATA(7:0).

Notes

More information
For detailed explanation of the signals available in each group see http://www.noao.edu/wiki/index.php/Firmware_Topics#DbgSigSlct_attribute_values

Attribute name **DbgTrigSlct** array size 1

Function
Select the signal for output to LCB:J13 for use as a pattern trigger

Firmware module LCB version 2.22

Description
The connector **LCB:J13** is normally assigned to the TSM present switch mounted on the controller chassis. When involved in debugging or development is it often a convenience to have a separate trigger available to trigger an oscilloscope or logic analyzer attached to the debug signal port. By setting this attribute to a non-zero value the connector is converted into a trigger output port. The TSM_PRESENT_P signal (**LCB:J13:1**) carries the trigger signal.
The attribute is divided into two fields; the module select field (bits 6:3) which have the same coding as the **DbgSigSlct** attribute and bits (2:0) which select the individual signal from that group.

Usage
Read / Write.

Address
0x0043

Calibration Units Boolean Slope 1.0 Offset 0.0

Limits Maximum 127.0 Minimum 0.0 Default 0.0

Associations
Attributes

Hardware
LCB:TSM_PRESENT, LCB:U85, LCB:J13:1

Notes
The TSM-PRESENT signals are emulated internally when this attribute is set to a non-zero value. This means that the safeguards concerning the TSM removal while the AFE is powered up will be bypassed.

More information
For detailed explanation of the signals available in each group see http://www.noao.edu/wiki/index.php/Firmware_Topics#DbgSigSlct_attribute_values

Attribute name **StartExpVctr** array size 1

Function
Indicates the most recent start vector issued with the START EXPOSURE command.

Firmware module LCB version 2.22

Description
Each START EXPOSURE command issued by the PAN has a start vector associated with it. This start vector normally determines the jump vector that the DHE sequencer uses to initiate some action or function. This attribute displays the last start vector received by the DHE. It is mainly used for debugging purposes.

Usage
Read only.

Address
0x0023

Calibration
Units Value **Slope** 1.0 **Offset** 0.0

Limits
Maximum 255.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes

Hardware

Notes

More information

Power Supply Services Module (PSM) Attributes

The power supply firmware module provides control and monitoring services that define the performance of the power supply hardware system of the Torrent DHE. This firmware module also provides power supervision and power sequencing to allow safe operation of the detector and other controller hardware. The Power Supply Services firmware is a Wishbone slave module connected to the FPGA internal Wishbone bus. It has a Wishbone module address value of 0x02.

Attribute name
PsmResetCmd **array size** 1

Function
Provides a local reset to the PSM firmware module

Firmware module
PSM **version** 2.21

Description
Writing a value of 1.0 (true) to this attribute resets the internal functions of the power supply services control firmware.
This action sets the default conditions as follows:
PowerSyncEnable = 1, **HtrPowerEnable** = 0, **VFanPowerEnable** = 1, **VanaPowerEnable** = 1, **VcbPowerEnable** = 1, **VbbPowerEnable** = 0, **MemPowerEnable** = 1, **HtrServoPauseEnable** = 1, **MezPwrEnbleReg** = 0, **VfanTempSetPoint** = 41.0, **Vana-SetPoint** = -10.5, **Vana+SetPoint** =10.5, **Vcb-SetPoint** = -18.0, **Vcb+SetPoint** = 18.0, **Vana-ServoEnable** = 1, **Vana+ServoEnable** = 1, **Vcb-ServoEnable** = 1, **Vcb+ServoEnable** = 1.

Usage
Write only.

Address
0xFFFE

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
TempScanEnable, TempScanPeriod, ShutterEnable, ShutterOpenCmd, PreflashEnable, PreflashOnCmd, ShutterForceStatus, SeqEnable, DheIsSlave, PauseExposure, IntegrationTime.

Hardware

Notes

More information

Attribute name
PsmCodeId **array size** 1

Function
Returns the PSM Module firmware revision level value

Firmware module
PSM **version** 2.21

Description
Reading this attribute provides the firmware revision level of this module as a major revision level with two decimal places.
Major level revision codes are used to describe application levels (e.g. 1.xx indicates development code, 2.xx are CCD production code versions, 3.xx is IR camera production code, etc.).
Semi-major code changes (i.e. the first decimal) generally incorporate functional changes that require software (assimilate tool) to be used to extract new attribute values and/or incorporate new functionality (e.g. incorporation of a new image buffer scheme, etc.).
Minor revision levels are for bug fixes and/or enhancements without affecting functionality.

Usage
Read only.

Address
0xFFFF

Calibration
Units Revision **Slope** 100.0 **Offset** 0.0

Limits
Maximum 655.35 **Minimum** 0.0 **Default** 2.21

Associations
Attributes None.

Hardware None.

Notes

More information

Attribute name
PsmModuleId **array size** 1

Function
Returns the function code of the PSM module to confirm its presence.

Firmware module
PSM **version** 2.21

Description
Reading this attribute enables any interrogating device to confirm the presence of this module at the given module select address. The constant assigned to the PSM identification attribute has the value 202.

Values between 100 and 199 represent MONSOON Orange hardware module identity codes.
Values between 200 and 299 represent MONSOON Torrent firmware module identity codes.

Usage
Read only.

Address
0xFFFE

Calibration
Units Ident **Slope** 1.0 **Offset** 0.0

Limits
Maximum 65535.0 **Minimum** 0.0 **Default** 202.0

Associations
Attributes None.

Hardware None.

Notes

More information

Attribute name **PsmModInStatus** **array size** 1

Function Returns the System status word as seen by the module

Firmware module PSM **version** 2.21

Description The system status word is defined by the interconnect system of the Wishbone bus that interconnects all firmware modules internal to the FPGA. This status word is broadcast to each module and is used to convey state information concerning the configuration and functional state of the controller.

Usage Read only.

Address 0xFFFD

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 0xffffffff **Minimum** 0.0 **Default** 0.0

Associations

Attributes **LCBModOutStatus, PSMModOutStatus, CFGModOutStatus, PIXModOutStatus, AFEModOutStatus, ClkModOutStatus**.

Hardware See the Wiki page link given below.

Notes

More information See http://www.noao.edu/wiki/index.php/Firmware_Topics - Wishbone_system_status_signal_assignment

Attribute name
PsmModOutStatus **array size** 1

Function
Provides local status information on the PSM module state

Firmware module
PSM **version** 2.21

Description
Reading this attribute provides additional state information internal to the PSM module. In this firmware revision the bit significance of this attribute is:

Bit	Significance	Bit	Significance
0	VfanTempSensorSlct(0)	1	VFanTempSensorSlct_reg(1)
2	VfanTempSensorSlct(2)	3	ShutDownQuick indicator bit
4	TsmPresent indicator bit		

Usage
Read only.

Address
0xFFFC

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 0xffffffff **Minimum** 0.0 **Default** 0.0

Associations
Attributes

Hardware
None.

Notes
VfanTempSensorSlct codes:

Value	Sensor selected	Value	Sensor selected
0	FPGA internal (default)	1	LCB temperature sensor 1
2	LCB temperature sensor 2	3	AFE1 temperature sensor 1
4	AFE2 temperature sensor 2	5	AFE2 temperature sensor 1
6	AFE2 temperature sensor 2		
7	VfanTemperature attribute write value (servo testing)		

More information
See the module PSM_RegisterControl_Ver221.vhd in the //{Torrent root}/Xilinx/ModuleBuilds/PSM_Services_Ver221 directory.

Attribute name
PwrStatOverride **array size** 1

Function
Override for power status allowing AFE operation if power status is bad

Firmware module
PSM **version** 2.21

Description
Set this attribute true to override the power protection scheme in the firmware. When set the AFE interface is maintained active even though there may be a power fault status indicated and / or power removed from the AFE board. It allows you to diagnose problems with the LCB_MEZ or AFE hardware in-situ. Do not set this bit for operational use. It directly sets the **IFC_LOCEN** hardware bit on the LCB.

Usage
Read / Write.

Address
0x020D

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **MezPwrEnbleReg**.

Hardware **IFC_LOCEN.**

Notes
The AFE interface is normally only enabled when power supply VANA+ is present on the AFE board. If the LCB_MEZ board detects a fault in any AFE power supply it will disable all power to that AFE and shut down the interface by setting **IFC_LOCEN** false in an attempt to minimize damage to the detector and/or the controller. Using this bit (in the lab) allows you to trouble shoot problems associated with the AFE power supplies.

More information

Attribute name
PwrUpPrimarySupplies **array size** 1

Function
Sequence the enabled PSM analog power supplies into an operational state

Firmware module
PSM **version** 2.21

Description
When their respective enable attributes are set true, setting this attribute will sequence the primary analog power supplies on or off depending on the value set to it. This operation is required before enabling the supplies to the AFE boards. The supplies affected are: VANA+/-, VCB+/-, VHV+/-, Vbb. Note that sequencing on the supplies (i.e. setting this attribute true) when Vbb is enabled will set the Vbb setpoint attribute to a value of zero. This allows the AFE boards to be powered up and the detector voltages programmed before setting the Vbb voltage if required. Note that the **PwrUpAfeSupplies** must also be set true to enable the Vbb supply. When the **PwrUpPrimarySupplies** attribute is set false, the **PwrUpAfeSupplies** is also set false.
Only supplies with their individual enable bit set true will be powered up. Note that the VHV+/- supplies are enabled with the **VcbPowerEnable** attribute

Usage
Read / Write.

Address
0x020A

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
PwrUpAfeSupplies, VbbSetPoint, PowerStatusReg, VanaPowerEnable, VbbPowerEnable, VcbPowerEnable

Hardware
VANA_ENBL, VCB_ENBL, VBB_ENBL, VANA_SYNC, VCB_SYNC, VHV_SYNC

Notes
The power on sequence when this attribute is set true is:
Power on VANA+/- supplies, wait for 100ms, power on the VCB+/- and VHV+/-, wait for 50ms and set the PrimaryPwrIsOn flag status to true.
When set false the power down sequence is:
Power down Vbb, VCB+/-, and VHV+/-, wait for 100ms, power down the VANA+/- supplies
When the attribute is false, the synchronization pulses to the VHV, VCB, and VANA supplies is suppressed.

More information

Attribute name
PwrUpAfeSupplies **array size** 1

Function
Enable / Disable power to the AFE boards.

Firmware module
PSM **version** 2.21

Description
This attribute sequences the power to the AFE boards using the individual AFE power enable bits to the LCB-MEZ board. Setting this attribute true powers up the AFE boards. The power on sequence is:
Power on VANA+/-, wait 50ms, power on VCB+/-, wait 50ms, power on VHV+/-, wait 100ms, set the AfePwrIsOn status bit true.
The power off sequence is:
Set the AfePwrIsOn status false and power down VHV+/-, wait 50ms, power down VCB+/-, wait 50ms, power down VANA+/-.
Only the supplies that have their separate enable bits set true will be powered up.
The **PwrUpPrimarySupplies** attribute must be set before you can apply power to the AFE boards.

Usage
Read / Write.

Address
0x020B

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
PowerStatusReg.

Hardware
AFE1_PWR_EN_VANA, AFE2_PWR_EN_VANA, AFE1_PWR_EN_VCB, AFE2_PWR_EN_VCB, AFE1_PWR_EN_VHV, AFE2_PWR_EN_VHV, VBB_ENBL, /AFE1_PWR_FAIL_VANA, /AFE2_PWR_FAIL_VANA, /AFE1_PWR_FAIL_VCB, /AFE2_PWR_FAIL_VCB, /AFE_PWR_FAIL_VHV

Notes
The separate AFE power status bits (**/AFE1_PWR_FAIL_VANA, /AFE2_PWR_FAIL_VANA, /AFE1_PWR_FAIL_VCB, /AFE2_PWR_FAIL_VCB, /AFE_PWR_FAIL_VHV**) are only enabled after the AfePwrIsOn status bit is true. If a power supply fails during operation or fails to come up and be stable before the AfePwrIsOn status bit goes true, the AFE power is shut down to that AFE board.
You can use the **MezPwrEnbleReg** attribute to override the sequence and force the power onto the AFE boards while bypassing the protection built into the firmware.

More information

Attribute name **PowerDownDHE** array size 1

Function
Shut down the DHE power in an orderly manner

Firmware module PSM version 2.21

Description
This on the DHE hardware attribute emulates the function of the power button. . Setting this attribute true removes power from the detector and then sequences the various DHE power supplies through power down before finally shutting down the VCC supply to the LCB (which results in loosing communication to/from the DHE). This attribute should be used to remotely shut down the DHE. The only recovery method is to power on the DHE using either the power button on the chassis or the remote power control function available on connector PSM:J4.

Usage
Read / Write.

Address
0x0203

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **PowerStatusReg.**

Hardware **AFE1_PWR_EN_VANA, AFE2_PWR_EN_VANA, AFE1_PWR_EN_VCB, AFE2_PWR_EN_VCB, AFE1_PWR_EN_VHV, AFE2_PWR_EN_VHV, VBB_ENBL, PWR_KILL.**

Notes

More information

Attribute name
MezPwrEnbleReg **array size** 1

Function
Provide an AFE power supply enable override to allow diagnostics to be performed on the LCB-MEZ and AFE Boards.

Firmware module
PSM **version** 2.21

Description
This attribute should only be used in the lab – never in operational use. This attribute allows you to override the LCB_MEZ power enable bits to force power onto the AFE (assuming that the power supply and/or hardware protection circuits on the LCB_MEZ board will allow you to do so). The bit significance is:

Bit	Supply override	Bit	Supply override	Bit	Supply override
0	AFE1 VANA+/-	1	AFE1 VCB+/-	2	AFE1 VHV+/-
3	Not used	4	AFE2 VANA+/-	5	AFE2 VCB+/-
6	AFE2 VHV+/-	7	IFC_LOCEN (same as the **PwrStatOverride** attribute).		

Usage
Read / Write.

Address
0x0202

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 255.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **PwrStatOverride.**

Hardware **AFE1_PWR_EN_VANA, AFE2_PWR_EN_VANA, AFE1_PWR_EN_VCB, AFE2_PWR_EN_VCB, AFE1_PWR_EN_VHV, AFE2_PWR_EN_VHV, /AFE1_PWR_FAIL_VANA, /AFE2_PWR_FAIL_VANA, /AFE1_PWR_FAIL_VCB, /AFE2_PWR_FAIL_VCB, /AFE_PWR_FAIL_VHV**

Notes
The raw (but inverted i.e. true status) power fail status bit information is available in bits 15:8 of the read value. Note that there is only one **/AFE_PWR_FAIL_VHV** bit for both AFE boards. The status for this single status bit is reflected in both bit AFE fields. The bit significance is:

Bit	Supply fail status	Bit	Supply fail status	Bit	Supply fail status	Bit	Supply fail status
8	AFE1_PWR_FAIL_VANA	9	AFE1_PWR_FAIL_VCB	10	AFE_PWR_FAIL_VHV	11	Not used
12	AFE2_PWR_FAIL_VANA	13	AFE2_PWR_FAIL_VCB	14	AFE_PWR_FAIL_VHV	15	Not used

More information

Attribute name **PowerStatusReg** array size 1

Function

Firmware module PSM version 2.21

Description

Provides an indication of the status of the power supply system. This is a read only attribute with the following bit significance:

Bit	Supply status	Bit	Supply status
0	Primary power is enabled	1	AFE power is enabled
2	Vbb supply is enabled	3	AFE VHV+/- supply fail
4	AFE2 VCB+/- supply fail	5	AFE2 VANA+/- supply fail
6	AFE1 VCB+/- supply fail	7	AFE1 VANA+/- supply fail

Usage Read only.

Address 0x020F

Calibration Units Boolean Slope 1.0 Offset 0.0

Limits Maximum 255.0 Minimum 0.0 Default 0.0

Associations

Attributes **PwrUpPrimarySupplies, PwrUpAfeSupplies, VbbPowerEnable.**

Hardware **/AFE1_PWR_FAIL_VANA, /AFE2_PWR_FAIL_VANA, /AFE1_PWR_FAIL_VCB, /AFE2_PWR_FAIL_VCB, /AFE_PWR_FAIL_VHV, VBB_ENBL.**

Notes

Bit 0 reflects the state of the PrimaryPwrIsOn status.
Bit 1 reflects the state of the AfePwrIsOn status.

More information

Attribute name **PsmHdwrVersion** **array size** 1

Function Allows firmware to work with revision –A– PSM hardware

Firmware module PSM **version** 2.21

Description Revision –A- PSM hardware did not have the Vbb voltage generator and the power supply enable signals where 'low true' polarity. This attribute allows the current firmware to control the REV –A- PSB modules by setting the attribute true. Do not change this attribute unless you know what you are doing !!

Usage Read / Write.

Address 0x020E

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 1.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes None.

Hardware **AFE1_PWR_EN_VANA, AFE2_PWR_EN_VANA, AFE1_PWR_EN_VCB, AFE2_PWR_EN_VCB, AFE1_PWR_EN_VHV, AFE2_PWR_EN_VHV, VBB_ENBL.**

Notes This attribute is depreciated and will be removed when all Rev –A– PSM boards have been removed from service.

More information

Attribute name
VhvPolaritySlct **array size** 1

Function
Selects the polarity of the VHV and Vbb voltage generators

Firmware module
PSM **version** 2.21

Description
The default condition (**VhvPolaritySlct** = false) is for the PSM to generate positive VHV voltages (for detector drain biases) and negative Vbb potentials (for detector back side bias). This condition corresponds to the normal N-Channel CCD technology. Setting this attribute true will generate negative VHV potentials and positive Vbb potentials to support P-Channel CCD technology detectors.

This attribute can only be changed when the **PwrUpPrimarySupplies** attribute is set false.

Usage
Read / Write.

Address
0x0205

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **PwrUpPrimarySupplies**.

Hardware **VHV_POL_SLCT.**

Notes
This attribute changes the PSM output of the VHV+/- supply from +32/-5 to +5/-32 volts with respect to AGND. The Vbb supply output changes from 0 to +75v to 0 to –75v.

The dynamic range of the DACs on the AFE boards that generate the high voltage bias potentials is 12 bits. This range is divided across the full positive and negative voltage swing. Programming a negative voltage into these DACs when the VHV supply is programmed for positive potential will slam the bias supply amplifier into the lower rail and may cause damage.

More information

Attribute name
PowerSyncEnable **array size** 1

Function
Enables the switching frequency of the various power supplies to be synchronized.

Firmware module
PSM **version** 2.21

Description
To achieve the lowest possible noise on the detector the PSM supplies need to have their switching frequency synchronized to the pixel read rate. This attribute enables this function. The exact switching frequency of each power supply is controlled by a harmonic of the measured pixel read frequency. This frequency is calculated by measuring the period (in SysClk increments) between the PWRSYNC pulses emitted by the sequencer (nominally one pulse per pixel). Setting this attribute false makes the power supplies switch at their default frequency which is not related to the pixel read rate thus causing power supply rail modulation by the characteristic ripple waveform of switch mode power supplies.

Usage
Read / Write.

Address
0x0200

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 1.0

Associations
Attributes PowerSyncRate,

Hardware **VHV_SYNC, VANA_SYNC, VCB_SYNC, VCC_SYNC, LOGIC_SYNC.**

Notes
The individual power sync frequencies are selected from a lookup table to determine the closest usable harmonic to the pixel rate. The closest usable harmonic is that which allows the supply to run within its' design range of switching frequencies. The harmonics used are 1st, 2nd, 3rd, 6th and 8th generated from the measured pixel read frequency. These sync clocks are available for inspection on the LCB debug signal connector (LCB:J4) using the DbgSigSlct and / or the DbgTrigSlct attributes in the LCB firmware module.

More information
See design document PowerSupplySyncAnalysis.xls
For **DbgSigSlct** and **DbgTrigSlct** attribute use see the wiki pages for additional details:
http://www.noao.edu/wiki/index.php/Firmware_Topics - DbgSigSlct_attribute_values

Attribute name
PowerSyncRate **array size** 1

Function
Used to set and indicate the current pixel read rate for power supply synchronization

Firmware module
PSM **version** 2.21

Description
When the sequencer is emitting power supply synchronization pulses (sequencer PWRSYNC function) this attribute indicates the number of SysClk cycles between the sequencer pulses. If the sequencer is not issuing pulses (i.e. not reading out) then this attribute can be set to force a power supply synchronization frequency.

Usage
Read / Write.

Address
0x0201

Calibration
Units SysClk **Slope** 1.0 **Offset** 0.0

Limits
Maximum 2048.0 **Minimum** 0.0 **Default** 216.0

Associations
Attributes **PowerSyncEnable**

Hardware **VHV_SYNC, VANA_SYNC, VCB_SYNC, VCC_SYNC, LOGIC_SYNC.**

Notes
The SysClk frequency is 53.125MHz; the period is approx.19ns.

The pixel read frequency is calculated as PixFreq = 53.125E6 / **PowerSyncRate**

The default frequency corresponds to approx. 245.9KHz

Operational boundaries to maintain synchronization to the pixel frequency are 26KHz to 547KHz

More information
See design document PowerSupplySyncAnalysis.xls
For **DbgSigSlct** and **DbgTrigSlct** attribute use see the wiki pages for additional details:
http://www.noao.edu/wiki/index.php/Firmware_Topics - DbgSigSlct_attribute_values

Attribute name
VFanPowerEnable **array size** 1

Function
Enables the DHE air circulation fan power supply to provide cooling

Firmware module
PSM **version** 2.21

Description
When this attribute is true the power supply for the DHE internal circulatory fan is enabled. The fan is used to regulate the internal temperature of the DHE.

Usage
Read / Write.

Address
0x0207

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 1.0

Associations
Attributes
VfanServoEnable, VfanTempSetPoint, VfanServoDeadBand, VfanServoPwmValue, VfanTemperature, VFanTempSensorSlct

Hardware
VFAN_ENBL, VFAN_ADJ.

Notes

More information

Attribute name **VFanServoEnable** array size 1

Function
Enables the DHE temperature regulation servo.

Firmware module PSM version 2.21

Description
When set true the internal DHE temperature is regulated by a circulation fan to try and maintain the value set to the **VfanTempSetPoint** attribute.

Usage
Read / Write.

Address
0x0119

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 1.0

Associations
Attributes
VfanPowerEnable, VfanTempSetPoint, VfanServoDeadBand, VfanServoPwmValue, VfanTemperature, VFanTempSensorSlct

Hardware
VFAN_ADJ.

Notes

More information

Attribute name
VFanTempSetPoint **array size** 1

Function
Sets the desired operating temperature for the DHE

Firmware module
PSM **version** 2.21

Description
With the **VfanServoEnable** attribute set true, the servo will attempt to maintain the temperature set into this attribute. The servo only has the capacity to cool down the DHE internal temperature by increasing the circulation of air across the surface of the electronics modules. The electronics modules themselves provide the positive bias through their power dissipation to increase the internal DHE temperature.

Usage
Read / Write.

Address
0x0110

Calibration
Units Deg. **Slope** 16.0 **Offset** 0.0

Limits
Maximum 127.0 **Minimum** 0.0 **Default** 41.0

Associations
Attributes
VfanPowerEnable, VfanServoEnable, VfanServoDeadBand, VfanServoPwmValue, VfanTemperature, VFanTempSensorSlct

Hardware
VFAN_ADJ.

Notes
The slope value used to calibrate the **VfanTemperature** attribute must be the set to the same value as the value for this attribute.

More information

Attribute name
VFanServoDeadBand **array size** 1

Function
Compensate for the servo quantization error in the servo calculation to prevent servo oscillation.

Firmware module
PSM **version** 2.21

Description
Use this attribute to define a span of temperature about the set point temperature where the servo will not try to correct the error. The servo depends on temperature feedback that has a certain quantization error. In addition, all servo calculations are done as fixed point arithmetic which adds to the error of the difference between the set point and actual temperature. Setting this attribute to a fraction of a degree will eliminate hunting of the servo.

Usage
Read / Write.

Address
0x011C

Calibration
Units Deg. **Slope** 16.0 **Offset** 0.0

Limits
Maximum 8.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
VfanPowerEnable, VfanServoEnable, VfanTempSetPoint, VfanServoPwmValue, VfanTemperature, VFanTempSensorSlct

Hardware
VFAN_ADJ.

Notes
The slope value used to calibrate the **VfanTemperature** attribute must be the set to the same value as the value for this attribute.

More information

Attribute name
VFanServoPwmValue **array size** 1

Function
Used to set or indicate the current DHE circulatory fan power level

Firmware module
PSM **version** 2.21

Description
When the **VfanServoEnable** attribute is set true, this attribute indicates the current power level (as a percentage) of the servo to maintain the temperature constant.

When the **VfanServoEnable** attribute is set false, this attribute sets the power level of the internal circulatory fan.

Usage
Read / Write.

Address
0x011A

Calibration
Units Percent **Slope** 1.27 **Offset** 0.0

Limits
Maximum 100.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
VfanPowerEnable, VfanServoEnable, VfanTempSetPoint, VfanServoDeadBand, VfanTemperature, VFanTempSensorSlct

Hardware
VFAN_ADJ.

Notes
This fan power supply is adjustable between the range of 8v and 14v corresponding to the PWM values of 0% to 100%.

More information

Attribute name
VFanTempSensorSlct **array size** 1

Function
Selects the temperature sensor to be used to supply the servo feedback temperature value.

Firmware module
PSM **version** 2.21

Description
There are temperature sensors on each hardware module. Those mounted on the LCB and AFE boards can be used to control the temperature of the DHE by being selected as the feedback temperature seen by the servo. This attribute allows you to select the appropriate sensor as:

Value	Sensor selected	Value	Sensor selected
0	FPGA internal temperature	1	LCB temperature sensor 1
2	LCB temperature sensor 2	3	AFE1 temperature sensor 1
4	AFE2 temperature sensor 2	5	AFE2 temperature sensor 1
6	AFE2 temperature sensor 2		
7	**VfanTemperature** attribute write value (servo testing)		

Usage
Read / Write.

Address
0x011E

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 7.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
PsmModOutStatus, VfanPowerEnable, VfanServoEnable, VfanTempSetPoint, VfanServoDeadBand, VfanTemperature, VFanServoPwmValue

Hardware
VFAN_ADJ.

Notes
Only use the code value of 7 for servo testing.

More information

Attribute name
VFanTemperature **array size** 1

Function
Indicate (or set) the servo feedback temperature

Firmware module
PSM **version** 2.21

Description
When the **VfanTempSensorSlct** attribute is set to any value except 7, this attribute indicates the feedback value to the servo as measured from the selected sensor.

When the **VfanTempSensorSlct** is set to a value of 7, this attribute is writable and allows you to test the servo response by introducing a step function into the servo error function.

Usage
Read / Write.

Address
0x011F

Calibration
Units Deg. **Slope** 16.0 **Offset** 0.0

Limits
Maximum 127.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
VfanPowerEnable, VfanServoEnable, VfanTempSetPoint, VfanServoDeadBand, VfanSensorSlct, VFanServoPwmValue

Hardware
VFAN_ADJ.

Notes
The slope value used to calibrate the **VfanTempSetPoint** attribute must be the set to the same value as the value for this attribute.

More information

Attribute name
HtrPowerEnable **array size** 1

Function
Enables the power supply to provide temperature control to the detector

Firmware module
PSM **version** 2.21

Description
When this attribute is true the power supply for the Detector heater is enabled. The heater is used to regulate the detector temperature.

Usage
Read / Write.

Address
0x0206

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
HtrServoEnable, HtrServoPauseEnable, HtrServoPwmValue, HtrServoDeadBand, HtrTempSensorSlct, HtrTempSetPoint, HtrTemperature, HtrVolts, HtrCurrent.

Hardware
VHTR_ENBL, /VHTR_SUSPEND, VHTR_ADJ, TEMP_1, TEMP_2, HTR_VOLTS, HTR_CURRENT.

Notes

More information

Attribute name **HtrServoEnable** array size 1

Function
Enables the Detector temperature regulation servo.

Firmware module PSM version 2.21

Description
When set true the internal Detector temperature is regulated by a small heater to try and maintain the value set to the **HtrTempSetPoint** attribute.

Usage
Read / Write.

Address
0x0109

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 1.0

Associations
Attributes
HtrPowerEnable, HtrServoPauseEnable, HtrServoPwmValue, HtrServoDeadBand, HtrTempSensorSlct, HtrTempSetPoint, HtrTemperature, HtrVolts, HtrCurrent.

Hardware
VHTR_ENBL, /VHTR_SUSPEND, VHTR_ADJ, TEMP_1, TEMP_2, HTR_VOLTS, HTR_CURRENT.

Notes

More information

Attribute name
HtrTempSetPoint **array size** 1

Function
Sets the desired operating temperature for the Detector

Firmware module
PSM **version** 2.21

Description
With the **HtrServoEnable** attribute set true, the servo will attempt to maintain the detector temperature set into this attribute. The servo only has the capacity to heat the Detector temperature by increasing the power through a small resistive heater attached to the cold plate surface of the detector mount. The dewar cryogen provides the negative (cooling) bias.

Usage
Read / Write.

Address
0x0100

Calibration
Units Kelvin **Slope** 16.0 **Offset** 0.0

Limits
Maximum 500.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
HtrPowerEnable, HtrServoEnable, HtrServoPauseEnable, HtrServoPwmValue, HtrServoDeadBand, HtrTempSensorSlct, HtrTemperature, HtrVolts, HtrCurrent.

Hardware
VHTR_ENBL, /VHTR_SUSPEND, VHTR_ADJ, TEMP_1, TEMP_2, HTR_VOLTS, HTR_CURRENT.

Notes
The slope and offset values used to calibrate the **HtrTemperature** attribute must be the set to the same value as the value for this attribute.

You can indicate the detector temperature in Deg. Celsius by setting the offset value to 273.0.

More information

Attribute name
HtrServoDeadBand **array size** 1

Function
Compensate for the servo quantization error in the servo calculation to prevent servo oscillation.

Firmware module
PSM **version** 2.21

Description
Use this attribute to define a span of temperature about the set point temperature where the servo will not try to correct the error. The servo depends on temperature feedback that has a certain quantization error. In addition, all servo calculations are done as fixed point arithmetic which adds to the error of the difference between the set point and actual temperature. Setting this attribute to a fraction of a degree will eliminate hunting of the servo.

Usage
Read / Write.

Address
0x010C

Calibration
Units Kelvin **Slope** 16.0 **Offset** 0.0

Limits
Maximum 8.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
HtrPowerEnable, HtrServoEnable, HtrServoPauseEnable, HtrServoPwmValue, HtrTempSensorSlct, HtrTempSetPoint, HtrTemperature, HtrVolts, HtrCurrent.

Hardware
VHTR_ENBL, /VHTR_SUSPEND, VHTR_ADJ, TEMP_1, TEMP_2, HTR_VOLTS, HTR_CURRENT.

Notes
The slope and offset values used to calibrate the **HtrTemperature** attribute must be the set to the same value as the value for this attribute.

More information

Attribute name
HtrServoPwmValue **array size** 1

Function
Used to set or indicate the current Detector heater power value

Firmware module
PSM **version** 2.21

Description
When the **HtrServoEnable** attribute is set true, this attribute indicates the current power level (as a percentage) of the servo to maintain the detector temperature constant.

When the **HtrServoEnable** attribute is set false, this attribute sets the power level fed to the detector heater

Usage
Read / Write.

Address
0x010A

Calibration
Units Percent **Slope** 1.27 **Offset** 0.0

Limits
Maximum 100.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
HtrPowerEnable, HtrServoEnable, HtrServoPauseEnable, HtrServoDeadBand, HtrTempSensorSlct, HtrTempSetPoint, HtrTemperature, HtrVolts, HtrCurrent.

Hardware
VHTR_ENBL, /VHTR_SUSPEND, VHTR_ADJ, TEMP_1, TEMP_2, HTR_VOLTS, HTR_CURRENT.

Notes
This heater power supply is an adjustable current source between the range of 0 milliamp and 500milliamps corresponding to the PWM values of 0% to 100%.

More information

Attribute name
HtrTempSensorSlct **array size** 1

Function
Selects the temperature sensor to be used to supply the servo feedback temperature value for the detector.

Firmware module
PSM **version** 2.21

Description
There are two temperature sensors inputs provided on the PSM. These are usually Si diode sensors mounted to the detector mount and, possibly, to the cryogen Dewar. This attribute allows you to select the appropriate sensor as:

Value	Sensor selected	Value	Sensor selected
0	Temp sensor 1	1	Temp sensor 2

These sensors are physically connected to the TSM-UTIL module.

Usage
Read / Write.

Address
0x010E

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
HtrPowerEnable, HtrServoEnable, HtrServoPauseEnable, HtrServoPwmValue, HtrServoDeadBand, HtrTempSetPoint, HtrTemperature, HtrVolts, HtrCurrent.

Hardware
VHTR_ENBL, /VHTR_SUSPEND, VHTR_ADJ, TEMP_1, TEMP_2, HTR_VOLTS, HTR_CURRENT.

Notes

More information

Attribute name **HtrTemperature** array size 1

Function
Indicate the servo feedback value for the detector temperature

Firmware module PSM version 2.21

Description
This attribute indicates the feedback value to the servo as measured from the selected sensor.

Usage
Read / Write.

Address
0x010F

Calibration
Units Kelvin. **Slope** 16.0 **Offset** 0.0

Limits
Maximum 500.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
HtrPowerEnable, HtrServoEnable, HtrServoPauseEnable, HtrServoPwmValue, HtrServoDeadBand, HtrTempSensorSlct, HtrTempSetPoint, HtrVolts, HtrCurrent.

Hardware
VHTR_ENBL, /VHTR_SUSPEND, VHTR_ADJ, TEMP_1, TEMP_2, HTR_VOLTS, HTR_CURRENT.

Notes
The slope and offset values used to calibrate the **HtrTempSetPoint** attribute must be the set to the same value as the value for this attribute.

You can indicate the detector temperature in Deg. Celsius by setting the offset value to 273.0.

More information

Attribute name
HtrServoPauseEnable **array size** 1

Function
Enable the sequencer to pause the power to the detector heater during readout to reduce noise.

Firmware module
PSM **version** 2.21

Description
When this attribute is set true the sequencer can interrupt the power being supplied to the detector during readout by writing the sequencer codes READOUT_BUSY and READOUT_IDLE to the EFR register. This may help reduce readout noise contributions from the controller.

Usage
Read / Write.

Address
0x010B

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 1.0

Associations
Attributes
HtrPowerEnable, HtrServoEnable, HtrServoPwmValue, HtrServoDeadBand, HtrTempSensorSlct, HtrTempSetPoint, HtrTemperature, HtrVolts, HtrCurrent.

Hardware
VHTR_ENBL, /VHTR_SUSPEND, VHTR_ADJ, TEMP_1, TEMP_2, HTR_VOLTS, HTR_CURRENT.

Notes

More information

Attribute name
HtrVolts **array size** 1

Function
Indicates the instantaneous voltage being applied across the detector heater

Firmware module
PSM **version** 2.21

Description
This attribute allows you to calculate instantaneous heater power being applied to the detector heater.

Usage
Read / Write.

Address
0X001F

Calibration
Units Volts **Slope** 228.7 **Offset** 69.8

Limits
Maximum 24.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
HtrPowerEnable, HtrServoEnable, HtrServoPauseEnable, HtrServoPwmValue, HtrServoDeadBand, HtrTempSensorSlct, HtrTempSetPoint, HtrTemperature, HtrCurrent.

Hardware
VHTR_ENBL, /VHTR_SUSPEND, VHTR_ADJ, TEMP_1, TEMP_2, HTR_VOLTS, HTR_CURRENT.

Notes
The voltage is measured using a voltage to frequency technique in the TSM module. This frequency is then measured by the LCB to indicate the potential across the detector heater element. The slope and offset values shown here are nominal and serve to indicate power levels being applied to the heater however, for accurate measurements this sensor must be calibrated each time the TSM / LCB combination is changed.

More information

Attribute name
HtrCurrent **array size** 1

Function
Indicates the instantaneous current flowing through the detector heater

Firmware module
PSM **version** 2.21

Description
This attribute allows you to calculate instantaneous heater power being applied to the detector heater.

Usage
Read / Write.

Address
0x001E

Calibration
Units Milliamps **Slope** 5.88 **Offset** 5.0

Limits
Maximum 600.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
HtrPowerEnable, HtrServoEnable, HtrServoPauseEnable, HtrServoPwmValue, HtrServoDeadBand, HtrTempSensorSlct, HtrTempSetPoint, HtrTemperature, HtrVolts.

Hardware
VHTR_ENBL, /VHTR_SUSPEND, VHTR_ADJ, TEMP_1, TEMP_2, HTR_VOLTS, HTR_CURRENT.

Notes
The current is measured using a current to frequency technique in the TSM module. This frequency is then measured by the LCB to indicate the power through the detector heater element. The slope and offset values shown here are nominal and serve to indicate power levels being applied to the heater however, for accurate measurements this sensor must be calibrated each time the TSM / LCB combination is changed.

More information

Attribute name
VanaPowerEnable **array size** 1

Function
Enables the AFE low voltage analog power supply generator

Firmware module
PSM **version** 2.21

Description
When this attribute is true the low voltage analog power supply for the AFE circuitry is enabled. This supply used to by the AFE to power the interface and video acquisition circuitry.

Usage
Read / Write.

Address
0x0208

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 1.0

Associations
Attributes
Vana+ServoEnable, Vana+SetPoint, Vana+ServoDeadBand, Vana+ServoPwmValue, Vana+Volts, Vana+Amps, Vana-ServoEnable, Vana-SetPoint, Vana-ServoDeadBand, Vana-ServoPwmValue, Vana-Volts, Vana-Amps,

Hardware
VANA_ENBL, VANA+_ADJ, VANA-_ADJ.

Notes

More information

Attribute name **Vana+ServoEnable** array size 1

Function
Enables the servo to stabilize the AFE low voltage positive analog supply.

Firmware module PSM version 2.21

Description
When set true the power supply voltage is regulated to try and maintain the value set to the **Vana+SetPoint** attribute.

Usage
Read / Write.

Address
0x0139

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 1.0

Associations
Attributes
VanaPowerEnable, Vana+SetPoint, Vana+ServoDeadBand, Vana+ServoPwmValue, Vana+Volts, Vana+Amps.

Hardware
VANA+_ADJ.

Notes

More information

Attribute name
Vana+SetPoint **array size** 1

Function
Sets the desired operating voltage for the AFE low voltage positive power supply

Firmware module
PSM **version** 2.21

Description
With the **Vana+ServoEnable** attribute set true, the servo will attempt to maintain the voltage set into this attribute. The purpose of the servo is to control the supply slew rate and to compensate for load and aging effects. The servo has a relatively slow loop response and it is the power supply itself that is designed to maintain voltage stability. The servo merely controls the output voltage and compensates for load losses since the servo feedback is at the point where the supply enters the AFE board.

Usage
Read / Write.

Address
0x0130

Calibration
Units Volts **Slope** 29.4 **Offset** 0.0

Limits
Maximum 12.0 **Minimum** 5.0 **Default** 10.5

Associations
Attributes
VanaPowerEnable, Vana+ServoEnable, Vana+ServoDeadBand, Vana+ServoPwmValue, Vana+Volts, Vana+Amps.

Hardware
VANA+_ADJ.

Notes
The slope and offset values used to calibrate the **Vana+Volts** attribute must be used set the values this attribute.

More information

Attribute name
Vana+ServoDeadBand **array size** 1

Function
Compensate for the servo quantization error in the servo calculation to prevent servo oscillation.

Firmware module
PSM **version** 2.21

Description
Use this attribute to define a span of voltage about the set point value where the servo will not try to correct the error. The servo depends on voltage feedback that has a certain quantization error. In addition, all servo calculations are done as fixed point arithmetic which adds to the error of the difference between the set point and actual voltage. Setting this attribute to a fraction of a volt will eliminate hunting of the servo.

Usage
Read / Write.

Address
0x013C

Calibration
Units Volts **Slope** 29.4 **Offset** 0.0

Limits
Maximum 4.3 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
VanaPowerEnable, Vana+ServoEnable, Vana+SetPoint, Vana+ServoPwmValue, Vana+Volts, Vana+Amps.

Hardware
VANA+_ADJ.

Notes
The slope and offset values used to calibrate the **Vana+Volts** attribute must be used set the values this attribute.

More information

Attribute name
Vana+ServoPwmValue **array size** 1

Function
Used to set or indicate the actual demand value driving the AFE analog positive low voltage generator

Firmware module
PSM **version** 2.21

Description
When the **Vana+ServoEnable** attribute is set true, this attribute indicates the current demand (as a percentage) set to the PSM voltage generator to maintain the voltage constant at the setpoint.

When the **Vana+ServoEnable** attribute is set false, this attribute sets the demand to the PSM voltage generator circuitry.

Usage
Read / Write.

Address
0x013A

Calibration
Units Percent **Slope** 1.27 **Offset** 0.0

Limits
Maximum 100.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
VanaPowerEnable, Vana+ServoEnable, Vana+SetPoint, Vana+ServoDeadBand, Vana+Volts, Vana+Amps.

Hardware
VANA+_ADJ.

Notes
This analog low voltage positive power supply is adjustable between the range of 5v and 12v corresponding to the PWM values of 0% to 100%.

More information

Attribute name **Vana+Volts** **array size** 1

Function Indicates the instantaneous voltage generated by the PSM analog positive low voltage generator

Firmware module PSM **version** 2.21

Description This attribute shows the voltage value of the telemetry measured by the LCB board circuitry before the supply enters into the LCB-MEZ board.

Usage Read only.

Address 0x000E

Calibration **Units** Volts **Slope** 29.4 **Offset** 0.0

Limits **Maximum** 34.8 **Minimum** 0.0 **Default** 0.0

Associations

Attributes **VanaPowerEnable, Vana+ServoEnable, Vana+SetPoint, Vana+ServoPwmValue, Vana+ServoDeadBand, Vana+Amps.**

Hardware **LCB:TVANA+, LCB:J6:2-3.**

Notes The voltage is measured using hardware channel 0 (firmware channel 16) of the SYSMON feature of the Virtex FPGA device.

More information

Attribute name
Vana+Amps **array size** 1

Function
Indicates the instantaneous load current seen by the PSM analog positive low voltage generator

Firmware module
PSM **version** 2.21

Description
This attribute shows the current drawn on the primary analog positive low voltage generator from the telemetry measured by the LCB-MEZ board circuitry before the supply is switched onto the AFE1 board. This current draw is from the AFE1 board. Due to limitations of the FPGA resources, AFE2 current draw is not available as an attribute.

Usage
Read / Write.

Address
0x000F

Calibration
Units Milliamps **Slope** 0.98 **Offset** 0.0

Limits
Maximum 600.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
VanaPowerEnable, Vana+ServoEnable, Vana+SetPoint, Vana+ServoPwmValue, Vana+ServoDeadBand, Vana+Volts.

Hardware
LCB:AFE1_TIVANA+, LCB:J6:24, LCB-MEZ:U32:5

Notes
The current is measured using hardware channel 6 (firmware channel 22) of the SYSMON feature of the Virtex FPGA device.

AFE2 load current is available at the LCB TP1 test point.

More information

Attribute name
Vana-ServoEnable **array size** 1

Function
Enables the servo to stabilize the AFE low voltage negative analog supply.

Firmware module
PSM **version** 2.21

Description
When set true the power supply voltage is regulated to try and maintain the value set to the **Vana-SetPoint** attribute.

Usage
Read / Write.

Address
0x0129

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 1.0

Associations
Attributes
VanaPowerEnable, Vana-SetPoint, Vana-ServoDeadBand, Vana-ServoPwmValue, Vana-Volts, Vana-Amps.

Hardware
VANA-_ADJ.

Notes

More information

Attribute name
Vana-SetPoint **array size** 1

Function
Sets the desired operating voltage for the AFE low voltage negative power supply

Firmware module
PSM **version** 2.21

Description
With the **Vana-ServoEnable** attribute set true, the servo will attempt to maintain the voltage set into this attribute. The purpose of the servo is to control the supply slew rate and to compensate for load and aging effects. The servo has a relatively slow loop response and it is the power supply itself that is designed to maintain voltage stability. The servo merely controls the output voltage and compensates for load losses since the servo feedback is at the point where the supply enters the AFE board.

Usage
Read / Write.

Address
0x0120

Calibration
Units Volts **Slope** 29.2 **Offset** 993.0

Limits
Maximum -5.0 **Minimum** -12.0 **Default** -10.5

Associations
Attributes
VanaPowerEnable, Vana-ServoEnable, Vana-ServoDeadBand, Vana-ServoPwmValue, Vana-Volts, Vana-Amps.

Hardware
VANA-_ADJ.

Notes
The slope and offset values used to calibrate the **Vana-Volts** attribute must be used set the values this attribute.

More information

Attribute name
Vana-ServoDeadBand **array size** 1

Function
Compensate for the servo quantization error in the servo calculation to prevent servo oscillation.

Firmware module
PSM **version** 2.21

Description
Use this attribute to define a span of voltage about the set point value where the servo will not try to correct the error. The servo depends on voltage feedback that has a certain quantization error. In addition, all servo calculations are done as fixed point arithmetic which adds to the error of the difference between the set point and actual voltage. Setting this attribute to a fraction of a volt will eliminate hunting of the servo.

Usage
Read / Write.

Address
0x012C

Calibration
Units Volts **Slope** 29.2 **Offset** 993.0

Limits
Maximum 4.3 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
VanaPowerEnable, Vana-ServoEnable, Vana-SetPoint, Vana-ServoPwmValue, Vana-Volts, Vana-Amps.

Hardware
VANA-_ADJ.

Notes
The slope and offset values used to calibrate the **Vana-Volts** attribute must be used set the values this attribute.

More information

Attribute name
Vana-ServoPwmValue **array size** 1

Function
Used to set or indicate the actual demand value driving the AFE analog negative low voltage generator

Firmware module
PSM **version** 2.21

Description
When the **Vana-ServoEnable** attribute is set true, this attribute indicates the current demand (as a percentage) set to the PSM voltage generator to maintain the voltage constant at the setpoint.

When the **Vana-ServoEnable** attribute is set false, this attribute sets the demand to the PSM voltage generator circuitry.

Usage
Read / Write.

Address
0x012A

Calibration
Units Percent **Slope** 1.27 **Offset** 0.0

Limits
Maximum 100.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
VanaPowerEnable, Vana-ServoEnable, Vana-SetPoint, Vana-ServoDeadBand, Vana-Volts, Vana-Amps.

Hardware
VANA-_ADJ.

Notes
This analog low voltage negative power supply is adjustable between the range of -5v and -12v corresponding to the PWM values of 0% to 100%.

More information

Attribute name **Vana-Volts** **array size** 1

Function Indicates the instantaneous voltage generated by the PSM analog negative low voltage generator

Firmware module PSM **version** 2.21

Description This attribute shows the voltage value of the telemetry measured by the LCB board circuitry before the supply enters into the LCB-MEZ board.

Usage Read only.

Address 0x0010

Calibration **Units** Volts **Slope** 29.2 **Offset** 993.0

Limits **Maximum** 0.0 **Minimum** -34.8 **Default** 0.0

Associations

Attributes **VanaPowerEnable, Vana-ServoEnable, Vana-SetPoint, Vana-ServoPwmValue, Vana-ServoDeadBand, Vana-Amps.**

Hardware **LCB:TVANA-,LCB:J6:15-16.**

Notes The voltage is measured using hardware channel 1 (firmware channel 17) of the SYSMON feature of the Virtex FPGA device.

More information

Attribute name **Vana-Amps** **array size** 1

Function Indicates the instantaneous load current seen by the PSM analog negative low voltage generator

Firmware module PSM **version** 2.21

Description This attribute shows the current drawn on the primary analog negative low voltage generator from the telemetry measured by the LCB-MEZ board circuitry before the supply is switched onto the AFE1 board. This current draw is from the AFE1 board. Due to limitations of the FPGA resources, AFE2 current draw is not available as an attribute.

Usage Read / Write.

Address 0x0011

Calibration **Units** Milliamps **Slope** 0.98 **Offset** 0.0

Limits **Maximum** 600.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes **VanaPowerEnable, Vana-ServoEnable, Vana-SetPoint, Vana-ServoPwmValue, Vana-ServoDeadBand, Vana-Volts.**

Hardware **LCB:AFE1_TIVANA-, LCB:J6:26, LCB-MEZ:U33:5**

Notes The current is measured using hardware channel 7 (firmware channel 23) of the SYSMON feature of the Virtex FPGA device.

AFE2 load current is available at the LCB TP2 test point.

More information

Attribute name
VcbPowerEnable **array size** 1

Function
Enables the AFE medium voltage analog power supply generators

Firmware module
PSM **version** 2.21

Description
When this attribute is true the medium voltage analog power supply for the AFE circuitry is enabled. This supply used to by the AFE to supply the clock and bias amplifier power. It is also used to bias the demand amplifier (**PSM:U27**) used in the Vbb voltage generator.

Usage
Read / Write.

Address
0x0209

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 1.0

Associations
Attributes
Vcb+ServoEnable, Vcb+SetPoint, Vcb+ServoDeadBand, Vcb+ServoPwmValue, Vcb+Volts,Afe1Vcb+Amps, Afe2Vcb+Amps, Vcb-ServoEnable, Vcb-SetPoint, Vcb-ServoDeadBand, Vcb-ServoPwmValue, Vcb-Volts, Afe1Vcb-Amps, Afe2Vcb-Amps.

Hardware
VCB_ENBL, VCB+_ADJ, VCB-_ADJ, VCB_SYNC.

Notes

More information

Attribute name **Vcb+ServoEnable** array size 1

Function
Enables the servo to stabilize the AFE medium voltage positive analog supply.

Firmware module PSM version 2.21

Description
When set true the power supply voltage is regulated to try and maintain the value set to the **Vcb+SetPoint** attribute.

Usage
Read / Write.

Address
0x0149

Calibration Units Boolean Slope 1.0 Offset 0.0

Limits Maximum 1.0 Minimum 0.0 Default 1.0

Associations

Attributes
VcbPowerEnable, Vcb+ServoEnable, Vcb+SetPoint, Vcb+ServoDeadBand, Vcb+ServoPwmValue, Vcb+Volts,Afe1Vcb+Amps, Afe2Vcb+Amps.

Hardware
VCB+_ADJ.

Notes

More information

Attribute name
Vcb+SetPoint **array size** 1

Function
Sets the desired operating voltage for the AFE medium voltage positive power supply

Firmware module
PSM **version** 2.21

Description
With the **Vcb+ServoEnable** attribute set true, the servo will attempt to maintain the voltage set into this attribute. The purpose of the servo is to control the supply slew rate and to compensate for load and aging effects. The servo has a relatively slow loop response and it is the power supply itself that is designed to maintain voltage stability. The servo merely controls the output voltage and compensates for load losses since the servo feedback is at the point where the supply enters the AFE board.

Usage
Read / Write.

Address
0x0140

Calibration
Units Volts **Slope** 29.6 **Offset** 0.0

Limits
Maximum 17.5 **Minimum** 10.0 **Default** 17.5

Associations
Attributes
VcbPowerEnable, Vcb+ServoEnable, Vcb+ServoDeadBand, Vcb+ServoPwmValue, Vcb+Volts, Afe1Vcb+Amps, Afe2Vcb+Amps.

Hardware
VCB+_ADJ.

Notes
The slope and offset values used to calibrate the **Vcb+Volts** attribute must be used set the values this attribute.

More information

Attribute name
Vcb+ServoDeadBand **array size** 1

Function
Compensate for the servo quantization error in the servo calculation to prevent servo oscillation.

Firmware module
PSM **version** 2.21

Description
Use this attribute to define a span of voltage about the set point value where the servo will not try to correct the error. The servo depends on voltage feedback that has a certain quantization error. In addition, all servo calculations are done as fixed point arithmetic which adds to the error of the difference between the set point and actual voltage. Setting this attribute to a fraction of a volt will eliminate hunting of the servo.

Usage
Read / Write.

Address
0x014C

Calibration
Units Volts **Slope** 29.6 **Offset** 0.0

Limits
Maximum 4.3 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
VcbPowerEnable, Vcb+ServoEnable, Vcb+SetPoint, Vcb+ServoPwmValue, Vcb+Volts, Afe1Vcb+Amps, Afe2Vcb+Amps.

Hardware
VCB+_ADJ.

Notes
The slope and offset values used to calibrate the **Vcb+Volts** attribute must be used set the values this attribute.

More information

Attribute name
Vcb+ServoPwmValue **array size** 1

Function
Used to set or indicate the actual demand value driving the AFE analog positive medium voltage generator

Firmware module
PSM **version** 2.21

Description
When the **Vcb+ServoEnable** attribute is set true, this attribute indicates the current demand (as a percentage) set to the PSM voltage generator to maintain the voltage constant at the setpoint.

When the **Vcb+ServoEnable** attribute is set false, this attribute sets the demand to the PSM voltage generator circuitry.

Usage
Read / Write.

Address
0x014A

Calibration
Units Percent **Slope** 1.27 **Offset** 0.0

Limits
Maximum 100.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
VcbPowerEnable, Vcb+ServoEnable, Vcb+SetPoint, Vcb+ServoDeadBand, Vcb+Volts, Afe1Vcb+Amps, Afe2Vcb+Amps.

Hardware
VCB+_ADJ.

Notes
This analog medium voltage positive power supply is adjustable between the range of 10v and 17.5v corresponding to the PWM values of 0% to 100%.

More information

Attribute name **Vcb+Volts** **array size** 1

Function Indicates the instantaneous voltage generated by the PSM analog positive medium voltage generator

Firmware module PSM **version** 2.21

Description This attribute shows the voltage value of the telemetry measured by the LCB board circuitry before the supply enters into the LCB-MEZ board.

Usage Read only.

Address 0x0012

Calibration **Units** Volts **Slope** 29.4 **Offset** 0.0

Limits **Maximum** 34.8 **Minimum** 0.0 **Default** 0.0

Associations

Attributes **VcbPowerEnable, Vcb+ServoEnable, Vcb+SetPoint, Vcb+ServoPwmValue, Vcb+ServoDeadBand, Afe1Vcb+Amps, Afe2Vcb+Amps.**

Hardware **LCB:TVCB+, LCB:J6:7-8.**

Notes The voltage is measured using hardware channel 2 (firmware channel 20) of the SYSMON feature of the Virtex FPGA device.

More information

Attribute name
Afe1Vcb+Amps **array size** 1

Function
Indicates the instantaneous load current from AFE 1 as seen by the PSM analog positive medium voltage generator

Firmware module
PSM **version** 2.21

Description
This attribute shows the current drawn by AFE1 board on the primary analog positive medium voltage generator from the telemetry measured by the LCB-MEZ board circuitry before the supply is switched onto the AFE1 board. This current draw is from the AFE1 board.

Usage
Read only.

Address
0x0013

Calibration
Units Milliamps **Slope** 1.96 **Offset** 0.0

Limits
Maximum 600.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
VcbPowerEnable, Vcb+ServoEnable, Vcb+SetPoint, Vcb+ServoPwmValue, Vcb+ServoDeadBand, Vcb+Volts.

Hardware
LCB:AFE1_TIVCB+, LCB:J6:28, LCB-MEZ:U25:5

Notes
The current is measured using hardware channel 8 (firmware channel 24) of the SYSMON feature of the Virtex FPGA device.

More information

Attribute name
Afe2Vcb+Amps **array size** 1

Function
Indicates the instantaneous load current from AFE 2 as seen by the PSM analog positive medium voltage generator

Firmware module
PSM **version** 2.21

Description
This attribute shows the current drawn by AFE2 board on the primary analog positive medium voltage generator from the telemetry measured by the LCB-MEZ board circuitry before the supply is switched onto the AFE2 board. This current draw is from the AFE2 board.

Usage
Read only.

Address
0x0014

Calibration
Units Milliamps **Slope** 1.96 **Offset** 0.0

Limits
Maximum 600.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
VcbPowerEnable, Vcb+ServoEnable, Vcb+SetPoint, Vcb+ServoPwmValue, Vcb+ServoDeadBand, Vcb+Volts.

Hardware
LCB:AFE2_TIVCB+, LCB:J6:27, LCB-MEZ:U24:5

Notes
The current is measured using hardware channel 12 (firmware channel 28) of the SYSMON feature of the Virtex FPGA device.

More information

Attribute name **Vcb-ServoEnable** array size 1

Function
Enables the servo to stabilize the AFE medium voltage negative analog supply.

Firmware module PSM version 2.21

Description
When set true the power supply voltage is regulated to try and maintain the value set to the **Vcb-SetPoint** attribute.

Usage
Read / Write.

Address
0x0159

Calibration Units Boolean Slope 1.0 Offset 0.0

Limits Maximum 1.0 Minimum 0.0 Default 1.0

Associations

Attributes
VcbPowerEnable, Vcb-SetPoint, Vcb-ServoDeadBand, Vcb-ServoPwmValue, Vcb-Volts, Afe1Vcb-Amps, Afe2Vcb-Amps.

Hardware
VCB-_ADJ.

Notes

More information

Attribute name
Vcb-SetPoint **array size** 1

Function
Sets the desired operating voltage for the AFE medium voltage negative power supply

Firmware module
PSM **version** 2.21

Description
With the **V**cb-**ServoEnable** attribute set true, the servo will attempt to maintain the voltage set into this attribute. The purpose of the servo is to control the supply slew rate and to compensate for load and aging effects. The servo has a relatively slow loop response and it is the power supply itself that is designed to maintain voltage stability. The servo merely controls the output voltage and compensates for load losses since the servo feedback is at the point where the supply enters the AFE board.

Usage
Read / Write.

Address
0x0150

Calibration
Units Volts **Slope** 29.4 **Offset** 995.0

Limits
Maximum -17.5 **Minimum** -10.0 **Default** -17.5

Associations
Attributes
VcbPowerEnable, Vcb-ServoEnable, Vcb-ServoDeadBand, Vcb-ServoPwmValue, Vcb-Volts, Afe1Vcb-Amps, Afe2Vcb-Amps.

Hardware
VCB-_ADJ.

Notes
The slope and offset values used to calibrate the **Vcb-Volts** attribute must be used set the values this attribute.

More information

Attribute name
Vcb-ServoDeadBand **array size** 1

Function
Compensate for the servo quantization error in the servo calculation to prevent servo oscillation.

Firmware module
PSM **version** 2.21

Description
Use this attribute to define a span of voltage about the set point value where the servo will not try to correct the error. The servo depends on voltage feedback that has a certain quantization error. In addition, all servo calculations are done as fixed point arithmetic which adds to the error of the difference between the set point and actual voltage. Setting this attribute to a fraction of a volt will eliminate hunting of the servo.

Usage
Read / Write.

Address
0x015C

Calibration
Units Volts **Slope** 29.4 **Offset** 0.0

Limits
Maximum 4.3 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
VcbPowerEnable, Vcb-ServoEnable, Vcb-SetPoint, Vcb-ServoPwmValue, Vcb-Volts, Afe1Vcb-Amps, Afe2Vcb-Amps.

Hardware
VCB-_ADJ.

Notes
The slope value used to calibrate the **Vcb-Volts** attribute must be used set the values this attribute.

More information

Attribute name
Vcb-ServoPwmValue **array size** 1

Function
Used to set or indicate the actual demand value driving the AFE analog negative medium voltage generator

Firmware module
PSM **version** 2.21

Description
When the **Vcb-ServoEnable** attribute is set true, this attribute indicates the current demand (as a percentage) set to the PSM voltage generator to maintain the voltage constant at the setpoint.

When the **Vcb-ServoEnable** attribute is set false, this attribute sets the demand to the PSM voltage generator circuitry.

Usage
Read / Write.

Address
0x015A

Calibration
Units Percent **Slope** 1.27 **Offset** 0.0

Limits
Maximum 100.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes

VcbPowerEnable, Vcb-ServoEnable, Vcb-SetPoint, Vcb-ServoDeadBand, Vcb-Volts, Afe1Vcb-Amps, Afe2Vcb-Amps.

Hardware

VCB-_ADJ.

Notes
This analog medium voltage negative power supply is adjustable between the range of -10.0v and –17.5v corresponding to the PWM values of 0% to 100%.

More information

Attribute name **Vcb-Volts** **array size** 1

Function Indicates the instantaneous voltage generated by the PSM analog negative medium voltage generator

Firmware module PSM **version** 2.21

Description This attribute shows the voltage value of the telemetry measured by the LCB board circuitry before the supply enters into the LCB-MEZ board.

Usage Read only.

Address 0x0015

Calibration **Units** Volts **Slope** 29.4 **Offset** 995.0

Limits **Maximum** 0.0 **Minimum** -34.8 **Default** 0.0

Associations

Attributes **VcbPowerEnable, Vcb-ServoEnable, Vcb-SetPoint, Vcb-ServoPwmValue, Vcb-ServoDeadBand, Vcb-Amps.**

Hardware **LCB:TVCB-,LCB:J6:13-14.**

Notes The voltage is measured using hardware channel 3 (firmware channel 19) of the SYSMON feature of the Virtex FPGA device.

More information

Attribute name
Afe1Vcb-Amps **array size** 1

Function
Indicates the instantaneous load current seen by the PSM analog negative medium voltage generator

Firmware module
PSM **version** 2.21

Description
This attribute shows the current drawn by AFE1 on the primary analog negative medium voltage generator from the telemetry measured by the LCB-MEZ board circuitry before the supply is switched onto the AFE board. This current draw is from the AFE1 board.

Usage
Read only.

Address
0x0016

Calibration
Units Milliamps **Slope** 1.96 **Offset** 0.0

Limits
Maximum 600.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
VcbPowerEnable, Vcb-ServoEnable, Vcb-SetPoint, Vcb-ServoPwmValue, Vcb-ServoDeadBand, Vcb-Volts.

Hardware
LCB:AFE1_TIVCB-, LCB:J6:30, LCB-MEZ:U20:5

Notes
The current is measured using hardware channel 9 (firmware channel 25) of the SYSMON feature of the Virtex FPGA device.

More information

Attribute name
Afe2Vcb-Amps **array size** 1

Function
Indicates the instantaneous load current seen by the PSM analog negative medium voltage generator

Firmware module
PSM **version** 2.21

Description
This attribute shows the current drawn by AFE2 on the primary analog negative medium voltage generator from the telemetry measured by the LCB-MEZ board circuitry before the supply is switched onto the AFE board. This current draw is from the AFE2 board.

Usage
Read only.

Address
0x0017

Calibration
Units Milliamps **Slope** 1.96 **Offset** 0.0

Limits
Maximum 600.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
VcbPowerEnable, Vcb-ServoEnable, Vcb-SetPoint, Vcb-ServoPwmValue, Vcb-ServoDeadBand, Vcb-Volts.

Hardware
LCB:AFE2_TIVCB-, LCB:J6:29, LCB-MEZ:U17:5

Notes
The current is measured using hardware channel 13 (firmware channel 29) of the SYSMON feature of the Virtex FPGA device.

More information

Attribute name
Vhv+Volts **array size** 1

Function
Indicate the primary power supply voltage for the positive high voltage generator.

Firmware module
PSM **version** 2.21

Description
The positive high voltage generator supplies the potential to power the high voltage bias amplifiers used to bias the detector drains in N-Channel operation. Under these conditions the supply should be approximately +32v.

In P-Channel mode (**VhvPolaritySlct** = 1), this should be approximately +5.0v. This potential is to prevent the high voltage bias amplifier output transistors saturating at or near a zero volts output.

The positive and negative high voltage generators are enabled in common with the medium voltage generators using the **VbbPowerEnable** attribute.

Usage
Read only.

Address
0x0018

Calibration
Units Volts **Slope** 29.4 **Offset** 0.0

Limits
Maximum 34.8 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **VcbPowerEnable, Afe1Vhv+Amps, Afe2Vhv+Amps.**

Hardware **LCB:TVHV+, LCB:J6:10**

Notes
The high voltage generators are not adjustable. Local regulation is provided on the separate AFE boards using LDO linear devices.

The voltage is measured using hardware channel 4 (firmware channel 20) of the SYSMON feature of the Virtex FPGA device.

More information

Attribute name
Afe1Vhv+Amps **array size** 1

Function
Indicate the current from the positive high voltage supply being consumed by the AFE 1 board

Firmware module
PSM **version** 2.21

Description
This is the current drawn on the positive high voltage supply by the AFE 1 board. The measurement is taken from the LCB-MEZ circuitry. The AFE board needs to be powered (**PwrUpAfeSupplies** = 1) up to register the correct value.

Usage
Read only.

Address
0x0019

Calibration
Units Milliamps **Slope** 4.12 **Offset** 0.0

Limits
Maximum 600.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **PwrUpAfeSupplies, Vhv+Volts.**

Hardware **LCB:AFE1_TIVHV+, LCB:J5:10, LCB-MEZ:U12:5**

Notes
The current is measured using hardware channel 10 (firmware channel 26) of the SYSMON feature of the Virtex FPGA device.

More information

Attribute name
Afe2Vhv+Amps **array size** 1

Function
Indicate the current from the positive high voltage supply being consumed by the AFE 2 board.

Firmware module
PSM **version** 2.21

Description
This is the current drawn on the positive high voltage supply by the AFE 2 board. The measurement is taken from the LCB-MEZ circuitry. The AFE board needs to be powered (**PwrUpAfeSupplies** = 1) up to register the correct value.

Usage
Read only.

Address
0x001A

Calibration
Units Milliamps **Slope** 4.12 **Offset** 0.0

Limits
Maximum 600.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **PwrUpAfeSupplies, Vhv+Volts.**

Hardware **LCB:AFE2_TIVHV+, LCB:J5:9, LCB-MEZ:U13:5**

Notes
The current is measured using hardware channel 14 (firmware channel 30) of the SYSMON feature of the Virtex FPGA device.

More information

Attribute name
Vhv-Volts **array size** 1

Function
Indicate the primary power supply voltage for the negative high voltage generator.

Firmware module
PSM **version** 2.21

Description
In P-Channel mode (**VhvPolaritySlct** = 1), the negative high voltage generator supplies the potential to power the high voltage bias amplifiers used to bias the detector drains in P-Channel operation. Under these conditions the supply should be approximately -32v.

In N-Channel mode (**VhvPolaritySlct** = 0), this supply should be read approximately -5.0v. This potential is to prevent the high voltage bias amplifier output transistors saturating at or near a zero volts output.

The positive and negative high voltage generators are enabled in common with the medium voltage generators using the **VbbPowerEnable** attribute.

Usage
Read only.

Address
0x001B

Calibration
Units Volts **Slope** 29.3 **Offset** 968.0

Limits
Maximum 0.0 **Minimum** -34.8 **Default** 0.0

Associations
Attributes **VcbPowerEnable, Afe1Vhv-Amps, Afe2Vhv-Amps.**

Hardware **LCB:TVHV-, LCB:J6:12**

Notes
The high voltage generators are not adjustable. Local regulation is provided on the separate AFE boards using LDO linear devices.

The voltage is measured using hardware channel 5 (firmware channel 21) of the SYSMON feature of the Virtex FPGA device.

More information

Attribute name
Afe1Vhv-Amps **array size** 1

Function
Indicate the current from the negative high voltage supply being consumed by the AFE 1 board.

Firmware module
PSM **version** 2.21

Description
This is the current drawn on the negative high voltage supply by the AFE 1 board. The measurement is taken from the LCB-MEZ circuitry. The AFE board needs to be powered (**PwrUpAfeSupplies** = 1) up to register the correct value.

Usage
Read only.

Address
0x001C

Calibration
Units Milliamps **Slope** 4.12 **Offset** 0.0

Limits
Maximum 600.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **PwrUpAfeSupplies, Vhv-Volts.**

Hardware **LCB:AFE1_TIVHV-, LCB:J5:12, LCB-MEZ:U4:5**

Notes
The current is measured using hardware channel 11 (firmware channel 27) of the SYSMON feature of the Virtex FPGA device.

More information

Attribute name
Afe2Vhv-Amps **array size** 1

Function
Indicate the current from the negative high voltage supply being consumed by the AFE 2 board.

Firmware module
PSM **version** 2.21

Description
This is the current drawn on the negative high voltage supply by the AFE 2 board. The measurement is taken from the LCB-MEZ circuitry. The AFE board needs to be powered (**PwrUpAfeSupplies** = 1) up to register the correct value.

Usage
Read only.

Address
0x001D

Calibration
Units Milliamps **Slope** 4.12 **Offset** 0.0

Limits
Maximum 600.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **PwrUpAfeSupplies, Vhv-Volts.**

Hardware **LCB:AFE2_TIVHV-, LCB:J5:11, LCB-MEZ:U7:5**

Notes
The current is measured using hardware channel 15 (firmware channel 31) of the SYSMON feature of the Virtex FPGA device.

More information

Attribute name
VbbPowerEnable **array size** 1

Function
Enables the detector backside bias voltage generator

Firmware module
PSM **version** 2.21

Description
When this attribute is true the high voltage backside bias supply (Vbb) is enabled. Not ethta this supply, if used, is connected directly to the detector i.e. it does not have a separate “bias enable” attribute that isolates the supply from the detector.

To enable Vbb the **VcbPowerEnable** supply must be enabled since it supplies the demand amplifier (**PSM:U27**) potential.

When **VhvPolaritySlct** = 0 the Vbb supply potential is negative. When **VhvPolaritySlct** = 1 the Vbb supply potential is positive

Usage
Read / Write.

Address
0x0204

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 1.0

Associations
Attributes
VcbPowerEnable, VhvPolaritySlct, VbbServoEnable, VbbSetPoint, VbbServoDeadBand, VbbServoPwmValue, VbbVolts.

Hardware
LCB:VBB_ENBL, LCB:VBB_ADJ, LCB:P1:11, LCB:P1:12, VHV_SYNC, LCB:P1:46, LCB:VHV_POL_SLCT, LCB:P1:45.

Notes

More information

Attribute name **VbbServoEnable** array size 1

Function
Enables the servo to stabilize the detector backside bias voltage generator

Firmware module PSM version 2.21

Description
When set true the power supply voltage is regulated to try and maintain the value set to the **VbbSetPoint** attribute.

Usage
Read / Write.

Address
0x0169

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 1.0

Associations
Attributes
VcbPowerEnable, VhvPolaritySlct, VbbSetPoint, VbbServoDeadBand, VbbServoPwmValue, VbbVolts.

Hardware
LCB:VBB_ADJ, LCB:P1:12.

Notes

More information

Attribute name
VbbSetPoint **array size** 1

Function
Sets the desired operating voltage for the detector backside bias voltage generator

Firmware module
PSM **version** 2.21

Description
With the **VbbServoEnable** attribute set true, the servo will attempt to maintain the voltage set into this attribute. The purpose of the servo is to control the supply slew rate and to compensate for load and aging effects. The servo has a relatively slow loop response and it is the power supply itself that is designed to maintain voltage stability. The servo merely controls the output voltage and compensates for load losses since the servo feedback is at the point where the supply enters the AFE board.

Usage
Read / Write.

Address
0x0160

Calibration
Units Volts **Slope** 25.68 **Offset** 2041.6

Limits
Maximum 80.0 **Minimum** -80.0 **Default** 0.0

Associations
Attributes
VcbPowerEnable, VhvPolaritySlct, VbbServoEnable, VbbServoDeadBand, VbbServoPwmValue, VbbVolts.

Hardware
LCB:VBB_ADJ, LCB:P1:12.

Notes
The slope and offset values used to calibrate the **VbbVolts** attribute must be used set the values this attribute.

More information

Attribute name
VbbServoDeadBand **array size** 1

Function
Compensate for the servo quantization error in the servo calculation to prevent servo oscillation.

Firmware module
PSM **version** 2.21

Description
Use this attribute to define a span of voltage about the set point value where the servo will not try to correct the error. The servo depends on voltage feedback that has a certain quantization error. In addition, all servo calculations are done as fixed point arithmetic which adds to the error of the difference between the set point and actual voltage. Setting this attribute to a fraction of a volt will eliminate hunting of the servo.

Usage
Read / Write.

Address
0x016C

Calibration
Units Volts **Slope** 25.68 **Offset** 0.0

Limits
Maximum 4.9 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
VcbPowerEnable, VhvPolaritySlct, VbbServoEnable, VbbSetPoint, VbbServoPwmValue, VbbVolts.

Hardware
LCB:VBB_ADJ, LCB:P1:12.

Notes
The slope value used to calibrate the **VbbVolts** attribute must be used set the values this attribute.

More information

Attribute name
VbbServoPwmValue **array size** 1

Function
Used to set or indicate the actual demand value driving the detector backside bias voltage generator

Firmware module
PSM **version** 2.21

Description
When the **VbbServoEnable** attribute is set true, this attribute indicates the current demand (as a percentage) set to the PSM voltage generator to maintain the voltage constant at the setpoint.

When the **VbbServoEnable** attribute is set false, this attribute sets the demand to the PSM voltage generator circuitry.

Usage
Read / Write.

Address
0x016A

Calibration
Units Percent **Slope** 1.27 **Offset** 0.0

Limits
Maximum 100.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
VcbPowerEnable, VhvPolaritySlct, VbbServoEnable, VbbSetPoint, VbbServoDeadBand, VbbVolts.

Hardware
LCB:VBB_ADJ, LCB:P1:12.

Notes
The detector backside bias voltage generator is adjustable between the range of 0v to +/-80v corresponding to the PWM values of 0% to 100%. The polarity of the supply depends on the **VhvPolaritySlct** attribute value.

More information

Attribute name
VbbVolts **array size** 1

Function
Indicates the instantaneous voltage of the detector backside bias voltage generator

Firmware module
PSM **version** 2.21

Description
This attribute shows the voltage value of the telemetry measured by the TSM-UTIL board. The detector backside bias voltage is directly connected to the detector via a direct route from the PSM. The telemetry is supplied by a small ADC mounted in the filter circuit for this supply on the TSM-UTIL board. This means that if the controller does not have a TSM attached (i.e. it is on the bench, a misleading value of –79v will be indicated by the telemetry.

Usage
Read only.

Address
0x0022

Calibration
Units Volts **Slope** 25.68 **Offset** 2041.6

Limits
Maximum 80.0 **Minimum** -80.0 **Default** 0.0

Associations
Attributes
VcbPowerEnable, VhvPolaritySlct, VbbServoEnable, VbbSetPoint, VbbServoDeadBand, VbbServoPwmValue.

Hardware
PSM:VBB_SRC, PSM:J2:23, TSM-UTIL:U13, LCB:TSM_SCL_SRC, LCB:TSM_SDA_SRC, LCB:TSM_SDA_SENSE,

Notes
The voltage is measured by a small ADC on the TSM_UTIL board. Telemetry data is read via the TSM I2C interface signals.

More information

Attribute name
MemPowerEnable **array size** 1

Function
Enables power to the LCB image buffer memory device (U31).

Firmware module
PSM **version** 2.21

Description
The LCB Image Buffer Memory is a DDR2 ram which requires a 1.8v power supply. This device consumes approximately 1.8 Watts of power. If the image buffer is not being used (i.e. PIX Attribute **StreamModeEnable** = 1) then this device can be powered down to save power and heat dissipation.

Usage
Read / Write.

Address
0x020C

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 1.0

Associations
Attributes
StreamModeEnable, WrtBuffrDataValue, WrtBuffrIncValue, WrtBuffrLength, WrtBuffrOrigin, ReadBuffrIncValue, ReadBuffrLength, ReadBuffrOrigin, BlkWrtToBuffr, BlkReadFromBuffr.

Hardware
LCB:U37

Notes

More information

Attribute name **VccAmps** array size 1

Function
Indicates the current of the Vcc suppy consumed by the LCB.

Firmware module PSM version 2.21

Description
The LCB requires a single 3.3v supply (Vcc). This attribute indicates the current consumed by the LCB.

Usage
Read only.

Address
0x000D

Calibration Units Amps Slope 393.0 Offset 0.0

Limits Maximum 5.0 Minimum 0.0 Default 0.0

Associations
Attributes None.

Hardware **LCB:U60, LCB:IP33D.**

Notes
The current is measured using dedicated hardware channel **VP0-VN0** (firmware channel 3) of the SYSMON feature of the Virtex FPGA device.

More information

Attribute name
DetectorTemp1 **array size** 1

Function
Indicate the temperature seen by the detector temperature sensor 1

Firmware module
PSM **version** 2.21

Description
The TSM-UTIL board has provision to read two temperature sensors. These sensors are normally used to control the detector temperature itself and perhaps to monitor cryogen tank levels. This attribute indicates the detected temperature of sensor number 1.

Usage
Read only.

Address
0x0020

Calibration
Units Kelvin **Slope** 16.0 **Offset** 0.0

Limits
Maximum 500.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes None.

Hardware **LCB:P1:9, LCB:TEMP_1.**

Notes
LCB:TEMP_1 is a square wave signal generated by the **TSM_UTIL** board. The firmware measures the frequency of this square wave to determine temperature. The expected frequency from the **TSM_UTIL** board 500 Hz per Deg. Kelvin.

If the input signal is beyond the bounds of reasonable frequency range, a value of 512K (8191) is set to the attribute. The bounds are 20K (10KHz) for the lower limit and 423K (211.5KHz) for the upper limit.

More information

Attribute name **DetectorTemp2** array size 1

Function
Indicate the temperature seen by the detector temperature sensor 2

Firmware module PSM version 2.21

Description
The TSM-UTIL board has provision to read two temperature sensors. These sensors are normally used to control the detector temperature itself and perhaps to monitor cryogen tank levels. This attribute indicates the detected temperature of sensor number 2.

Usage
Read only.

Address
0x0021

Calibration
Units Kelvin **Slope** 16.0 **Offset** 0.0

Limits
Maximum 500.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes None.

Hardware **LCB:P1:10, LCB:TEMP_2.**

Notes
LCB:TEMP_2 is a square wave signal generated by the **TSM_UTIL** board. The firmware measures the frequency of this square wave to determine temperature. The expected frequency from the **TSM_UTIL** board 500 Hz per Deg. Kelvin.

If the input signal is beyond the bounds of reasonable frequency range, a value of 512K (8191) is set to the attribute. The bounds are 20K (10KHz) for the lower limit and 423K (211.5KHz) for the upper limit.

More information

Attribute name **FpgaTemp** array size 1

Function
Indicates the internal operating temperature of the FPGA (U27).

Firmware module PSM version 2.21

Description
The Virtex 5 FPGA provides various telemetry values. This attribute indicates the actual temperature of the FPGA die inside the Virtex FPGA package.

Usage
Read only.

Address
0x0000

Calibration
Units Deg C. **Slope** 2.03 **Offset** 555.0

Limits
Maximum 230.0 **Minimum** -273.0 **Default** 0.0

Associations
Attributes
None.

Hardware
None.

Notes
This attribute shows the result from firmware channel 0 of the SYSMON module. This channel is internal to the Virtex FPGA device.

More information

Attribute name
FpgaTempMax **array size** 1

Function
Indicates the maximum measured operating temperature of the FPGA (U27).

Firmware module
PSM **version** 2.21

Description
The Virtex 5 FPGA provides various telemetry values. This attribute indicates the maximum temperature reached by the FPGA die inside the Virtex FPGA package. This measurement is historical and dates from the last reboot event of the FPGA.

Usage
Read only.

Address
0x0005

Calibration
Units Deg C. **Slope** 2.03 **Offset** 555.0

Limits
Maximum 230.0 **Minimum** -273.0 **Default** 0.0

Associations
Attributes
None.

Hardware
None.

Notes
This attribute shows the result from firmware channel 32 of the SYSMON module. This channel is internal to the Virtex FPGA device.

More information

Attribute name
FpgaTempMin **array size** 1

Function
Indicates the minimum measured operating temperature of the FPGA (U27).

Firmware module
PSM **version** 2.21

Description
The Virtex 5 FPGA provides various telemetry values. This attribute indicates the minimum temperature reached by the FPGA die inside the Virtex FPGA package. This measurement is historical and dates from the last reboot event of the FPGA. It usually indicates the ambient temperature of the DHE when power was applied

Usage
Read only.

Address
0x0008

Calibration
Units Deg C. **Slope** 2.03 **Offset** 555.0

Limits
Maximum 230.0 **Minimum** -273.0 **Default** 0.0

Associations
Attributes None.

Hardware None.

Notes
This attribute shows the result from firmware channel 36 of the SYSMON module. This channel is internal to the Virtex FPGA device.

More information

Attribute name
FpgaVRefN **array size** 1

Function
Indicates the FPGA (U27) calibration value used by the SYSMON module for the Vref- voltage.

Firmware module
PSM **version** 2.21

Description
The Virtex 5 FPGA provides various telemetry values. This attribute indicates the value measured as the SYSMON ADC calibration reference for the negative reference.

Usage
Read only.

Address
0x0004

Calibration
Units Volts **Slope** 341.33 **Offset** 0.0

Limits
Maximum 3.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes None.

Hardware **LCB:R16**

Notes
This attribute shows the result from firmware channel 5 of the SYSMON module. This channel is internal to the Virtex FPGA device.

Normal value is 0.0 volts.

More information

Attribute name
FpgaVRefP **array size** 1

Function
Indicates the FPGA (U27) calibration value used by the SYSMON module for the Vref+ voltage.

Firmware module
PSM **version** 2.21

Description
The Virtex 5 FPGA provides various telemetry values. This attribute indicates the value measured as the SYSMON ADC calibration reference for the positive reference.

Usage
Read only.

Address
0x0003

Calibration
Units Volts **Slope** 341.33 **Offset** 0.0

Limits
Maximum 3.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes None.

Hardware **LCB:U9, LCB:TP15, LCB AVDD** supply

Notes
This attribute shows the result from firmware channel 4 of the SYSMON module. This channel is internal to the Virtex FPGA device.

Normal value is 2.5 volts

More information

Attribute name
FpgaVccAux **array size** 1

Function
Indicates the voltage seen on the VccAux supply by the FPGA.

Firmware module
PSM **version** 2.21

Description
The VccAux supply is used internally by the FPGA for analog functions (SYSMON, PLL oscillators, etc.).

Usage
Read / Write.

Address
0x0002

Calibration
Units Volts **Slope** 341.33 **Offset** 0.0

Limits
Maximum 3.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes None.

Hardware **LCB:U83, LCB:TP8, LCB +2.5V** supply

Notes
This attribute shows the result from firmware channel 2 of the SYSMON module. This channel is internal to the Virtex FPGA device.

Normal value is 2.5 volts.

More information

Attribute name
FpgaVccAuxMax **array size** 1

Function
Indicates the maximum voltage seen on the VccAux supply by the FPGA.

Firmware module
PSM **version** 2.21

Description
The VccAux supply is used internally by the FPGA for analog functions (SYSMON, PLL oscillators, etc.). This measurement is historical from the last FPGA reboot event.

Usage
Read only.

Address
0x0007

Calibration
Units Volts **Slope** 341.33 **Offset** 0.0

Limits
Maximum 3.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes None.

Hardware **LCB:U83, LCB:TP8, LCB +2.5V** supply

Notes
This attribute shows the result from firmware channel 34 of the SYSMON module. This channel is internal to the Virtex FPGA device.

More information

Attribute name
FpgaVccAuxMin **array size** 1

Function
Indicates the minimum voltage seen on the VccAux supply by the FPGA.

Firmware module
PSM **version** 2.21

Description
The VccAux supply is used internally by the FPGA for analog functions (SYSMON, PLL oscillators, etc.). This measurement is historical from the last FPGA reboot event.

Usage
Read only.

Address
0x000A

Calibration
Units Volts **Slope** 341.33 **Offset** 0.0

Limits
Maximum 3.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes None.

Hardware **LCB:U83, LCB:TP8, LCB +2.5V** supply

Notes
This attribute shows the result from firmware channel 38 of the SYSMON module. This channel is internal to the Virtex FPGA device.

More information

Attribute name **FpgaVccInt** **array size** 1

Function Indicates the voltage seen on the VccInt supply by the FPGA.

Firmware module PSM **version** 2.21

Description The VccInt supply is used by the FPGA for all internal logic functions.

Usage Read Only.

Address 0x0001

Calibration **Units** Volts **Slope** 341.33 **Offset** 0.0

Limits **Maximum** 3.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes None.

Hardware **LCB:U20, LCB:TP10, +1.0V** supply

Notes This attribute shows the result from firmware channel 1 of the SYSMON module. This channel is internal to the Virtex FPGA device.

Nominal value is 1.00 volts.

More information

Attribute name
FpgaVccIntMax **array size** 1

Function
Indicates the maximum voltage seen on the VccInt supply by the FPGA.

Firmware module
PSM **version** 2.21

Description
The VccInt supply is used by the FPGA for all internal logic functions.

This measurement is historical from the last FPGA reboot event.

Usage
Read only.

Address
0x0006

Calibration
Units Volts **Slope** 341.33 **Offset** 0.0

Limits
Maximum 3.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes None.

Hardware **LCB:U20, LCB:TP10, +1.0V** supply

Notes
This attribute shows the result from firmware channel 33 of the SYSMON module. This channel is internal to the Virtex FPGA device.

More information

Attribute name
FpgaVccIntMin **array size** 1

Function
Indicates the minimum voltage seen on the VccInt supply by the FPGA.

Firmware module
PSM **version** 2.21

Description
The VccInt supply is used by the FPGA for all internal logic functions.

This measurement is historical from the last FPGA reboot event.

Usage
Read only.

Address
0x0009

Calibration
Units Volts **Slope** 341.33 **Offset** 0.0

Limits
Maximum 3.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes None.

Hardware **LCB:U20, LCB:TP10, +1.0V** supply

Notes
This attribute shows the result from firmware channel 37 of the SYSMON module. This channel is internal to the Virtex FPGA device.

More information

Configuration Services Module (CFG) Attributes

The Clock services firmware is a Wishbone master/slave module connected to the FPGA internal Wishbone bus. It has a Wishbone module address value of 0x04.The attributes of this module control the reading of the temperature telemetry and serial number devices on each hardware module, the reading and writing of the hardware eeprom storage devices on each hardware module, the control of the shutter and pre-flash functions, and implements a programmable sequencer for the control and readout of detectors.

Attribute name **CfgResetCmd** array size 1

Function
Provides a local reset to the CFG firmware module

Firmware module CFG version 2.20

Description
Writing a value of 1.0 (true) to this attribute resets the internal functions of the configuration services control firmware.
This action sets the default conditions as follows:
TempScanEnable = 1, **TempScanPeriod** = 300, **ShutterEnable** = 1, **ShutterOpenCmd** = 0, **PreflashEnable** = 1, **PreflashOnCmd** = 0, **ShutterForceStatus** = 1, **SeqEnable** = 0, **DheIsSlave** = 0, **PauseExposure** = 0, **IntegrationTime** = 0.

Usage
Write only.

Address
0xFFFE

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
TempScanEnable, TempScanPeriod, ShutterEnable, ShutterOpenCmd, PreflashEnable, PreflashOnCmd, ShutterForceStatus, SeqEnable, DheIsSlave, PauseExposure, IntegrationTime.

Hardware

Notes

More information

Attribute name **CfgCodeId** array size 1

Function
Returns the CFG Module firmware revision level value

Firmware module CFG version 2.20

Description
Reading this attribute provides the firmware revision level of this module as a major revision level with two decimal places.
Major level revision codes are used to describe application levels (e.g. 1.xx indicates development code, 2.xx are CCD production code versions, 3.xx is IR camera production code, etc.).
Semi-major code changes (i.e. the first decimal) generally incorporate functional changes that require software (assimilate tool) to be used to extract new attribute values and/or incorporate new functionality (e.g. incorporation of a new image buffer scheme, etc.).
Minor revision levels are for bug fixes and/or enhancements without affecting functionality.

Usage
Read only.

Address
0xFFFF

Calibration
Units Revision **Slope** 100.0 **Offset** 2.20

Limits
Maximum 655.35 **Minimum** 0.0 **Default** 0.0

Associations
Attributes None.

Hardware None.

Notes

More information

Attribute name **CfgModuleId** array size 1

Function
Returns the function code of the CFG module to confirm its presence.

Firmware module CFG version 2.20

Description
Reading this attribute enables any interrogating device to confirm the presence of this module at the given module select address. The constant assigned to the CLK identification attribute has the value 203.

Values between 100 and 199 represent MONSOON Orange hardware module identity codes.
Values between 200 and 299 represent MONSOON Torrent firmware module identity codes.

Usage
Read only.

Address
0xFFFE

Calibration
Units Ident **Slope** 1.0 **Offset** 0.0

Limits
Maximum 65535.0 **Minimum** 0.0 **Default** 203.0

Associations
Attributes
None.

Hardware
None.

Notes

More information

Attribute name **CfgModInStatus** **array size** 1

Function Returns the System status word as seen by the module

Firmware module CFG **version** 2.20

Description

The system status word is defined by the interconnect system of the Wishbone bus that interconnects all firmware modules internal to the FPGA. This status word is broadcast to each module and is used to convey state information concerning the configuration and functional state of the controller.

Usage Read only.

Address 0xFFFD

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 0xffffffff **Minimum** 0.0 **Default** 0.0

Associations

Attributes **LCBModOutStatus, PSMModOutStatus, CFGModOutStatus, PIXModOutStatus, AFEModOutStatus, ClkModOutStatus**.

Hardware See the Wiki page link given below.

Notes

More information

See http://www.noao.edu/wiki/index.php/Firmware_Topics - Wishbone_system_status_signal_assignment

Attribute name **CfgModOutStatus** array size 1

Function
Provides local status information on the CFG module state

Firmware module CFG version 2.20

Description
Reading this attribute provides additional state information internal to the CFG module. In this firmware revision the bit significance of this attribute is:

Bit	Significance	Bit	Significance	Bit	Significance
0	ReadoutActive	1	AFE0_ModuleDetect	2	AFE1_ModuleDetect
3	**DheIsSlave**	4	FrameStart	5	LineStart
19:16	BusTimeoutReg	23:20	BusGrantReg	27:24	BusErrorReg
31:28	BusEventStatus				

Usage
Read only.

Address
0xFFFC

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 0xffffffff **Minimum** 0.0 **Default** 0.0

Associations
Attributes **DheIsSlave**

Hardware None.

Notes

More information
See the module CfgRegisterControl_Ver220.vhd in the //{Torrent root}/Xilinx/ModuleBuilds/CFG_Services_Ver220 directory.

Attribute name **mcbControl** array size 1

Function
Provide compatibility to MONSOON Orange sequencer control word

Firmware module CFG version 2.20

Description
This attribute combines several independent attributes into one control word. It is defined to provide backwards compatibility to MONSOON Orange software systems. The separate fields in this attribute need to be used with the RDMSKWRT keyword in their access method in the .csv config file. This keyword allows individual fields to be written without disturbing adjacent fields by first reading the attribute, masking the result, changing the field value, and OR'ing the result back to the read value before writing back to the attribute i.e. read-mask-write operation. The independent fields are:

Bit	Significance	Bit	Significance	Bit	Significance
0	**SeqEnable**	1	**PauseExposure**	3:2	**SeqClkDivide**
4	**DheIsSlave**	15:8	**SyncDelay**		

Usage
Read / write using RDMSKWRT protocol.

Address
0xFFFB

Calibration Units Boolean Slope 1.0 Offset 0.0

Limits Maximum 0xffff Minimum 0.0 Default 0.0

Associations
Attributes **SeqEnable, PauseExposure, SeqClkDivide, DheIsSlave, SyncDelay**

Hardware

Notes

More information

Attribute name **IntegrationTime** array size 1

Function
Sets the required integration time.

Firmware module CFG version 2.20

Description
Sets the target integration time to compare to the integration timer incorporated into the sequencer(**actualIntegrationTime**). The integration timer is controlled by the sequencer by writing two code words to the EFR register (**SeqEFR**). These codes enable and disable the timer. When the timer reaches the target time set by this attribute the bit in the sequencer command register (**SeqCmds**) is set.
These bits can be tested in the sequencer code to determine the end of an exposure.

Usage
Read / write.

Address
0x0000

Calibration
Units Millisec. **Slope** 1.0 **Offset** 0.0

Limits
Maximum 4294967295.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **ActualIntegrationTime**, **CfgResetCmd.**

Hardware

Notes
The value of this attribute can be adjusted while the sequencer timer is running to prolong or shorten the required exposure time.

More information

Attribute name **TempScanEnable** array size 1

Function
Enables temperature telemetry scanning

Firmware module CFG version 2.20

Description
When this attribute is true, the internal logic will scan the hardware temperature sensors on a periodic basis as set by the **TempScanPeriod** attribute. The data from each scan is available in the individual attributes associated with hardware temperature telemetry.
This attribute must be set true if the internal DHE temperature control servo is enabled (**VfanServoEnable**) in the PSM module and the FPGA temperature sensor for Vfan control is *not* selected as the servo feedback source (i.e. the LCB or AFE sensors are being used to sense the DHE temperature for the servo) or if the backside bias (Vbb) supply servo is active (**VbbPowerEnable,VbbServoEnable**).

Usage
Read / write.

Address
0x0010

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 1.0

Associations
Attributes
TempScanPeriod, VfanServoEnable, VfanTempSensorSlct, LcbTemperature1, LcbTemperature2, PsmTemperature1, PsmTemperature2, TsmTemperature1, TsmTemperature2, Afe1Temperature1, Afe1Temperature2, Afe2Temperature1, Afe2Temperature2, VbbPowerEnable,VbbServoEnable

Hardware

Notes
The hardware temperature sensors are part of the individual I2C buses on each hardware module. Scanning is done by reading the two temperature sense devices attached to each active (i.e. detected) I2C bus. The firmware reads a 10-bit value which corresponds to a full scale range of +/-127 Deg. C. with 0.25 Deg. C. resolution. Note that the operating temperature of the DHE is constrained to be much less than this measurement range !

More information

Attribute name **TempScanPeriod** array size 1

Function
Sets the scan interval to read values from the hardware temperature sensors

Firmware module CFG version 2.20

Description
When the temperature scanning is enabled (default state), this attribute sets the period between individual scans. Nominally it should be set to around 300ms if the DHE Temperature servo control is active and the servo temperature sensor is not the FPGA internal temperature sensor (attributes **VfanServoEnable, VfanTempSensorSlct)** or if the backside bias (Vbb) supply servo is active (**VbbPowerEnable,VbbServoEnable**).

Usage
Read / Write.

Address
0x0011

Calibration
Units Millisec. **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1023.0 **Minimum** 0.0 **Default** 300.0

Associations
Attributes
TempScanEnable, VfanServoEnable, VfanTempSensorSlct, LcbTemperature1, LcbTemperature2, PsmTemperature1, PsmTemperature2, TsmTemperature1, TsmTemperature2, Afe1Temperature1, Afe1Temperature2, Afe2Temperature1, Afe2Temperature2, VbbPowerEnable,VbbServoEnable

Hardware

Notes
The temperature scans are suspended if the ReadoutActive flag is being used by the sequencer to indicate when a ‘lowest noise’ state is required (see details on the **SeqEFR** attribute). However, note that if a scan is in progress when the ReadoutActive flag is set true, the scan will continue until the sensors have been read. This does not necessarily mean that interference with the readout process will occur, but be aware that some I2C activity may continue for a short time after the flag has been set.

More information

Attribute name **DetectI2CBus** array size 1

Function
Initiates a search for attached I2C buses.

Firmware module CFG version 2.20

Description
This process is run automatically when the DHE is powered up. This attribute can be used to determine the presence (or lack) of the hardware modules. There is an independent I2C bus, attached and mastered by the FPGA, on each LCB, TSM, PSM and AFE board (module). When this attribute is set true, the logic will scan the hardware with a specific sequence to identify the hardware configuration of the DHE.
When read, this attribute provides bit-position value that indicates the hardware configuration of the DHE. The bit significance is:

Bit	Significance	Bit	Significance	Bit	Significance
0	LCB Present(*)	1	PSM Present	2	TSM Present
3	AFE1 Present	4	AFE2 Present	(*) Always true.	

Usage
Read / write. Read to identify which hardware modules are present. Write to initiate a scan of the hardware.

Address
0x0012

Calibration Units Boolean Slope 1.0 Offset 0.0

Limits Maximum 31.0 Minimum 0.0 Default 1.0

Associations

Attributes

Hardware

MON_SCL, MON_SDA, PSM_SDA_SNS, PSM_SDA_SRC, PSM_SCL_SRC, TSM_SDA_SNS, TSM_SDA_SRC, TSM_SCL_SRC, AFE_SDA_SRC0, AFE_SDA_SNS0, AFE_SCL_SRC0, AFE_SDA_SRC1, AFE_SDA_SNS1, AFE_SCL_SRC1

Notes
Be aware that the signal **AFE_SCL_SRC0** is also used to select the FPGA eeprom revision that is loaded to the FPGA during the cold boot process to allow independent firmware code to be loaded for IR and CCD hardware configurations of the DHE.

More information

Attribute name **ReadTemps** array size 1

Function
Reads temperature values from specific hardware module(s).

Firmware module CFG version 2.20

Description
Setting the appropriate value allows you to update the temperature attributes associated with a specific set of hardware modules. The attribute value is divided into two fields described below:

Bit	Significance
0	Selects temperature sensor 1 or 2
20:16	I2C Channel Address described as:

Bit	Significance	Bit	Significance	Bit	Significance	Bit	Significance
16	LCB I2C Bus.	17	PSM I2C Bus.	18	TSM I2C Bus.	19	AFE1 I2C Bus
20	AFE2 I2C Bus.						

Usage
Write only.

Address
0x0013

Calibration Units Boolean Slope 1.0 Offset 0.0

Limits Maximum 2031617.0 Minimum 0.0 Default 0.0

Associations

Attributes

LcbTemperature1, LcbTemperature2, PsmTemperature1, PsmTemperature2, TsmTemperature1, TsmTemperature2, Afe1Temperature1, Afe1Temperature2, Afe2Temperature1, Afe2Temperature2

Hardware

MON_SCL, MON_SDA, PSM_SDA_SNS, PSM_SDA_SRC, PSM_SCL_SRC, TSM_SDA_SNS, TSM_SDA_SRC, TSM_SCL_SRC, AFE_SDA_SRC0, AFE_SDA_SNS0, AFE_SCL_SRC0, AFE_SDA_SRC1, AFE_SDA_SNS1, AFE_SCL_SRC1

Notes
Multiple hardware modules may be read simultaneously by specifying more than one I2C Channel address bits.

More information
See the wiki pages for additional details:
http://www.noao.edu/wiki/index.php/Firmware_Topics - Addresses_for_I2C_Bus_Devices_.2F_FPGA_B

Attribute name **ReadSerialNums** array size 1

Function
Reads temperature values from specific hardware module(s).

Firmware module CFG version 2.20

Description
Setting the appropriate value allows you to update the hardware silicon serial number attributes associated with a specific set of hardware modules. The attribute value has one field described below:

Bit	Significance
4:0	I2C Channel Address described as:

Bit	Significance	Bit	Significance	Bit	Significance	Bit	Significance
0	LCB I2C Bus.	1	PSM I2C Bus.	2	TSM I2C Bus.	3	AFE1 I2C Bus
4	AFE2 I2C Bus.						

Usage
Write only.

Address
0x0014

Calibration **Units** Boolean **Slope** 65536.0 **Offset** 0.0

Limits **Maximum** 31 **Minimum** 0.0 **Default** 0.0

Associations

Attributes

LcbSerialNum, PsmSerialNum, TsmSerialNum, Afe1SerialNum, Afe2SerialNum.

Hardware

MON_SCL, MON_SDA, PSM_SDA_SNS, PSM_SDA_SRC, PSM_SCL_SRC, TSM_SDA_SNS, TSM_SDA_SRC, TSM_SCL_SRC, AFE_SDA_SRC0, AFE_SDA_SNS0, AFE_SCL_SRC0, AFE_SDA_SRC1, AFE_SDA_SNS1, AFE_SCL_SRC1

Notes
Multiple hardware modules may be read simultaneously by specifying more than one I2C Channel address bits.

Note the default slope value which converts the attribute value to a compatible format for the generic I2C Channel addressing scheme.

More information
See the wiki pages for additional details:
http://www.noao.edu/wiki/index.php/Firmware_Topics - Addresses_for_I2C_Bus_Devices_.2F_FPGA_B

Attribute name **eepRdCmdReg** array size 1

Function
Reads one page from a specific hardware module eeprom data store

Firmware module CFG version 2.20

Description
Setting the appropriate value allows you to read one page from the hardware module eeprom store and update the attributes associated eeprom reading and writing. The attribute value is divided into two fields described below:

Bit	Significance
7:0	Selects the eeprom page number
20:16	I2C Channel Address described as:

Bit	Significance	Bit	Significance	Bit	Significance	Bit	Significance
16	LCB I2C Bus.	17	PSM I2C Bus.	18	TSM I2C Bus.	19	AFE1 I2C Bus
20	AFE2 I2C Bus.						

Usage
Read / write. Reading the attribute after setting it to an appropriate value returns a status which indicates the eeprom read process status. Bit(31)=I2C manager busy, Bit(30)= Error occurred during read - bad I2C acknowledge

Address
0x0020

Calibration Units Boolean Slope 1.0 Offset 0.0

Limits Maximum 2031871.0 Minimum 0.0 Default 0.0

Associations
Attributes **eepDataReg,eepFloatReg**

Hardware **MON_SCL, MON_SDA, PSM_SDA_SNS, PSM_SDA_SRC, PSM_SCL_SRC, TSM_SDA_SNS, TSM_SDA_SRC, TSM_SCL_SRC, AFE_SDA_SRC0, AFE_SDA_SNS0, AFE_SCL_SRC0, AFE_SDA_SRC1, AFE_SDA_SNS1, AFE_SCL_SRC1**

Notes
Only one I2C Channel Address bit may be set for each read. The contents of the eeprom page are read and the same value for each 16-word page are placed in the **eepDataReg**, **eepFloatReg** attributes. The difference between the two attributes sets (as defined in the .csv config file) is to allow the PAN to easily access the data as either unsigned integer values or as floating point values.

More information
See the wiki pages for additional details:
http://www.noao.edu/wiki/index.php/Firmware_Topics - Addresses_for_I2C_Bus_Devices_.2F_FPGA_B

Attribute name **eepWrtCmdReg** array size 1

Function
Writes one page of eeprom store data to specific hardware module

Firmware module CFG version 2.20

Description
Setting the appropriate value allows you to write one page of data from the **eepDataReg** or **eepFloatReg** attributes to the hardware module eeprom store. The attribute value is divided into two fields described below:

Bit	Significance
7:0	Selects the eeprom page number
20:16	I2C Channel Address described as:

Bit	Significance	Bit	Significance	Bit	Significance	Bit	Significance
16	LCB I2C Bus.	17	PSM I2C Bus.	18	TSM I2C Bus.	19	AFE1 I2C Bus
20	AFE2 I2C Bus.						

Usage
Read / write. Reading the attribute after setting it to an appropriate value returns a status which indicates the eeprom read process status. Bit(31)=I2C manager busy, Bit(30)= Error occurred during read - bad I2C acknowledge

Address
0x0021

Calibration Units Boolean Slope 1.0 Offset 0.0

Limits Maximum 2031871.0 Minimum 0.0 Default 0.0

Associations

Attributes **eepDataReg,eepFloatReg**

Hardware **MON_SCL, MON_SDA, PSM_SDA_SNS, PSM_SDA_SRC, PSM_SCL_SRC, TSM_SDA_SNS, TSM_SDA_SRC, TSM_SCL_SRC, AFE_SDA_SRC0, AFE_SDA_SNS0, AFE_SCL_SRC0, AFE_SDA_SRC1, AFE_SDA_SNS1, AFE_SCL_SRC1**

Notes
Sixteen 32-bit data values are written to one page of the specified eeprom storage devices. Multiple I2C Channel Addresses may be specified to write the same data to many eeprom devise simultaneously.

More information
See the wiki pages for additional details:
http://www.noao.edu/wiki/index.php/Firmware_Topics - Addresses_for_I2C_Bus_Devices_.2F_FPGA_B

Attribute name **eepDataReg** **array size** 16

Function Unsigned integer read and write registers for the hardware eeprom data stores

Firmware module CFG **version** 2.20

Description

These registers provide read and write access to the data stored in the hardware eeprom stores. These data are used to hold calibration and hardware configuration data specific to each hardware module. This data is usually read from the hardware modules when a PAN connects to the DHE hardware to prepare a table of data used in the calibration of the hardware. These attributes contain the same data as the **eepFloatReg** attributes. These attributes are described to provide and accept unsigned integer values to/from the PAN computer.

Usage Read / Write.

Address 0x0030 => 0x003F

Calibration **Units** Value **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 4294967300.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes **eepWrtCmdReg, eepRdCmdReg, eepFloatReg**

Hardware **MON_SCL, MON_SDA, PSM_SDA_SNS, PSM_SDA_SRC, PSM_SCL_SRC, TSM_SDA_SNS, TSM_SDA_SRC, TSM_SCL_SRC, AFE_SDA_SRC0, AFE_SDA_SNS0, AFE_SCL_SRC0, AFE_SDA_SRC1, AFE_SDA_SNS1, AFE_SCL_SRC1**

Notes

More information

See the wiki pages for additional details:
http://www.noao.edu/wiki/index.php/Firmware_Topics - Addresses_for_I2C_Bus_Devices_.2F_FPGA_B

Attribute name **eepFloatReg** array size 16

Function
Floating point read and write registers for the hardware eeprom data stores

Firmware module CFG version 2.20

Description
These registers provide read and write access to the data stored in the hardware eeprom stores. These data are used to hold calibration and hardware configuration data specific to each hardware module. This data is usually read from the hardware modules when a PAN connects to the DHE hardware to prepare a table of data used in the calibration of the hardware. These attributes contain the same data as the **eepDataReg** attributes. These attributes are described to provide and accept floating point values to/from the PAN computer.

Usage
Read / Write.

Address
0x0030 => 0x003F

Calibration
Units Value **Slope** 1.0 **Offset** 0.0

Limits
Maximum $\sim 10^{38.53}$ **Minimum** $\sim 10^{-44.85}$ **Default** 0.0

Associations
Attributes
eepWrtCmdReg, eepRdCmdReg, eepDataReg

Hardware
MON_SCL, MON_SDA, PSM_SDA_SNS, PSM_SDA_SRC, PSM_SCL_SRC, TSM_SDA_SNS, TSM_SDA_SRC, TSM_SCL_SRC, AFE_SDA_SRC0, AFE_SDA_SNS0, AFE_SCL_SRC0, AFE_SDA_SRC1, AFE_SDA_SNS1, AFE_SCL_SRC1

Notes
You will not see any difference between these two data register sets when reading the values from the DHE. This is just a way of describing different attributes to facilitate the PAN computers method of interpreting the same data. The difference is in the ‘Vals’ and ‘TypCde’ fields of the Attribute descriptor that is embedded into the VHDL source code

More information
See the wiki pages for additional details:
http://www.noao.edu/wiki/index.php/Firmware_Topics - Addresses_for_I2C_Bus_Devices_.2F_FPGA_B

Attribute name **LcbTemperature1** **array size** 1

Function Returns the temperature measured on the backside lower edge of the LCB.

Firmware module CFG **version** 2.20

Description

Reading this attribute (when temperature scanning is enabled or after the **ReadTemps** attribute has been set to a value of 0x10000) will return the temperature of the sensor device U57 on the LCB module.

Usage Read only.

Address 0x0040

Calibration **Units** Deg. C. **Slope** 16.0 **Offset** 0.0

Limits **Maximum** 127.0 **Minimum** -127.0 **Default** 0.0

Associations

Attributes **ReadTemps, TempScanEnable, TempScanPeriod.**

Hardware **MON_SCL, MON_SDA,** U57

Notes

More information

See schematic TRNT-EL-04-2002_Rb page 7 C2.
See also data sheet fro MCP9803 device at
http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en020951

Attribute name **LcbTemperature2** **array size** 1

Function Returns the temperature measured on the front side of the LCB.

Firmware module CFG **version** 2.20

Description

Reading this attribute (when temperature scanning is enabled or after the **ReadTemps** attribute has been set to a value of 0x10001) will return the temperature of the sensor device U26 on the LCB module.

Usage Read only.

Address 0x0041

Calibration **Units** Deg. C. **Slope** 16.0 **Offset** 0.0

Limits **Maximum** 127.0 **Minimum** -127.0 **Default** 0.0

Associations

Attributes **ReadTemps, TempScanEnable, TempScanPeriod.**

Hardware **MON_SCL, MON_SDA,** U26

Notes

More information

See schematic TRNT-EL-04-2002_Rb page 7 C2.
See also data sheet fro MCP9803 device at
http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en020951

Attribute name **PsmTemperature1** array size 1

Function
Returns the temperature measured on the top side edge of the PSM.

Firmware module CFG version 2.20

Description
Reading this attribute (when temperature scanning is enabled or after the **ReadTemps** attribute has been set to a value of 0x20000) will return the temperature of the sensor device U22 on the PSM module.

Usage
Read only.

Address
0x0042

Calibration
Units Deg. C. **Slope** 16.0 **Offset** 0.0

Limits
Maximum 127.0 **Minimum** -127.0 **Default** 0.0

Associations
Attributes
ReadTemps, TempScanEnable, TempScanPeriod.

Hardware
PSM_SDA_SNS, PSM_SDA_SRC, PSM_SCL_SRC, U22

Notes

More information
See schematic TRNT-EL-04-2001_Rb page 11 C2.
See also data sheet fro MCP9803 device at
http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en020951

Attribute name **PsmTemperature2** array size 1

Function
Returns the temperature measured on the bottom side middle of the PSM.

Firmware module CFG version 2.20

Description
Reading this attribute (when temperature scanning is enabled or after the **ReadTemps** attribute has been set to a value of 0x20001) will return the temperature of the sensor device U36 on the PSM module.

Usage
Read only.

Address
0x0043

Calibration
Units Deg. C. **Slope** 16.0 **Offset** 0.0

Limits
Maximum 127.0 **Minimum** -127.0 **Default** 0.0

Associations
Attributes
ReadTemps, TempScanEnable, TempScanPeriod.

Hardware
PSM_SDA_SNS, PSM_SDA_SRC, PSM_SCL_SRC, PSM U36

Notes

More information
See schematic TRNT-EL-04-2001_Rb page 11 C2.
See also data sheet fro MCP9803 device at
http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en020951

Attribute name **TsmTemperature1** array size 1

Function
Returns the temperature measured on the bottom side of the TSM-UTIL.

Firmware module CFG version 2.20

Description
Reading this attribute (when temperature scanning is enabled or after the **ReadTemps** attribute has been set to a value of 0x40000) will return the temperature of the sensor device U9 on the TSM-UTIL module.

Usage
Read only.

Address
0x0044

Calibration
Units Deg. C. **Slope** 16.0 **Offset** 0.0

Limits
Maximum 127.0 **Minimum** -127.0 **Default** 0.0

Associations
Attributes
ReadTemps, TempScanEnable, TempScanPeriod.

Hardware
TSM_SDA_SNS, TSM_SDA_SRC, TSM_SCL_SRC, TSM-UTIL U9

Notes

More information
See schematic TRNT-EL-04-2009_Ra page 1 D3.
See also data sheet fro MCP9803 device at
http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en020951

Attribute name **TsmTemperature2** array size 1

Function
Returns the temperature measured on the top side of the TSM-UTIL.

Firmware module CFG version 2.20

Description
Reading this attribute (when temperature scanning is enabled or after the **ReadTemps** attribute has been set to a value of 0x40001) will return the temperature of the sensor device U8 on the TSM-UTIL module.

Usage
Read only.

Address
0x0045

Calibration
Units Deg. C. **Slope** 16.0 **Offset** 0.0

Limits
Maximum 127.0 **Minimum** -127.0 **Default** 0.0

Associations
Attributes
ReadTemps, TempScanEnable, TempScanPeriod.

Hardware
TSM_SDA_SNS, TSM_SDA_SRC, TSM_SCL_SRC, TSM-UTIL U8

Notes

More information
See schematic TRNT-EL-04-2009_Ra page 1 D3.
See also data sheet fro MCP9803 device at
http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en020951

Attribute name **Afe1Temperature1** array size 1

Function
Returns the temperature measured on the bottom side of the AFE1 board.

Firmware module CFG version 2.20

Description
Reading this attribute (when temperature scanning is enabled or after the **ReadTemps** attribute has been set to a value of 0x80000) will return the temperature of the sensor device U151 on the AFE module inserted into the bottom position (AFE1).

Usage
Read only.

Address
0x0046

Calibration
Units Deg. C. **Slope** 16.0 **Offset** 0.0

Limits
Maximum 127.0 **Minimum** -127.0 **Default** 0.0

Associations
Attributes
ReadTemps, TempScanEnable, TempScanPeriod.

Hardware
AFE_SDA_SRC0, AFE_SDA_SNS0, AFE_SCL_SRC0, AFE U151

Notes

More information
See schematic TRNT-EL-04-2004_Rc page 11 E4.
See also data sheet fro MCP9803 device at
http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en020951

Attribute name **Afe1Temperature2** array size 1

Function
Returns the temperature measured on the top side of the AFE1 board.

Firmware module CFG version 2.20

Description
Reading this attribute (when temperature scanning is enabled or after the **ReadTemps** attribute has been set to a value of 0x80001) will return the temperature of the sensor device U70 on the AFE module inserted into the bottom position (AFE1).

Usage
Read only.

Address
0x0047

Calibration
Units Deg. C. **Slope** 16.0 **Offset** 0.0

Limits
Maximum 127.0 **Minimum** -127.0 **Default** 0.0

Associations
Attributes
ReadTemps, TempScanEnable, TempScanPeriod.

Hardware
AFE_SDA_SRC0, AFE_SDA_SNS0, AFE_SCL_SRC0, AFE U70

Notes

More information
See schematic TRNT-EL-04-2004_Rc page 11 E4.
See also data sheet fro MCP9803 device at
http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en020951

Attribute name **Afe2Temperature1** array size 1

Function
Returns the temperature measured on the bottom side of the AFE2 board.

Firmware module CFG version 2.20

Description
Reading this attribute (when temperature scanning is enabled or after the **ReadTemps** attribute has been set to a value of 0x100000) will return the temperature of the sensor device U151 on the AFE module inserted into the top position (AFE2).

Usage
Read only.

Address
0x0048

Calibration
Units Deg. C. **Slope** 16.0 **Offset** 0.0

Limits
Maximum 127.0 **Minimum** -127.0 **Default** 0.0

Associations
Attributes
ReadTemps, TempScanEnable, TempScanPeriod.

Hardware
AFE_SDA_SRC1, AFE_SDA_SNS1, AFE_SCL_SRC1, AFE U151

Notes

More information
See schematic TRNT-EL-04-2004_Rc page 11 E4.
See also data sheet fro MCP9803 device at
http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en020951

Attribute name **Afe2Temperature2** array size 1

Function
Returns the temperature measured on the top side of the AFE2 board.

Firmware module CFG version 2.20

Description
Reading this attribute (when temperature scanning is enabled or after the **ReadTemps** attribute has been set to a value of 0x100001) will return the temperature of the sensor device U70 on the AFE module inserted into the top position (AFE2).

Usage
Read only.

Address
0x0049

Calibration
Units Deg. C. **Slope** 16.0 **Offset** 0.0

Limits
Maximum 127.0 **Minimum** -127.0 **Default** 0.0

Associations
Attributes
ReadTemps, TempScanEnable, TempScanPeriod.

Hardware
AFE_SDA_SRC1, AFE_SDA_SNS1, AFE_SCL_SRC1, AFE U70

Notes

More information
See schematic TRNT-EL-04-2004_Rc page 11 E4.
See also data sheet fro MCP9803 device at
http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en020951

Attribute name **LcbSerialNum** array size 1

Function
Returns the value of the silicon serial number from the LCB module.

Firmware module CFG version 2.20

Description
Reading this attribute (after the **ReadSerialNums** attribute has been set to a value of 0x10000) will return the unique silicon serial number device U82 on the LCB module.

Usage
Read only.

Address
0x0050

Calibration
Units SerNum **Slope** 1.0 **Offset** 0.0

Limits
Maximum 4294967295.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **ReadSerialNums**

Hardware **MON_SCL, MON_SDA,** LCB U82

Notes

More information
See schematic TRNT-EL-04-2002_Rb page 7 C2.
See also data sheet fro DS28CM00 device at
http://www.maxim-ic.com/datasheet/index.mvp/id/5248

Attribute name **PsmSerialNum** array size 1

Function
Returns the value of the silicon serial number from the PSM module.

Firmware module CFG version 2.20

Description
Reading this attribute (after the **ReadSerialNums** attribute has been set to a value of 0x20000) will return the unique silicon serial number device U21 on the PSM module.

Usage
Read only.

Address
0x0051

Calibration
Units SerNum **Slope** 1.0 **Offset** 0.0

Limits
Maximum 4294967295.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **ReadSerialNums**

Hardware **PSM_SDA_SNS, PSM_SDA_SRC, PSM_SCL_SRC,** PSM U21

Notes

More information
See schematic TRNT-EL-04-2001_Rb page 11 E2.
See also data sheet fro DS28CM00 device at
http://www.maxim-ic.com/datasheet/index.mvp/id/5248

Attribute name **TsmSerialNum** array size 1

Function
Returns the value of the silicon serial number from the TSM module.

Firmware module CFG version 2.20

Description
Reading this attribute (after the **ReadSerialNums** attribute has been set to a value of 0x40000) will return the unique silicon serial number device U1 on the TSM-UTIL module.

Usage
Read only.

Address
0x0052

Calibration
Units SerNum **Slope** 1.0 **Offset** 0.0

Limits
Maximum 4294967295.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **ReadSerialNums**

Hardware **TSM_SDA_SNS, TSM_SDA_SRC, TSM_SCL_SRC,** TSM-UTIL U1

Notes

More information
See schematic TRNT-EL-04-2009_Ra page 1 D3.
See also data sheet fro DS28CM00 device at
http://www.maxim-ic.com/datasheet/index.mvp/id/5248

Attribute name **Afe1SerialNum** array size 1

Function
Returns the value of the silicon serial number from the AFE1 module.

Firmware module CFG version 2.20

Description
Reading this attribute (after the **ReadSerialNums** attribute has been set to a value of 0x80000) will return the unique silicon serial number device U72 on the AFE module inserted into the lower (AFE1) slot of the LCB.

Usage
Read only.

Address
00x0053

Calibration
Units SerNum **Slope** 1.0 **Offset** 0.0

Limits
Maximum 4294967295.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **ReadSerialNums**

Hardware **AFE_SDA_SRC0, AFE_SDA_SNS0, AFE_SCL_SRC0,** AFE U72

Notes

More information
See schematic TRNT-EL-04-2004_Rc page 11 E3.
See also data sheet fro DS28CM00 device at
http://www.maxim-ic.com/datasheet/index.mvp/id/5248

Attribute name **Afe2SerialNum** array size 1

Function
Returns the value of the silicon serial number from the AFE2 module.

Firmware module CFG version 2.20

Description
Reading this attribute (after the **ReadSerialNums** attribute has been set to a value of 0x100000) will return the unique silicon serial number device U72 on the AFE module inserted into the upper (AFE2) slot of the LCB.

Usage
Read only.

Address
00x0054

Calibration
Units SerNum **Slope** 1.0 **Offset** 0.0

Limits
Maximum 4294967295.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **ReadSerialNums**

Hardware **AFE_SDA_SRC1, AFE_SDA_SNS1, AFE_SCL_SRC1,** AFE U72

Notes

More information
See schematic TRNT-EL-04-2004_Rc page 11 E3.
See also data sheet fro DS28CM00 device at
http://www.maxim-ic.com/datasheet/index.mvp/id/5248

Attribute name **ShutterEnable** array size 1

Function
Enables the shutter to be controlled via commands from the sequencer

Firmware module CFG version 2.20

Description
Setting this attribute true enables the sequencer to use the EFR register commands to open and close the shutter via the control shutter control signal (**SHUTTER_OPEN**) during an integration. **SHUTTER_OPEN** is available on the TSM-UTIL connector J2 (connected to the TSM chassis mounted shutter connector). Setting this attribute false will disable the sequencer control of the shutter, thus allowing timed dark integrations to be made without modifying the sequencer code path. This attribute does not affect the manual operation of the shutter via the **ShutterOpenCmd** attribute i.e. when this attribute is false, the shutter may still be controlled manually by the PAN.

Usage
Read / Write.

Address
0x0060

Calibration Units Boolean Slope 1.0 Offset 0.0

Limits Maximum 1.0 Minimum 0.0 Default 1.0

Associations
Attributes **ShutterStatus**

Hardware **SHUTTER_OPEN_CMD**

Notes

More information

Attribute name **PreflashEnable** array size 1

Function
Enables the pre-flash signal to be controlled via commands from the sequencer

Firmware module CFG version 2.20

Description
Setting this attribute true enables the sequencer to use the EFR register commands to control the pre-flash signal via the control pre-flash control signal (**PREFLASH_ON**) during an integration. **PREFLASH_ON** is available on the TSM-UTIL connector J2 (connected to the TSM chassis mounted shutter connector). Setting this attribute true will enable the sequencer control of a pre-flash source (i.e. LED, etc.), thus allowing timed flat integrations to be made without modifying the sequencer code path. This attribute does not affect the manual operation of the pre-flash signal via the **PreflashOnCmd** attribute i.e. when this attribute is false, the pre-flash may still be controlled manually by the PAN.

Usage
Read / Write.

Address
0x0062

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **PreflashPolarity**

Hardware **PREFLASH_ON, SHUTTER_RTN.**

Notes

More information

Attribute name **ShutterOpenCmd** **array size** 1

Function Manually controls the shutter state.

Firmware module CFG **version** 2.20

Description

Setting this attribute true overrides any sequencer control of the shutter and sets the shutter to the open state.

Usage Read / Write.

Address 0x0061

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 1.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes **ShutterStatus, ShutterForceStatus, ShutterPolarity**

Hardware **SHUTTER_OPEN_CMD**

Notes

The shutter control signal is opto-coupled to an open collector output. The output transistor has a 70V VCE maximum working voltage and a maximum current capacity of 50ma or can dissipate 150mW, whichever comes first.

The shutter polarity attribute allows the ‘normally open’ or ‘normally closed’ state for the DHE shutter closed state.

More information

See data sheet for SFH690 Optocoupler series:
http://www.vishay.com/product?docid=83686

Attribute name **PreflashOnCmd** array size 1

Function
Manually controls the pre-flash state.

Firmware module CFG version 2.20

Description
Setting this attribute true overrides any sequencer control of the pre-flash signal and sets the pre-flash to the on state. The pre-flash signal can be used to control a light source internal to the detector Dewar to allow flat field exposures to be made in-situ. It can also be used for any other (clean please) purpose that requires an external signal to control it.

Usage
Read / Write.

Address
0x0063

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes

Hardware **PREFLASH_ON, SHUTTER_RTN**

Notes
The pre-flash control signal is opto-coupled to an open collector output. The output transistor has a 70V VCE maximum working voltage and a maximum current capacity of 50ma or can dissipate 150mW, whichever comes first.
The **Preflashpolarity** attribute allows the ‘normally open’ or ‘normally closed’ state for the DHE pre-flash off state.

More information
See data sheet for SFH690 Optocoupler series:
http://www.vishay.com/product?docid=83686

Attribute name **ShutterForceStatus** **array size** 1

Function Disables the external shutter position status signals

Firmware module CFG **version** 2.20

Description

When true, this attribute connects the shutter status signals directly to the internal controller shutter status i.e. opening the shutter will show open status, closing the shutter will show closed status. This attribute is set true if there is no external shutter position status available.

Usage Read / Write.

Address 0x0064

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 1.0 **Minimum** 0.0 **Default** 1.0

Associations

Attributes **ShutterOpenCmd, ShutterOpenTime, ShutterCloseTime, ShutterStatus**.

Hardware None.

Notes External shutter position status is used to compute the shutter transit time. If this attribute is set true, the **ShutterOpenTime, ShutterCloseTime** attributes will not provide this information.

More information

Attribute name ShutterOpenTime array size 1

Function
Reports the shutter transit time from close to open position.

Firmware module CFG version 2.20

Description
This attribute measures the time from the point that the shutter closed status bit goes false until the shutter open status bit goes true.

Usage
Read only.

Address
0x0065

Calibration
Units Millisec. **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1023.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
ShutterOpenCmd, ShutterForceStatus, ShutterPolarity, ShutterStatusPolarity.

Hardware
TSM_UTIL **SHUTTER_SENSE_OPEN_P, SHUTTER_SENSE_OPEN_N, SHUTTER_SENSE_CLOSE_P, SHUTTER_SENSE_CLOSE_N**

Notes
The **ShutterPolarity** and **ShutterStatusPolarity** attributes must be set appropriately to sense the correct transition. If reversed, this attribute will not report the correct value.

The **SHUTTER_SENSE_OPEN_P, SHUTTER_SENSE_OPEN_N, SHUTTER_SENSE_CLOSE_P, SHUTTER_SENSE_CLOSE_N** signals are uncommitted inputs to SFH690 opto-couplers. Maximum forward current should be externally limited to approx. 10ma. Forward voltage drop of the diode is approx. 1.2v.

More information
See data sheet for SFH690 Optocoupler series:
http://www.vishay.com/product?docid=83686

Attribute name ShutterCloseTime array size 1

Function
Reports the shutter transit time from open to closed position.

Firmware module CFG version 2.20

Description
This attribute measures the time from the point that the shutter open status bit goes false until the shutter closed status bit goes true.

Usage
Read only.

Address
0x0066

Calibration
Units Millisec. **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1023 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
ShutterOpenCmd, ShutterForceStatus, ShutterPolarity, ShutterStatusPolarity.

Hardware
TSM_UTIL **SHUTTER_SENSE_OPEN_P, SHUTTER_SENSE_OPEN_N, SHUTTER_SENSE_CLOSE_P, SHUTTER_SENSE_CLOSE_N**

Notes
The **ShutterPolarity** and **ShutterStatusPolarity** attributes must be set appropriately to sense the correct transition. If reversed, this attribute will not report the correct value.

The **SHUTTER_SENSE_OPEN_P, SHUTTER_SENSE_OPEN_N, SHUTTER_SENSE_CLOSE_P, SHUTTER_SENSE_CLOSE_N** signals are uncommitted inputs to SFH690 opto-couplers. Maximum forward current should be externally limited to approx. 10ma. Forward voltage drop of the diode is approx. 1.2v.

More information
See data sheet for SFH690 Optocoupler series:
http://www.vishay.com/product?docid=83686

Attribute name **ShutterStatus** array size 1

Function
Reports the position and operational status of the shutter

Firmware module CFG version 2.20

Description
When connected to external shutter position sense electronics, this attribute shows the positional state of the shutter. There are two bits that combine to give four possible states. The status is expressed as:

Value	Shutter state
0	Forced status or shutter in transit
1	Shutter is open
2	Shutter is closed
3	Shutter is jammed

Usage
Read only.

Address
0x0067

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 3.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
ShutterOpenCmd, ShutterForceStatus, ShutterPolarity, ShutterStatusPolarity.

Hardware
TSM_UTIL **SHUTTER_SENSE_OPEN_P, SHUTTER_SENSE_OPEN_N, SHUTTER_SENSE_CLOSE_P, SHUTTER_SENSE_CLOSE_N**

Notes
The **SHUTTER_SENSE_OPEN_P, SHUTTER_SENSE_OPEN_N, SHUTTER_SENSE_CLOSE_P, SHUTTER_SENSE_CLOSE_N** signals are uncommitted inputs to SFH690 opto-couplers. Maximum forward current should be externally limited to approx. 10ma. Forward voltage drop of the diode is approx. 1.2v.
The shutter status is based on the availability of two independent signals from the shutter assembly; open status and closed status. If only one status signal is available from the shutter assembly, the Torrent hardware status signals can be wired in parallel with reversed polarity to provide the required input to drive the status system.

More information
See data sheet for SFH690 Optocoupler series:
http://www.vishay.com/product?docid=83686

Attribute name **ShutterPolarity** array size 1

Function
Sets the polarity of the shutter control signal

Firmware module CFG version 2.20

Description
This attribute provides a way to establish the electrical polarity of the shutter control signal. The shutter control signal is the open collector output of an opto-coupler device (PSM U43).

Setting this attribute false activates the opto-coupler when the shutter is commanded to open and allows the open collector output to conduct to the **SHUTTER_RTN** signal to open the shutter.

Setting this attribute true activates the opto-coupler when the shutter is commanded to close and allows the open collector output to conduct to the **SHUTTER_RTN** signal to close the shutter.

Usage
Read / Write.

Address
0x0068

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **ShutterOpenCmd**

Hardware TSM-UTIL J2 **SHUTTER_OPEN, SHUTTER_RTN**

Notes
The shutter control signal is opto-coupled to an open collector output. The output transistor has a 70V VCE maximum working voltage and a maximum current capacity of 50ma or can dissipate 150mW, whichever comes first.

More information
See data sheet for SFH690 Optocoupler series:
http://www.vishay.com/product?docid=83686

Attribute name **PreflashPolarity** array size 1

Function
Sets the polarity of the pre-flash control signal

Firmware module CFG version 2.20

Description
This attribute provides a way to establish the electrical polarity of the pre-flash control signal. The pre-flash control signal is the open collector output of an opto-coupler device (PSM U23).

Setting this attribute false activates the opto-coupler when the pre-flash is commanded ‘on’ and allows the open collector output to conduct to the **SHUTTER_RTN** signal to power the pre-flash circuit.

Setting this attribute true activates the opto-coupler when the pre-flash is commanded ‘off’ and allows the open collector output to conduct to the **SHUTTER_RTN** signal to power down the pre-flash circuit.

Usage
Read / Write.

Address
0x0069

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **PreflashOnCmd**

Hardware TSM-UTIL J2 **PREFLASH_ON, SHUTTER_RTN.**

Notes
The pre-flash control signal is opto-coupled to an open collector output. The output transistor has a 70V VCE maximum working voltage and a maximum current capacity of 50ma or can dissipate 150mW, whichever comes first.

More information
See data sheet for SFH690 Optocoupler series:
http://www.vishay.com/product?docid=83686

Attribute name **ShutterStatusPolarity** array size 1

Function
Establish the polarity of the shutter status signals.

Firmware module CFG version 2.20

Description
Use this attribute to establish the correct polarity for the two status signals that represent ‘open’ and ‘closed’ status for the shutter.

Setting this attribute false will establish ‘low true’ polarity for the status signals i.e. opto-coupler is not turned on indicates true status.

Setting this attribute true will establish ‘high true’ polarity for the status signals i.e. opto-coupler is turned on indicates true status.

Usage
Read / Write.

Address
0x006A

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
ShutterStatus, ShutterOpenTime, ShutterCloseTime.

Hardware
TSM_UTIL **SHUTTER_SENSE_OPEN_P, SHUTTER_SENSE_OPEN_N, SHUTTER_SENSE_CLOSE_P, SHUTTER_SENSE_CLOSE_N**

Notes
The **SHUTTER_SENSE_OPEN_P, SHUTTER_SENSE_OPEN_N, SHUTTER_SENSE_CLOSE_P, SHUTTER_SENSE_CLOSE_N** signals are uncommitted inputs to SFH690 opto-couplers. Maximum forward current should be externally limited to approx. 10ma. Forward voltage drop of the diode is approx. 1.2v.
The shutter status is based on the availability of two independent signals from the shutter assembly; open status and closed status. If only one status signal is available from the shutter assembly, the Torrent hardware status signals can be wired in parallel with reversed polarity to provide the required input to drive the status system.

More information
See data sheet for SFH690 Optocoupler series:
http://www.vishay.com/product?docid=83686

Attribute name **DheIsSlave** array size 1

Function
Forces the DHE Controller to use external synchronization logic.

Firmware module CFG version 2.20

Description
Multiple Torrent DHE modules may be used to synchronously control an array of detectors when one DHE has insufficient resources to provide the necessary clock, bias, and video circuits. The DHE's are daisy chained together using standard RJ45 cables through the LCB SYNC_IN and SYNC_OUT ports (J8, J9). These cables provide for clock and 'start_exposure' command synchronization. Under these conditions, all DHE's are loaded with identical sequencer programs and one DHE is designated master while all other are designated as slaves by setting this attribute true. This forces the slave DHE modules to acquire and use the external synchronization signals on J9.

Usage
Read / Write.

Address
0x0080

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
SeqCmds, SyncDelay, SlaveClkMode, SlaveClkXferEn, SyncInEqualization, SyncOutEqualization.

Hardware
INSYNC_STB, INSYNC_CLK, OUTSYNC_STB, OUTSYNC_CLK.

Notes
The functionality to use synchronized Torrent DHEs is not implemented in this firmware version. This attribute should be set to false.

More information

Attribute name **SeqEnable** array size 1

Function
Enables the sequencer to run.

Firmware module CFG version 2.20

Description
The sequencer employed in Torrent is a small programmable microprocessor capable of writing to all attributes, implementing timing functions and allows conditional branching. Setting this attribute true and allows the sequencer code to run from the instruction at the first program position.
Setting this attribute false stops sequencer program execution, resets the *start_exp* flag and *start_vector* bits in the **SeqCmds** attribute, sets the sequencer program counter to zero, resets the *integration_timer_run*, *readout_busy*, *pixel_data_disable*, and *sync_out_high* flags, closes the shutter, and switches off pre-flash in the **SeqEFR** register, Clears all stack pointers, sets the sequencer write mode to be 32-bit (LMR), sets the device address register (LDA) to zero, clears all loop counts, and cancels any running delay timers.

Usage
Read / Write.

Address
0x0100

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 1.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **McbControl**, **SeqCmds, SeqEFR.**

Hardware

Notes

More information
Torrent Sequencer user manual.

Attribute name **ActualIntegrationTime** **array size** 1

Function Returns the value of the integration timer

Firmware module CFG **version** 2.20

Description

This attribute will return the incremental time from when the integration timer was enabled by the sequencer writing a code to the EFR register. It can be used to determine what the current exposure is and when the readout process will occur.
When the value of this attribute equals or exceeds the value written to the **IntegrationTime** attribute, the *terminal_count (TC)* flag is set in the SeqCmds attribute.

Usage Read only.

Address 0x0101

Calibration **Units** millisec **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 4294967300.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes **SeqEFR,SeqCmds.**

Hardware None.

Notes In sequencer code, write the value of 4 to the EFR register to start the integration counter, write the value of 8 to stop the integration timer. The EFR cannot be written to directly by the PAN.

More information Torrent Sequencer user manual

Attribute name **SeqCmds** array size 1

Function
Returns the state of the sequencer command register

Firmware module CFG version 2.20

Description
The sequencer command register is used to control the sequencer operation. It is used when a conditional branch instruction is encountered in the sequencer code to redirect sequencer program flow. It is a mixture of firmware and software conditions. The are six separate in this 16-bit attribute value:

Bit(s)	Significance
0	Always true, used for direct branching.
1	*ext_sync* state – used in multiple master slave DHE apps.
2	*terminal_count (TC)* Flag - **actualIntegrationTime** >= **IntegrationTime**
3	*start_exp* Command received – Used to initiate an exposure sequence
11:4	*start_vector* – Indicates which sequence to initiate when the *start_exp* flag
15:12	*user_bits* – General flags written directly from PAN to alter seq pgm flow.

Usage
Read only.

Address
0x0102

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 65535.0 **Minimum** 0.0 **Default** 1.0

Associations
Attributes
SeqEnable, actualIntegrationTime, IntegrationTime, SeqUserBits.

Hardware

Notes

More information
Torrent Sequencer user manual

Attribute name **PauseExposure** array size 1

Function

Allows an active integration to be paused

Firmware module CFG version 2.20

Description

Setting this attribute true will close the shutter (if it has been commanded open by the sequencer), switch off the pre-flash (if it had been switched on by the sequencer) and suspend the integration timer indefinately.

Setting this attribute false will open the shutter (if it has been previously commanded open by the sequencer), switch on the pre-flash (if it had been previously switched on by the sequencer) and resume the integration timer increment.

Usage

Read / Write.

Address

0x0103

Calibration

Units Boolean **Slope** 1.0 **Offset** 0.0

Limits

Maximum 1.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes **ActualIntegrationTime, ShutterStatus**

Hardware TSM-UTIL J12, **SHUTTER_OPEN, PREFLASH_ON, SHUTTER_RTN**

Notes

More information

Attribute name **SyncDelay** array size 1

Function
Sets the delay for a master DHE to issue a SYNC pulse on the SYNC_OUT port

Firmware module CFG version 2.20

Description
This attribute sets the delay from when the start exposure (*start_exp*) flag has been set in the master DHE to when the master emits the required sync pulse (via J8) to the daisy chained slave DHEs. This is to allow sufficient time for all slave DHEs to have received the start_exposure commands from their respective PANs and the slave DHE sequencer be in a condition of waiting for the master sync pulse arrival to start the sequence. The arrival of the master *ext_sync* flag in the **SeqCmds** attribute is also delayed by the value in this attribute.

Usage
Read / Write.

Address
0x0104

Calibration
Units millisec **Slope** 1.0 **Offset** 0.0

Limits
Maximum 255.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **SeqCmds**

Hardware LCB J8 **OUTSYNC_STB**

Notes
Note that multiple master / slave DHE implementations is not supported in this firmware revision.

More information

Attribute name **SeqUserBits** array size 1

Function
Allows the PAN to set the *user_bits* to control sequencer program flow

Firmware module CFG version 2.20

Description
The PAN can directly set and reset four bits of the **SeqCmds** register (bits 15:12). These bits can be tested by an active sequencer program using the conditional branch instructions. In this way the PAN can directly influence the program flow of the sequencer code. Normally, the LSB is reserved for debugging sequencer code and is used as a 'continuous run' flag to cycle the sequencer code without end.

Usage
Read / Write.

Address
0x0105

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 15.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **SeqCmds**

Hardware

Notes
These bits are not reset by the **SeqEnable** attribute state i.e. they are persistent.

More information
Torrent Sequencer user manual

Attribute name **SeqClkDivide** array size 1

Function
Allows for slowing down the basic sequencer clock cycle period.

Firmware module CFG version 2.20

Description
The basic sequencer clock cycle period for the Torrent sequencer is 37ns. This value can be adjusted by setting this attribute to values greater than zero. The association between the instruction cycle time and the value of this attribute is:

Value	Sequencer clock period
0	37ns
1	74ns
2	148ns
3	296ns

This value directly affects the period of each instruction cycle and the period of the DSC instruction. It does not affect the other timer instruction periods i.e. DUS and DMS instructions always provide timed delays in microsecs. and millisecs. respectively..

Usage
Read / Write.

Address
0x0106

Calibration **Units** Boolean. **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 3.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes

Hardware

Notes

More information

Attribute name **SeqStatus** array size 1

Function
Returns run time status of the sequencer.

Firmware module CFG version 2.20

Description
This attribute returns information about the current run time state of the sequencer micro-processor. It is not very useful (because it is only a snapshot and cannot be continuously monitored by the PAN) but can indicate activity of the sequencer code. The bit fields are described below:

Bit(s)	Significance
0	Sequencer run flag – the sequencer is running
1	Sequencer bus request flag – sequencer is waiting for a WB bus grant
2	Wishbone write request – the sequencer is active on the bus
17:8	Sequencer program counter value
29:24	Sequencer internal address stack pointer value i.e. subroutine depth

Usage
Read only.

Address
0x0107

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 1057226503.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **SeqEnable**

Hardware

Notes

More information

Attribute name **SeqEFR** array size 1

Function
Returns the value of the internal sequencer EFR register

Firmware module CFG version 2.20

Description
The EFR register is used by the sequencer to directly control firmware and hardware functions and provide operating modes for the sequencer code. The bit significance for this register is:

Bit	Significance
0	*reset_start_exp* – reset the start exposure bit in the SeqCmds register
1	*enable_int_counter* – enable the integration timer
2	*shutter_open_cmd* – Shutter is commanded to be 'open'
3	*pre-flash_on_cmd* – Pre-flash is commanded to be 'on'
4	*pix_data_disable* – Disable pixel data flow pipeline
5	*readout_in_progress* – sequencer is in process of reading out a detector
6	*power_supply_sync* – synchronize power supply to pixel rate
7	*sync_out_true* – set the sync pulse to slave DHEs high

Usage Read only.

Address 0x0108

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 255.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **SeqCmds, SeqEnable, actualIntegrationTime.**

Hardware

Notes

More information

Attribute name **SeqTST** array size 1

Function
Returns the value of the data from a sequencer read operation.

Firmware module CFG version 2.20

Description
This attribute is not used. It is intended for future firmware revisions where the sequencer has expanded capability of reading an attribute and performing a conditional branch on the result.

Usage
Read only.

Address
0x0109

Calibration
Units Value **Slope** 1.0 **Offset** 0.0

Limits
Maximum 4294967299.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes

Hardware

Notes
Not implemented in this version of firmware.

More information

Attribute name **SeqLoopReg** array size 16

Function
Sets the value of the sequencer loop registers to control iteration functions

Firmware module CFG version 2.20

Description
There are sixteen sequencer loop attribute registers designed to support iteration control for the sequencer operation. These registers are mainly used to describe the number of rows and columns in a detector structure to control the sequencer program flow. These registers are used with the sequencer L RB (loop register begin) and LPE (loop end) sequencer instructions.

Usage
Read / Write

Address
0x0110 => 0x011F

Calibration
Units Value **Slope** 1.0 **Offset** 0.0

Limits
Maximum 65535.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes

Hardware

Notes

More information

Attribute name **SeqPatMem** array size 4096

Function
Defines the start address of the sequencer pattern store memory

Firmware module CFG version 2.20

Description
The sequencer pattern store is used to hold 32-bit constants that are written to the attributes in the controller by the sequencer micro-processor in order to perform some function and/or put the controller into a defined state.

Writing to these constants required two 16-bit words to be written as a little-ended pairs to each even / odd constant address location. This is to maintain compatibility with MONSOON Orange programming practices.

There are 4096 16-bit pattern constant locations starting from the value specified in this attribute that allows a total of 2048 32-bit constants to be written to the pattern memory store.

Usage
Read / Write.

Address
0x1000 => 0x1FFF

Calibration
Units **Slope** 1.0 **Offset** 0.0

Limits
Maximum 65535.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes

Hardware

Notes
These constants are sequenced out of the sequencer micro-processor output bus in a timed manner and are written as a normal Wishbone bus transaction to any available attribute of the controller. Pattern constants are defined as being 16-bit or 32-bit values. 16-bit values contain the attribute address in the most significant 16-bit field and the value to be written to the attribute in the lower 16-bit field. 32-bit values contain just the attribute value and must be used with a valid ‘device address’ (LDA instruction) to define the attribute address.

More information

Attribute name **SeqPgmMem** **array size** 1024

Function
Defines the start address of the sequencer program store memory area.

Firmware module CFG **version** 2.20

Description
The sequencer micro-processor uses a 4-bit word size. The sequencer program consists of an assembled collection of these 4-bit codes with their associated operands. These codes are loaded to the micro-processor program store starting at this address. There are 1024 16-bit values that can be written. Data is written little-endian.
This protocol is to maintain compatibility with MONSOON Orange programming practices

Usage
Read / Write.

Address
0x4000 => 0x43FF

Calibration **Units** Value **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 65535.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes

Hardware

Notes

More information

Pixel Services Module (PIX) Attributes

The Pixel Services firmware is a Wishbone slave module connected to the FPGA internal Wishbone bus. The attributes of this module control the flow of pixel data from the front end (CDD or IR AFE(s)) to the Local Control Board (LCB) data multiplexor.

The WishBone Bus module address for the PIX Services module is 0x08.

Attribute name **PixResetCmd** array size 1

Function
Provides a local reset to the Pix firmware module

Firmware module PIX version 2.21

Description
Writing a value of 1.0 (true) to this attribute resets the internal functions of the Pixel Services firmware.

This action sets the default conditions as follows:
StreamModeEnable = 0.

Usage
Write only.

Address
0xFFFE

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
StreamModeEnable.

Hardware

Notes

More information

Attribute name **PixCodeId** array size 1

Function
Returns the PIX Module firmware revision level value

Firmware module PIX version 2.21

Description
Reading this attribute provides the firmware revision level of this module as a major revision level with two decimal places.
Major level revision codes are used to describe application levels (e.g. 1.xx indicates development code, 2.xx are CCD production code versions, 3.xx is IR camera production code, etc.).
Semi-major code changes (i.e. the first decimal) generally incorporate functional changes that require software (assimilate tool) to be used to extract new attribute values and/or incorporate new functionality (e.g. incorporation of a new image buffer scheme, etc.).
Minor revision levels are for bug fixes and/or enhancements without affecting functionality.

Usage
Read only.

Address
0xFFFF

Calibration
Units Revision **Slope** 100.0 **Offset** 0.0

Limits
Maximum 655.35 **Minimum** 0.0 **Default** 2.21

Associations
Attributes None.

Hardware None.

Notes

More information

Attribute name **PixModuleId** array size 1

Function
Returns the function code of the PIX module to confirm its presence.

Firmware module PIX version 2.21

Description
Reading this attribute enables any interrogating device to confirm the presence of this module at the given module select address. The constant assigned to the PIX identification attribute has the value 204.

Values between 100 and 199 represent MONSOON Orange hardware module identity codes.
Values between 200 and 299 represent MONSOON Torrent firmware module identity codes.

Usage
Read only.

Address
0xFFFE

Calibration
Units Ident **Slope** 1.0 **Offset** 0.0

Limits
Maximum 65535.0 **Minimum** 0.0 **Default** 204.0

Associations
Attributes
None.

Hardware
None.

Notes

More information

Attribute name **PixModInStatus** array size 1

Function
Returns the System status word as seen by the module

Firmware module PIX version 2.21

Description
The system status word is defined by the interconnect system of the Wishbone bus that interconnects all firmware modules internal to the FPGA. This status word is broadcast to each module and is used to convey state information concerning the configuration and functional state of the controller.

Usage
Read only.

Address
0xFFFD

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 0xffffffff **Minimum** 0.0 **Default** 0.0

Associations
Attributes
LCBModOutStatus, PSMModOutStatus, CFGModOutStatus, PIXModOutStatus, AFEModOutStatus, ClkModOutStatus.

Hardware
See the Wiki page link given below.

Notes

More information
See http://www.noao.edu/wiki/index.php/Firmware_Topics - Wishbone_system_status_signal_assignment

Attribute name **PixModOutStatus** array size 1

Function
Provides local status information on the PIX module state

Firmware module PIX version 2.21

Description
Reading this attribute provides additional state information internal to the LCB module. In this firmware revision the only significant bit is the LSB that indicates the state of the image buffer memory DDR2 dynamic ram controller. When bit 0 indicates true the memory controller has been successfully initialized.

Bit	Significance	Bit	Significance
0	MemCntrlInitDone		

Usage
Read only.

Address
0xFFFC

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 0xffffffff **Minimum** 0.0 **Default** 0.0

Associations
Attributes None.

Hardware **LCB:MEM_PWR_EN, LCB:U37**

Notes

More information

Attribute name **StreamModeEnable** array size 1

Function
Enables direct transfer of pixel data to the PAN without local image buffering.

Firmware module PIX version 2.21

Description
This attribute is set true by default. When true, the pixel data stream generated by the AFE hardware and acquired by the AFE firmware is transferred to the destination communication ports without using the image buffer memory in the DHE. The destination ports are determined by the **SCDataDestination** and **QLDataDestination** attributes.

Usage
Read / Write.

Address
0x0102

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 1.0

Associations
Attributes
SCDataDestination, QLDataDestination, EmbedSyncEnable, PackPixelMode, SCDataPrecision, QLDataPrecision.

Hardware

Notes

More information

Attribute name **EmbedSyncEnable** array size 1

Function
Enables image frame and line markers to be embedded into the pixel data

Firmware module PIX version 2.21

Description
If set true, and the sequencer code has been written to use the PULSE_FRAME and PULSE_LINE EFR register codes to delineate the pixel stream, the respective markers are inserted into PixelData(31) and PixelData(30) bit positions. This allows the PAN to detect the start of frame and start of each line within the frame to align the data and detect data drops (never happens ☺)

Usage
Read / Write.

Address
0x0101

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **PackPixelMode.**

Hardware None.

Notes
This option cannot be used with the **PackPixelMode** attribute set true.

More information

Attribute name **PackPixelMode** array size 1

Function

Enables the packing of two 16-bit pixel data values into one 32-bit word.

Firmware module PIX version 2.21

Description

Setting this attribute true enables the logic to pack two 16-bit pixel data values into one 32-bit word used to transmit the data to the PAN. This attribute only applies to data transported by the SFPDP (Systran) communication port.
The advantage of this is to reduce the bandwidth requirements of the communication port by a factor of 2.
When the **StreamModeEnable** attribute is set false this also reduces the time (latency) of the pixel transmission by half.
If 18-bit data is required (by appropriately setting the **SCDataPrecision, QLDataPrecision** attributes) then setting this attribute true truncates the pixel data to PixelData(15:0).

Usage Read / Write.

Address 0x0103

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 1.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes **StreamModeEnable**, **SCDataDestination, QLDataDestination, EmbedSyncEnable, SCDataPrecision, QLDataPrecision.**

Hardware .

Notes

More information

Attribute name **SCDataDestination** array size 1

Function
Determines to which communication port science data will be sent

Firmware module PIX version 2.21

Description
This attribute determines through which communications port to send the acquired raw pixel data stream i.e. the science data stream.
The bit significance for this attribute is:

Bit	Destination port
4	SFPDP (Systran) communication port
5	SYNC-OUT communication port
6	UART communication port
7	GIGe pixel stream communications port

Note that a value of 0 indicates No port i.e. bit bucket

Usage
Read / Write.

Address
0x0026

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 15.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **SCDataPrecision.**

Hardware None.

Notes

More information

Attribute name SCDataPrecision array size 1

Function
Establishes the format of the science pixel data to send to the PAN

Firmware module PIX version 2.21

Description
The CCD AFE variant acquires data from the video channels as 18-bit unsigned integers. This attribute allows you to optionally select a 16-bit value where the dynamic range of the raw pixel data word is not required. The value significance of this attribute is:

Value	Pixel data word format
0	16-bit from PixelData(15:0)
1	16-bit from Pixeldata(16:1)
2	16-bit from Pixeldata(17:2)
3	18-bit native data.

Usage
Read / Write.

Address
0x0025

Calibration Units Boolean Slope 1.0 Offset 0.0

Limits Maximum 3.0 Minimum 0.0 Default 0.0

Associations

Attributes **SCDataDestination.**

Hardware None.

Notes

More information

Attribute name **QLDataDestination** array size 1

Function
Determines to which communication port ‘quick look’ data will be sent

Firmware module PIX version 2.21

Description
This attribute determines through which communications port to send the processed ‘Quick Look’ pixel data stream i.e. image display data stream.
The bit significance for this attribute is:

Bit	Destination port
0	SFPDP (Systran) communication port
1	SYNC-OUT communication port
2	UART communication port
3	GIGe pixel stream communications port

Note that a value of 0 indicates No port i.e. bit bucket

Usage
Read / Write.

Address
0x0022

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 15.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes
QLDataPrecision, QLModeSel, QLRowBin, QLColumnBin.

Hardware
None.

Notes
Multiple destination communication ports can be specified in the attribute.

The preprocessing for the quick look display feature is currently disabled. QL data is the same as science data in this release of firmware.

More information

Attribute name **QLDataPrecision** array size 1

Function
Establishes the format of the quick look pixel data to send to the display device.

Firmware module PIX version 2.21

Description
The CCD AFE variant acquires data from the video channels as 18-bit unsigned integers. This attribute allows you to optionally select a 16-bit value where the dynamic range of the raw pixel data word is not required. The value significance of this attribute is:

Value	Pixel data word format
0	16-bit from PixelData(15:0)
1	16-bit from Pixeldata(16:1)
2	16-bit from Pixeldata(17:2)
3	18-bit native data.

Usage
Read / Write.

Address
0x0021

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 3.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes **QLDataDestination, QLModeSel, QLRowBin, QLColumnBin.**

Hardware None.

Notes
The preprocessing for the quick look display feature is currently disabled. QL data is the same as science data in this release of firmware.

More information

Attribute name **QLModeSel** **array size** 1

Function Selects which data stream to send to the PAN, Science or Quick Look

Firmware module PIX **version** 2.21

Description

Setting this attribute true selects the Quick Look data stream for transmission to the PAN.

When this attribute is false, the Science data stream is sent to the PAN.

Usage Read / Write.

Address 0x0020

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 1.0 **Minimum** 0.0 **Default** 1.0

Associations

Attributes **ScDataDestination, ScDataPrecision, QLDataDestination, QLDataPrecision, QLRowBin, QLColumnBin.**

Hardware

Notes The preprocessing for the quick look display feature is currently disabled. QL data is the same as science data in this release of firmware.

More information

Attribute name **QLRowBin** array size 1

Function
Sets the row binning factor for quick look display data

Firmware module PIX version 2.21

Description
This attribute determines the row binning factor applied to quick look data before transmitting the data to the display device. Essentially this allows the display image data size to be decimated to reduce transmission time. The value significance of this attribute is:

Value	Row binning factor
0	No Binning
1	2 x binning
2	4 x binning
3	8 x binning

Usage
Read / Write.

Address
0x0024

Calibration
Units Rows. **Slope** 1.0 **Offset** 0.0

Limits
Maximum 3.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
QLDataDestination, QLDataPrecision, QLModeSel, QLColumnBin.

Hardware
None.

Notes
The preprocessing for the quick look display feature is currently disabled. QL data is the same as science data in this release of firmware.

More information

Attribute name **QLColumnBin** array size 1

Function
Sets the column binning factor for quick look display data

Firmware module PIX version 2.21

Description
This attribute determines the column binning factor applied to quick look data before transmitting the data to the display device. Essentially this allows the display image data size to be decimated to reduce transmission time. The value significance of this attribute is:

Value	Row binning factor
4	No Binning
5	2 x binning
6	4 x binning
7	8 x binning

Usage
Read / Write.

Address
0x0023

Calibration
Units Rows. **Slope** 1.0 **Offset** 0.0

Limits
Maximum 3.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
QLDataDestination, QLDataPrecision, QLModeSel, QLRowBin.

Hardware
None.

Notes
The preprocessing for the quick look display feature is currently disabled. QL data is the same as science data in this release of firmware.

More information

Attribute name **AcqPxlCount** array size 1

Function
Displays the number of pixels acquired in the last image

Firmware module PIX version 2.21

Description
This read only attribute displays the number of pixels received by the Pixel Services module from the AFE Control module. This is normally the number of detector columns x number of detector rows.

The accumulated value is cleared automatically when the sequencer issues a PULSE FRAME command via the EFR register or it can be programmatically cleared using the **ClearStats** attribute.

Usage
Read only.

Address
0x0106

Calibration **Units** Pixels **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 4294967295.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **ClearStats.**

Hardware None.

Notes

More information

Attribute name **PanPxlCount** array size 1

Function
Displays the number of pixels sent to the PAN in the last image

Firmware module PIX version 2.21

Description
This read only attribute displays the number of pixels sent to the PAN by the Pixel Services.

The accumulated value is cleared automatically when the sequencer issues a PULSE FRAME command via the EFR register or it can be programmatically cleared using the **ClearStats** attribute.

Usage
Read only.

Address
0x0107

Calibration **Units** Pixels **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 4294967295.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes
ClearStats, PackPixelMode, QLRowBin, QLColumnBin.

Hardware
None.

Notes
If the **PackPixelMode** attribute is true, the number displayed here will be half the value of the **AcqPixCount** attribute.

The value of this attribute is unaffected by the **ScDataDestination** and **QLDataDestination** attributes.

More information

Attribute name **MaxPixelvalue** array size 1

Function
Displays the maximum pixel data value acquired in the last image

Firmware module PIX version 2.21

Description
This read only attribute displays the maximum value found in the last pixel image data stream.

The value is cleared automatically when the sequencer issues a PULSE FRAME command via the EFR register or it can be programmatically cleared using the **ClearStats** attribute.

Usage
Read only.

Address
0x0105

Calibration **Units** ADU **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 262143.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **ScDataPrecision, QLDataPrecision.**

Hardware None.

Notes

More information

Attribute name **MinPixelvalue** array size 1

Function
Displays the minimum pixel data value acquired in the last image

Firmware module PIX version 2.21

Description
This read only attribute displays the minimum value found in the last pixel image data stream.

The value is cleared automatically when the sequencer issues a PULSE FRAME command via the EFR register or it can be programmatically cleared using the **ClearStats** attribute.

Usage
Read only.

Address
0x0104

Calibration **Units** ADU **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 262143.0 **Minimum** 0.0 **Default** 262143.0

Associations
Attributes **ScDataPrecision, QLDataPrecision.**

Hardware None.

Notes

More information

Attribute name **ClearStats** **array size** 1

Function Clears the statistics counters

Firmware module PIX **version** 2.21

Description

Use this attribute to clear the results of the statics counters.

The values are also cleared when the sequencer issues a PULSE FRAME command via the EFR register.

Usage Write only.

Address 0x0108

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 1.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes **AcqPxlCount, PanPxlCount, MaxPixelvalue, MinPixelvalue.**

Hardware None.

Notes

More information

Attribute name **BlkReadFromBuffr** array size

Function
Initiates a block read from the pixel image buffer memory

Firmware module PIX version 2.21

Description
Setting this attribute true initiates a block read from the pixel image buffer memory. The parameters for reading should have been set in the **ReadBuffrOrigin**, **ReadBuffrLength**, and **ReadBuffrIncValue** attributes.

After this attribute is set true the Pixel Services module will emit a stream of pixel data from the memory to the PAN or Display device as selected by the **QLModeSel** attribute.

All normal processing modes (i.e. data precision, binning, etc.) are applied to the data stream.

Usage
Read / Write.

Address
0x001B

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 1.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes
ReadBuffrOrigin, **ReadBuffrLength**, **ReadBuffrIncValue, ScDataDestination, ScDataPrecision, QLDataDestination,QLDataPrecision,QLDataPrecision, QLModeSel, QLRowBin, QLColumnBin**

Hardware
None.

Notes
Reading this attribute returns the current status of the read process. Only the LSB of the word is valid and indicates, when true, that the Image buffer memory read operation is busy.

Image buffer functionality is untested in this version of the firmware.

More information

Attribute name **ReadBuffrOrigin** array size 1

Function

Sets the memory address of the origin of a block read from the image buffer memory.

Firmware module PIX version 2.21

Description

This attribute sets the base address from where the pixel data is read from during a block read operation.

Normally, image data is stored in the image buffer memory as a linear array from an address origin of zero.

The PULSE FRAME command, issued by the sequencer sets the write address pointer for the image buffer memory to zero.

Usage Read / Write.

Address 0x0018

Calibration **Units** Address **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 67108863.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes

BlkReadFromBuffr, ReadBuffrLength, **ReadBuffrIncValue, ScDataDestination, ScDataPrecision, QLDataDestination,QLDataPrecision,QLDataPrecision, QLModeSel, QLRowBin, QLColumnBin**

Hardware

None.

Notes Image buffer functionality is untested in this version of the firmware.

More information

Attribute name **ReadBuffrLength** array size 1

Function
Sets the required number of words to read from the image buffer memory during a block read operation.

Firmware module PIX version 2.21

Description
Set this attribute to the number of pixel data values that are required to be read during a block read operation.

The value is before any binning is applied.

Usage
Read / Write.

Address
0x0019

Calibration **Units** Pixels **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 67108863.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes
BlkReadFromBuffr, ReadBuffrOrigin, ReadBuffrIncValue, ScDataDestination, ScDataPrecision, QLDataDestination,QLDataPrecision,QLDataPrecision, QLModeSel, QLRowBin, QLColumnBin

Hardware
.

Notes

More information

Attribute name **ReadBuffrIncValue** **array size** 1

Function Sets the address increment value during block read operations from the image buffer memory.

Firmware module PIX **version** 2.21

Description

The address counter will be incremented after each pixel read by the value of this attribute. Setting this value to values greater than 1 will allow you to descramble individual amplifiers from the raw data image stored in the image buffer memory.

Usage Read / Write.

Address 0x001A

Calibration **Units** Skip **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 67108863.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes **BlkReadFromBuffr, ReadBuffrOrigin**, **ReadBuffrLength, ScDataDestination, ScDataPrecision, QLDataDestination,QLDataPrecision,QLDataPrecision, QLModeSel, QLRowBin, QLColumnBin**

Hardware None.

Notes

More information

Attribute name **BlkWrtToBuffr** array size 1

Function
Initiates a block write to the image buffer memory.

Firmware module PIX version 2.21

Description
Setting this attribute true initiates a block write to the pixel image buffer memory. The parameters for writing should have been set in the **WrtBuffrDataValue**, **WrtBuffrOrigin**, **WrtBuffrLength**, and **WrtBuffrIncValue** attributes.

After this attribute is set true the Pixel Services module will fill the image buffer memory with the constant in the **WrtBuffrDataValue** attribute**.**

Usage
Read / Write.

Address
0x0014

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 1.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **WrtBuffrDataValue**, **WrtBuffrOrigin**, **WrtBuffrLength**, **WrtBuffrIncValue**

Hardware None.

Notes
Image buffer functionality is untested in this version of the firmware.

More information

Attribute name **WrtBuffrDataValue** array size 1

Function
Sets the constant to write to the image buffer memory during a block write operation.

Firmware module PIX version 2.21

Description
This attribute is 32-bits wide but several values are special. The value significance is:

Value	Constant written to memory
0	Clear memory with zeros.
1	Write the write count to memory
2 – max	Write the value of the attribute to memory

Usage
Read / Write.

Address
0x0013

Calibration **Units** Value **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 2147483647.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **BlkWrtToBuffr, WrtBuffrOrigin**, **WrtBuffrLength**, **WrtBuffrIncValue**

Hardware .

Notes
Image buffer functionality is untested in this version of the firmware.

More information

Attribute name **WrtBuffrOrigin** **array size** 1

Function Sets the memory address of the origin of a block write to the image buffer memory.

Firmware module PIX **version** 2.21

Description

This attribute sets the base address from where the block write operation begins

Usage Read / Write.

Address 0x0010

Calibration **Units** Address **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 67108863.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes **BlkWrtToBuffr, WrtBuffrDataValue**, **WrtBuffrLength**, **WrtBuffrIncValue**

Hardware None.

Notes Image buffer functionality is untested in this version of the firmware.

More information

Attribute name **WrtBuffrLength** array size 1

Function
Sets the required number of words to write to the image buffer memory during a block write operation.

Firmware module PIX version 2.21

Description
Set this attribute to the number of pixel data values that are required to be written during a block read operation.

Usage
Read / Write.

Address
0x0011

Calibration
Units Words **Slope** 1.0 **Offset** 0.0

Limits
Maximum 67108863.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **BlkWrtToBuffr, WrtBuffrDataValue**, **WrtBuffrOrigin**, **WrtBuffrIncValue**

Hardware .

Notes
Image buffer functionality is untested in this version of the firmware.

More information

Attribute name **WrtBuffrIncValue** array size 1

Function
Sets the address increment value during a block write operation to the image buffer memory.

Firmware module PIX version 2.21

Description
The address counter will be incremented after each pixel writen by the value of this attribute.

Usage
Read / Write.

Address
0x0012

Calibration
Units Skip **Slope** 1.0 **Offset** 0.0

Limits
Maximum 67108863.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
BlkWrtToBuffr, WrtBuffrDataValue, **WrtBuffrOrigin**, **WrtBuffrLength**

Hardware
None.

Notes
Image buffer functionality is untested in this version of the firmware.

More information

AFE Control Module (AFE) Attributes

The Analog Front End (AFE) Control firmware is a Wishbone slave module connected to the FPGA internal Wishbone bus. The attributes of this module control the clocking, bias voltage generation, and pixel data acquisition functions of the controller.

The WishBone Bus module address for the AFE Control module is 0x10.

Attribute name **AfeResetCmd** array size 1

Function
Provides a local reset to the Pix firmware module

Firmware module AFE version 2.21

Description
Writing a value of 1.0 (true) to this attribute resets the internal functions of the AFE Control firmware.

This action sets the default conditions as follows:
TelScanInt = 1000, **TelScanCmd** = 0, **SimDatType** = 0, **ChanSrcSlct** = [1,2,3,4,5,6,7,8], **AfeInterfaceEnbl** = 3, **CdsPortConfigReg** = 1, **ClkPortConfigReg** = 1, **CdsChanSlctReg** = 255.

Usage
Write only.

Address
0xFFFE

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 1.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes
TelScanInt, **TelScanCmd**, **SimDatType**, **ChanSrcSlct**], **AfeInterfaceEnbl**, **CdsPortConfigReg**, **ClkPortConfigReg**, **CdsChanSlctReg**.

Hardware
LCB:U21, LCB:U59, LCB:XA1J1:B3-B4, LCB:XA2J1:B3-B4, LCB:AFE_CLKBIASIO83, LCB:AFE_CLKBIASIO84, AFE:P1:83, AFE:AFE_CTRL_ENABLE.

Notes

More information

Attribute name **AfeCodeId** array size 1

Function
Returns the AFE Module firmware revision level value

Firmware module AFE version 2.21

Description
Reading this attribute provides the firmware revision level of this module as a major revision level with two decimal places.
Major level revision codes are used to describe application levels (e.g. 1.xx indicates development code, 2.xx are CCD production code versions, 3.xx is IR camera production code, etc.).
Semi-major code changes (i.e. the first decimal) generally incorporate functional changes that require software (assimilate tool) to be used to extract new attribute values and/or incorporate new functionality (e.g. incorporation of a new image buffer scheme, etc.).
Minor revision levels are for bug fixes and/or enhancements without affecting functionality.

Usage
Read only.

Address
0xFFFF

Calibration
Units Revision **Slope** 100.0 **Offset** 0.0

Limits
Maximum 655.35 **Minimum** 0.0 **Default** 2.21

Associations
Attributes None.

Hardware None.

Notes

More information

Attribute name **AfeModuleId** array size 1

Function
Returns the function code of the AFE control module to confirm its presence.

Firmware module PIX version 2.21

Description
Reading this attribute enables any interrogating device to confirm the presence of this module at the given module select address. The constant assigned to the AFE identification attribute has the value 205.

Values between 100 and 199 represent MONSOON Orange hardware module identity codes.
Values between 200 and 299 represent MONSOON Torrent firmware module identity codes.

Usage
Read only.

Address
0xFFFE

Calibration
Units Ident **Slope** 1.0 **Offset** 0.0

Limits
Maximum 65535.0 **Minimum** 0.0 **Default** 205.0

Associations
Attributes
None.

Hardware
None.

Notes

More information

Attribute name **AfeModInStatus** array size 1

Function
Returns the System status word as seen by the module

Firmware module AFE version 2.21

Description
The system status word is defined by the interconnect system of the Wishbone bus that interconnects all firmware modules internal to the FPGA. This status word is broadcast to each module and is used to convey state information concerning the configuration and functional state of the controller.

Usage
Read only.

Address
0xFFFD

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 0xffffffff **Minimum** 0.0 **Default** 0.0

Associations
Attributes
LCBModOutStatus, PSMModOutStatus, CFGModOutStatus, PIXModOutStatus, AFEModOutStatus, ClkModOutStatus.

Hardware
See the Wiki page link given below.

Notes

More information
See http://www.noao.edu/wiki/index.php/Firmware_Topics - Wishbone_system_status_signal_assignment

Attribute name **AfeModOutStatus** array size 1

Function
Provides local status information on the AFE module state

Firmware module AFE version 2.21

Description
Reading this attribute provides additional state information internal to the AFE module.The bit significance of the status word is:

Bit	Significance	Bit	Significance
0	AFE Test Point refresh active(*)	1	AFE DAC refresh active(*)
4	Test Point command Fifo empty	5	DAC command fifo empty
8	Telemetry Scan trigger active	9	TP & Dac refresh request active

(*) This occurs as part of the AFE power up process to re-establish TP and DAC registers on the AFE board.

Usage Read only.

Address 0xFFFC

Calibration Units Boolean Slope 1.0 Offset 0.0

Limits Maximum 0xffffffff Minimum 0.0 Default 0.0

Associations
Attributes **PwrUpAfeSupplies**

Hardware

Notes

More information

Attribute name **TelScanCmd** array size 1

Function
Initiates a telemetry read cycle for the selected channel on the AFE board

Firmware module AFE version 2.21

Description
The AFE telemetry system can be manually triggered by setting the appropriate value to this attribute. This is only allowed if automatic (periodic) scanning is disabled by setting the **TelScanInt** attribute to 0. The bit significance of the value set to this attribute is:

Bit	Telemetry channel	Bit	Telemetry channel
0	Clock and Bias voltage telemetry	1	Reference voltage telemetry
2	Clock DAC low voltage telemetry	3	Clock DAC high voltage telemetry
4	Bias DAC monitor telemetry	5	Video Offset DAC monitor telemetry

The telemetry read scan is completed for all AFE boards that are present and the results written to the respective attribute registers.

Usage
Read / Write.

Address
0xF003

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 63.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes

TelScanInt, Afe1LvBiasTel, Afe1HvBiasTel, Afe1ClkTel, Afe1RefTel, Afe1AuxTelReg, Afe2LvBiasTel, Afe2HvBiasTel, Afe2ClkTel, Afe2RefTel, Afe2AuxTelReg

Hardware

LCB:AFE_CLKBIASIO57-58-59-61-62-63, AFE:U41, AFE:/TELMON0_SYNC, AFE:/TELMON1_SYNC, AFE:/TELADC0_SYNC, AFE:/TELMUX0_SYNC, AFE:TELMUX1_SYNC, AFE:TELADC_DIN, AFE:U141, AFE:TEL_SCLK, AFE:TELADC_DOUT, AFE:/TELMON_DOUT0, AFE:/TELMON_DOUT1. AFE:AFE_DATA14-16-17, LCB:AFE_PWRDATA14-16-17-32-34-35.

Notes
This attribute can only be set true when the periodic scan is switched off i.e. **TelScanInt** = 0.

The attribute is cleared as soon as the firmware begins the telemetry scan process so reading this attribute back and finding it zero indicates acceptance of the command.

Automatic or periodic telemetry scans only read the Clock and Bias voltage telemetry and Reference voltage telemetry channels.

More information

Attribute name **TelScanInt** array size 1

Function
Sets the period between the automatic or periodic AFE telemetry read scans.

Firmware module AFE version 2.21

Description
Under normal use, the telemetry channels are scanned in a periodic manner to update the relevant attributes. In this way the PAN can access the telemetry values without the delay associated with reading the actual value. The latency of these values is thus set by the period set to this attribute. During readout the periodic telemetry scans can be disabled by the sequencer to reduce possible interference. The sequencer uses the READOUT_BUSY and READOUT_IDLE command codes issued to the EFR register to achieve this.

Setting the attribute value to zero disables periodic telemetry scans.

Usage
Read / Write.

Address
0xF004

Calibration
Units milliSec. **Slope** 1.0 **Offset** 0.0

Limits
Maximum 4095.0 **Minimum** 0.0 **Default** 1000.0

Associations

Attributes

Afe1LvBiasTel, Afe1HvBiasTel, Afe1ClkTel, Afe1RefTel, Afe2LvBiasTel, Afe2HvBiasTel, Afe2ClkTel, Afe2RefTel.

Hardware

LCB:AFE_CLKBIASIO57-58-59-61-62-63, AFE:U41, AFE:/TELMON0_SYNC, AFE:/TELMON1_SYNC, AFE:/TELADC0_SYNC, AFE:/TELMUX0_SYNC, AFE:TELMUX1_SYNC, AFE:TELADC_DIN, AFE:U141, AFE:TEL_SCLK, AFE:TELADC_DOUT, AFE:/TELMON_DOUT0, AFE:/TELMON_DOUT1. AFE:AFE_DATA14-16-17, LCB:AFE_PWRDATA14-16-17-32-34-35.

Notes

More information

Attribute name **AfeInterfaceEnbl** array size 1

Function
Enables the electrical interface to the AFE boards.

Firmware module AFE version 2.21

Description
A scan of the hardware configuration is performed after the FPGA boot operation has completed. A scan can also be initiated by using the **DetectI2CBus** attribute. After the detection of the hardware this attribute is set to indicate which AFE boards are present. Bit 0 indicates the detection of AFE1 and bit 1 indicates the detection of AFE2. At any time after the detection process this attribute can be modified to physically turn off the electrical interface to an AFE board by setting the appropriate bit to zero. This action also removes power from the affected AFE board. This could be used to conserve power dissipation when the second AFE board is not required for normal operation. Reading this attribute after boot will indicate the position of the detected AFE boards in the DHE.

Usage Read / Write.

Address 0xF000

Calibration Units Boolean Slope 1.0 Offset 0.0

Limits Maximum 3.0 Minimum 0.0 Default 3.0

Associations

Attributes **DetectI2CBus.**

Hardware **LCB:U21, LCB:U59, LCB:XA1J1:B3-B4, LCB:XA2J1:B3-B4, LCB:AFE_CLKBIASIO83, LCB:AFE_CLKBIASIO84, AFE:P1:83, AFE:AFE_CTRL_ENABLE + others.**

Notes

More information

Attribute name **BiasEnbl** array size 1

Function
Connects the bias voltage groups to the detector via the isolation switches on the AFE

Firmware module AFE version 2.21

Description
The bias voltages are connected to the TSM (and to any detector that is connected to the TSM) when this attribute is set true. Each bit of this attribute controls a group of four bias potentials. The bit significance for this attribute is:

Bit	Bias group	Bit	Bias group
0	AFE1 Low voltage biases 0:3	1	AFE1 low voltage biases 4:7
2	AFE1 High voltage biases 0:3	3	AFE1 High voltage biases 4:7
4	AFE2 Low voltage biases 0:3	5	AFE2 low voltage biases 4:7
6	AFE2 High voltage biases 0:3	7	AFE2 High voltage biases 4:7

Usage Read / Write.

Address 0xF005

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 255.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes **PwrUpAfeSupplies, WatchDogEnable.**

Hardware **AFE:U46, AFE:U47, AFE:U53,AFE:U54, AFE:U141, AFE:U142**

Notes
This attribute is set false when the **PwrUpAfeSupplies** attribute is set false, or when the **WatchDogEnable** attribute is set false, or when the watchdog triggers a reboot due to the loss of the clock signal.

More information

Attribute name **ClkEnbl** array size 1

Function
Connects the clock voltage groups to the detector via the isolation switches on the AFE

Firmware module AFE version 2.21

Description
The clock voltages are connected to the TSM (and to any detector that is connected to the TSM) when this attribute is set true. Each bit of this attribute controls a group of four clock generators. The bit significance for this attribute is:

Bit	Bias group	Bit	Bias group
0	AFE1 Clock group 0:3	1	AFE1 Clock group 4:7
2	AFE1 Clock group 8:11	3	AFE1 Clock group 12:15
4	AFE2 Clock group 0:3	5	AFE2 Clock group 4:7
6	AFE2 Clock group 8:11	7	AFE2 Clock group 12:15

Usage
Read / Write.

Address
0xF008

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 255.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes
PwrUpAfeSupplies, WatchDogEnable.

Hardware
LCB:AFE_CLKBIAS19:22, AFE:U8, AFE:U9, AFE:U10, AFE:U12, AFE:146, AFE:U147.

Notes
This attribute is set false when the **PwrUpAfeSupplies** attribute is set false, or when the **WatchDogEnable** attribute is set false, or when the watchdog triggers a reboot due to the loss of the clock signal.

More information

Attribute name **ClkPortConfigReg** array size 1

Function
Configures the mode of the functional control of the clock state attribute

Firmware module AFE version 2.21

Description
This attribute determines the way in which data set to the **AfeClkStateReg** attribute is interpreted. The mode values set to the **ClkPortConfigReg** attribute facilitate the writing and maintenance of the sequencer code. The value significance of this attribute is:

Value	Mode
0	AFE1 and AFE2 independent. Write 32-bit data to **AfeClkStateReg.** **AfeClkStateReg**(31:16) => AFE2, **AfeClkStateReg**(15:0) => AFE1
1	AFE2 slaved to AFE1. Write 16-bit data to **AfeClkStateReg.** **AfeClkStateReg**(15:0) => AFE2, **AfeClkStateReg**(15:0) => AFE1
2	AFE1 slaved to AFE2. Write 32-bit data to **AfeClkStateReg.** **AfeClkStateReg**(31:16) => AFE2, **AfeClkStateReg**(31:16) => AFE1

Usage Read / Write.

Address 0x3000

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 2.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **AfeClkStateReg.**

Hardware None.

Notes

More information

Attribute name **AfeClkStateReg** array size 1

Function
Sets the clock pattern state to the detector

Firmware module AFE version 2.21

Description
Data values written to this attribute set the clock pattern state directly. The sequencer constructs the sequence of clock states at the detector by stuffing values into this attribute at programmed intervals. The word written to this attribute has different number of significant bits depending on the value of the **ClkPortConfigReg** attribute. When the **ClkPortConfigReg** is non-zero, the clock words are written simultaneously to AFE1 and AFE2 boards. When the **ClkPortConfigReg** attribute is set to zero, there is a 12ns delay between writing the independent clock values to AFE1 board and AFE2 board.

Usage
Read / Write.

Address
0x3002

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 4294967295.0 **Minimum** 0.0 **Default** 1.0

Associations
Attributes
ClkPortConfigReg, ClkEnbl.

Hardware
LCB:AFE_CLKBIASIO00:15, LCB:AFECLKBIASIO82:83, LCB:XA1J1, LCB:XA2J1, AFE:U63, AFE:U149,

Notes

More information

Attribute name **CdsPortConfigReg** array size 1

Function
Configures the mode for the selection of active Correlated Double Sampler (CDS) circuits.

Firmware module AFE version 2.21

Description
This attribute allows you to set groups of the AFE1 and AFE2 CDS circuits to be enabled and written to as copied versions of the **CdsChanSlctReg** and **CdsStateReg** attributes. The mode values set to the **CdsPortConfigReg** attribute facilitate the writing and maintenance of the sequencer code. The value significance of this attribute is:

Value	Mode
0	AFE1 and AFE2 CDS are independent. The value of the **CdsChanSlctReg** attribute determines the active CDS circuits.
1	AFE2 active channels slaved to AFE1 active channels. Bits 3:0 of the **CdsChanSlctReg** attribute determines the AFE1 and AFE2 active CDS circuits
2	AFE1 active channels slaved to AFE2 active channels. Bits 7:4 of the **CdsChanSlctReg** attribute determines the AFE1 and AFE2 active CDS circuits
3	All AFE CDS channels selected. **CdsChanSlctReg** attribute has no effect.

Usage
Read / Write.

Address
0x2000

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 3.0 **Minimum** 0.0 **Default** 1.0

Associations
Attributes **CdsChanSlctReg, CdsStateReg.**

Hardware

Notes

More information

Attribute name **CdsChanSlctReg** array size 1

Function
Sets the individual CDS channel enables for hardware

Firmware module AFE version 2.21

Description
Each bit in this attribute controls the enable to allow writing state information to the CDS hardware. When a channel bit is set false in this attribute, writing fresh data to the **CdsStateReg** attribute will not affect the CDS state of the channel. The bit significance for this attribute is:

Bit	Channel	Bit	Channel
0	AFE1 CDS channel 1	1	AFE1 CDS channel 2
2	AFE1 CDS channel 3	3	AFE1 CDS channel 4
4	AFE2 CDS channel 1	5	AFE2 CDS channel 2
6	AFE2 CDS channel 3	7	AFE2 CDS channel 4

Usage
Read / Write.

Address
0x2001

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 255.0 **Minimum** 0.0 **Default** 255.0

Associations

Attributes **CdsStateReg, CdsPortConfigReg.**

Hardware **LCB:PWRDATAIO44:47-52:55, AFE:/AFE_CHANSLCT0:3, AFE:U102, AFE:U117**

Notes
The **CdsPortConfigReg** attribute defines the **CdsChanSlctReg** data bits (i.e. 7:0, 3:0, 7:4) that are used to select the active CDS channels when a value is written to the **CdsStateReg** attribute.

More information

Attribute name **CdsStateReg** array size 1

Function
Sets the CDS pattern state to the video processor hardware on the AFE

Firmware module AFE version 2.21

Description
This attribute determines the state that is set to the AFE video processing hardware that have their channels enabled for writing (see the **CdsChanSlctReg** attribute). The individual bit significance for this attribute is:

Bit	Video processor state
0	Command to Convert (CDS_CNVRTST) – Initiates ADC conversion
1	Invert video signal (CDS_INV) – Integrate on video portion of sig.
2	Non-invert video signal (CDS_NONINV) – Integrate on reset portion of sig.
3	Integrate (CDS_INTEGRATE) – Allows the integrator to function.
4	DC Restore (CDS_DCRESTORE) – Clamps AC coupled input to GND.
5	Reset Integrator (CDS_RESET) – Resets the integrator output to zero.

Usage
Read / Write.

Address
0x2002

Calibration Units Boolean Slope 1.0 Offset 0.0

Limits Maximum 63.0 Minimum 0.0 Default 54.0

Associations

Attributes
CdsChanSlctReg, CdsPortConfigReg.

Hardware
LCB:AFE_PWRDATAIO36:43, LCB:AFE_PWRDATAIO72:73, AFE:U63, AFE_U107, AFE:U102, AFE:U117.

Notes
Note that the **CDS_CNVRTST** signal is a 25ns pulse, not a level.

The value of this attribute is written to the active channels defined by the **CdsPortConfigReg** and **CdsChanSlctReg** attributes.

More information

Attribute name ccdSeqPatMem array size 64

Function
Code store address for the CDS micro-sequencer.

Firmware module AFE version 2.21

Description
The address of this attribute is the start of a 64 x 16-bit word memory that holds the state code for the CDS micro-sequencer. This sequencer is used to offload the pattern generation for the CDS circuitry from the main sequencer processor in the CFG module. Each word of the micro-sequencer state code contains an operand field and a time delay field. The bit fields of each word are:

Bits	Purpose
15:8	Time delay field. Produces a delay until the next word is executed. The delay is in units of the DClk / 2 (i.e. 80MHz / 2 = 40Mhz = 25ns)
7:0	The operand field. The bit significance is that of the **CdsStateReg** Attribute.

Usage
Read / Write.

Address
0x2040 => 0x207F

Calibration Units Boolean Slope 1.0 Offset 0.0

Limits Maximum 65535 Minimum 0.0 Default 0.0

Associations

Attributes **CdsStateReg, CcdSeqTrig, CdsChanSlctReg, CdsPortConfigReg.**

Hardware None.

Notes

More information

Attribute name **CcdSeqTrig** array size 1

Function
Initiates the CDS micro-sequencer function.

Firmware module AFE version 2.21

Description
Use this attribute to trigger a sequence of patterns to control the CDS circuitry on the AFE boards. Writing a appropriate value to this attribute starts the micro-sequencer at the address vector contained in the attribute value bits (5:0). The complete significance of the attribute value is:

Bits	Significance
23:16	CDS Channel select. One bit for each CDS video channel. See the description for the **CdsChanSlctReg** attribute.
14:8	Sequence run length. The number of patterns to issue to the CDS Circuits.
5:0	Start address in micro-sequencer pattern memory to begin the sequence.

Usage
Read / Write.

Address
0x2003

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 16777215.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes

Hardware
None.

Notes
Note that the micro-sequencer supports the use of the **CdsPortConfigReg** attribute. Bits 23:16 of the **CcdSeqTrig** attribute override the **CdsChanSlctReg** attribute value.

Sequencer code address pointer will wrap so specifying a run length value 40 steps (0x28) starting at address 32 (0x20) will send the operands from 0x20 => 0x3F _and_ 0x00 => 0x08.

More information

Attribute name ChanSrcSlct array size 8

Function

Selects the physical video channels to be acquired by the DHE and the order in which they are to be sent to the PAN.

Firmware module AFE version 2.21

Description

Each of the eight ChanSrcSlct attributes define an available acquisition channel. Setting individual physical channel numbers to these attributes allows you to specify which video acquisition circuits are selected for acquisition. The legal values for these attributes and the significance is:

Value	Acquired channel	Value	Acquired channel
0	Disabled – no data acquired	1	Acquire from AFE1, chan. 1
2	Acquire from AFE1, chan. 2	3	Acquire from AFE1, chan. 3
4	Acquire from AFE1, chan. 4	5	Acquire from AFE2, chan. 1
6	Acquire from AFE2, chan. 2	7	Acquire from AFE2, chan. 3
8	Acquire from AFE2, chan. 4	9	Acquire chan. number idents.
10	Acquire simulated data.	11=>15	Acquire but pixel data = 0

Usage

Read / Write.

Address

0x1010 => 0x1017

Calibration Units Boolean Slope 1.0 Offset 0.0

Limits Maximum 15.0 Minimum 0.0 Default [1,2,3,4,5,6,7,8]

Associations

Attributes **ActiveChannels, SimDatType.**

Hardware **AFE:DATA0:1:2:3, AFE:U100, AFE:P2:27:29:31:33, LCB:AFE_PWRDATAIO00:01:02:03:18:19:20:21.**

Notes

When a ChanSrcSlct attribute has the value 9, the returned pixel data values are fixed as the number of the acquisition channel i.e. setting ChanSrcSlct[6] to a value of 9 make channel 6 an active acquisition channel and will result in all pixel data for that channel having a value of 6.

When a ChanSrcSlct attribute has a value of 10, the pixel value will be a simulated value injected at the AFE ADC serial data stream interface in the firmware.

More information

Attribute name **ActiveChannels** array size 1

Function
Displays the number of active acquisition channels currently selected

Firmware module AFE version 2.21

Description
This read only attribute displays the number of active channels selected for acquisition. This value is determined by the **ChanSrcSlct** attributes.

Usage
Read only.

Address
0x1001

Calibration
Units Channels **Slope** 1.0 **Offset** 0.0

Limits
Maximum 8.0 **Minimum** 0.0 **Default** 8.0

Associations
Attributes **ChanSrcSlct.**

Hardware None.

Notes

More information

Attribute name **SimDatType** array size 1

Function
Established the type of simulated data when for channels simulating acquisition

Firmware module AFE version 2.21

Description
If a **ChanSrcSlct** attribute has a value of 10, this attribute determines what type of simulated pixel data is acquired by that channel. The value significance for this attribute is:

Value	Simulated data type.
0	Pixel data values of zero. Constant value.
1	Accumulated pixel count since boot.
2	Psuedo random numbers in LS 8-bits (not very good).
3	My special key word = 0x2B36A. Constant value.

Usage
Read / Write.

Address
0x1000

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 3.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **ChanSrcSlct.**

Hardware None.

Notes

More information

Attribute name **Afe1VidOffVal** array size 4

Function
Sets the pixel data offset value for AFE1 acquisition circuits

Firmware module AFE version 2.21

Description
These attributes allow offsetting the pixel data values by a stable amount to compensate for any DC offset in the video processing circuit.

Usage
Read / Write.

Address
0x4010

Calibration
Units Value **Slope** 1.0 **Offset** 0.0

Limits
Maximum 4095.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
AfeRawPixData.

Hardware
LCB:AFE_CLKBIASIO48:50:54:77, LCB:XA1J1, LCB:XA2J1, AFE:U41, AFE:U141, AFE:/DAC_SYNC1, AFE:DAC_SCLK, AFE:DAC_SDIN, AFE:U92, AFE:DAC1_VOUT00:03.

Notes
The electrical offset is bipolar. Values between 0 and 2047 add a negative offset, values between 2049 and 4095 add a positive offset to the pixel data values. A value of 2048 is nominally zero offset.

A normal value, for N-Channel operation is around 2080.

Note that these attributes do not affect the value of simulated pixel data.

More information

Attribute name **Afe2VidOffVal** **array size** 4

Function Sets the pixel data offset value for AFE2 acquisition circuits

Firmware module AFE **version** 2.21

Description

These attributes allow offsetting the pixel data values by a stable amount to compensate for any DC offset in the video processing circuit.

Usage Read / Write.

Address 0x 4050

Calibration **Units** Value **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 4095.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes **AfeRawPixData.**

Hardware **LCB:AFE_CLKBIASIO48:50:54:77, LCB:XA1J1, LCB:XA2J1, AFE:U41, AFE:U141, AFE:/DAC_SYNC1, AFE:DAC_SCLK, AFE:DAC_SDIN, AFE:U92, AFE:DAC1_VOUT00:03.**

Notes

The electrical offset is bipolar. Values between 0 and 2047 add a negative offset, values between 2049 and 4095 add a positive offset to the pixel data values. A value of 2048 is nominally zero offset.

A normal value, for N-Channel operation is around 2080.

Note that these attributes do not affect the value of simulated pixel data.

More information

Attribute name **AfeRawPixData** **array size** 8

Function Displays the most recent acquired pixel data value from the video processing circuits i.e. this is the raw ADC conversion result.

Firmware module AFE **version** 2.21

Description

These attributes correspond to the raw ADC values acquired on the last conversion trigger (CTC). They are mainly used for diagnostic purposes. They are 18-bit values. Addresses 0x1030 => 0x1033 correspond to AFE1 channels 1 to 4. Addresses 0x1034 => 0x1037 correspond to AFE2 channels 1 to 4.

Usage Read only.

Address 0x1030 => 0x1037

Calibration **Units** ADU **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 262143.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes **Afe1VidOffVal, Afe2VidOffVal, CdsStateReg.**

Hardware None.

Notes

More information

Attribute name **Afe1ClkLoVal** array size 16

Function
Sets the voltage for the AFE1 associated clock channel when the clock is set to a low state

Firmware module AFE version 2.21

Description
These sixteen attributes establish the voltage to set to the detector when the clock is in the Low state. These attributes control the clock voltages on the AFE1 board. The attribute association is linear i.e. lowest address corresponds to the clock[0] channel, the highest address corresponds to the clock[15] channel

The clock state is set by the **AfeClkStateReg** attribute.

Usage
Read / Write.

Address
0x4020 => 0x402F

Calibration
Units Volts **Slope** 114.65 **Offset** 2048.0

Limits
Maximum 16.9 **Minimum** -16.9 **Default** 0.0

Associations
Attributes
Afe1ClkTel, AfeClkStateReg.

Hardware
. LCB:AFE_CLKBIASIO48:51:54:77, LCB:XA1J1, LCB:XA2J1, AFE:U41, AFE:U141, AFE:/DAC_SYNC2, AFE:DAC_SCLK, AFE:DAC_SDIN, AFE:U13, AFE:VCLKLO_00:15.

Notes

More information

Attribute name **Afe2ClkLoVal** array size 16

Function
Sets the voltage for the AFE2 associated clock channel when the clock is set to a low state

Firmware module AFE version 2.21

Description
These sixteen attributes establish the voltage to set to the detector when the clock is in the Low state. These attributes control the clock voltages on the AFE2 board. The attribute association is linear i.e. lowest address corresponds to the clock[0] channel, the highest address corresponds to the clock[15] channel

The clock state is set by the **AfeClkStateReg** attribute.

Usage
Read / Write.

Address
0x4060 => 0x406F

Calibration
Units Volts **Slope** 114.65 **Offset** 2048.0

Limits
Maximum 16.9 **Minimum** -16.9 **Default** 0.0

Associations
Attributes
Afe2ClkTel, AfeClkStateReg.

Hardware
. LCB:AFE_CLKBIASIO48:51:54:77, LCB:XA1J1, LCB:XA2J1, AFE:U41, AFE:U141, AFE:/DAC_SYNC2, AFE:DAC_SCLK, AFE:DAC_SDIN, AFE:U13, AFE:VCLKLO_00:15.

Notes

More information

Attribute name **Afe1ClkHiVal** array size 16

Function
Sets the voltage for the AFE1 associated clock channel when the clock is set to a high state

Firmware module AFE version 2.21

Description
These sixteen attributes establish the voltage to set to the detector when the clock is in the High state. These attributes control the clock voltages on the AFE1 board. The attribute association is linear i.e. lowest address corresponds to the clock[0] channel, the highest address corresponds to the clock[15] channel.

The clock state is set by the **AfeClkStateReg** attribute.

Usage
Read / Write.

Address
0x4030 => 0x403F

Calibration
Units Volts **Slope** 114.65 **Offset** 2048.0

Limits
Maximum 16.9 **Minimum** -16.9 **Default** 0.0

Associations
Attributes
Afe1ClkTel, AfeClkStateReg.

Hardware
. LCB:AFE_CLKBIASIO48:51:54:77, LCB:XA1J1, LCB:XA2J1, AFE:U41, AFE:U141, AFE:/DAC_SYNC3, AFE:DAC_SCLK, AFE:DAC_SDIN, AFE:U27, AFE:VCLKHI_00:15.

Notes

More information

Attribute name **Afe2ClkHiVal** array size 16

Function
Sets the voltage for the AFE2 associated clock channel when the clock is set to a high state

Firmware module AFE version 2.21

Description
These sixteen attributes establish the voltage to set to the detector when the clock is in the High state. These attributes control the clock voltages on the AFE2 board. The attribute association is linear i.e. lowest address corresponds to the clock[0] channel, the highest address corresponds to the clock[15] channel

The clock state is set by the **AfeClkStateReg** attribute.

Usage
Read / Write.

Address
0x4070 => 0x407F

Calibration
Units Volts **Slope** 114.65 **Offset** 2048.0

Limits
Maximum 16.9 **Minimum** -16.9 **Default** 0.0

Associations
Attributes
Afe2ClkTel, AfeClkStateReg.

Hardware
. LCB:AFE_CLKBIASIO48:51:54:77, LCB:XA1J1, LCB:XA2J1, AFE:U41, AFE:U141, AFE:/DAC_SYNC3, AFE:DAC_SCLK, AFE:DAC_SDIN, AFE:U27, AFE:VCLKHI_00:15.

Notes

More information

Attribute name **Afe1ClkTel** array size 16

Function
Returns the actual clock voltage present at the detector produced by the AFE1 board.

Firmware module AFE version 2.21

Description
These attributes return the voltage of the clock associated signal at the input side of the detector isolation switches i.e they represent the voltage at the output of the clock amplifier device.

Usage
Read only.

Address
0x8010 => 0x801F

Calibration
Units Volts **Slope** 100.97 **Offset** 1800.0

Limits
Maximum 18.0 **Minimum** -18.0 **Default** 0.0

Associations
Attributes
Afe1ClkLoVal, Afe1ClkHiVal, AfeClkStateReg.

Hardware
LCB:AFE_CLKBIASIO57-58-59-61-62-63, AFE:U41, AFE:/TELMON0_SYNC, AFE:/TELMON1_SYNC, AFE:/TELADC0_SYNC, AFE:/TELMUX0_SYNC, AFE:TELMUX1_SYNC, AFE:TELADC_DIN, AFE:U141, AFE:TEL_SCLK, AFE:TELADC_DOUT, AFE:/TELMON_DOUT0, AFE:/TELMON_DOUT1. AFE:AFE_DATA14-16-17, LCB:AFE_PWRDATA14-16-17-32-34-35.

Notes

More information

Attribute name **Afe2ClkTel** array size 16

Function
Returns the actual clock voltage present at the detector produced by the AFE2 board.

Firmware module AFE version 2.21

Description
These attributes return the voltage of the clock associated signal at the input side of the detector isolation switches i.e they represent the voltage at the output of the clock amplifier device.

Usage
Read only.

Address
0x8050 => 0x805F

Calibration
Units Volts **Slope** 100.97 **Offset** 1800.0

Limits
Maximum 18.0 **Minimum** -18.0 **Default** 0.0

Associations
Attributes
Afe2ClkLoVal, Afe2ClkHiVal, AfeClkStateReg.

Hardware
LCB:AFE_CLKBIASIO57-58-59-61-62-63, AFE:U41, AFE:/TELMON0_SYNC, AFE:/TELMON1_SYNC, AFE:/TELADC0_SYNC, AFE:/TELMUX0_SYNC, AFE:TELMUX1_SYNC, AFE:TELADC_DIN, AFE:U141, AFE:TEL_SCLK, AFE:TELADC_DOUT, AFE:/TELMON_DOUT0, AFE:/TELMON_DOUT1. AFE:AFE_DATA14-16-17, LCB:AFE_PWRDATA14-16-17-32-34-35.

Notes

More information

Attribute name **Afe1LvBiasVal** array size 8

Function
Establishes the voltage of the low voltage biases produced by the AFE1 board.

Firmware module AFE version 2.21

Description
These eight attributes establish the voltage applied to the detector by the low voltage bias generators of AFE1. The attribute association is linear i.e. lowest address corresponds to the LVBias[0] channel, the highest address corresponds to the LVBias[7] channel

Usage
Read / Write.

Address
0x4000 => 0x4007

Calibration
Units Volts **Slope** 113.96 **Offset** 2047.48

Limits
Maximum 16.9 **Minimum** -16.9 **Default** 0.0

Associations
Attributes **Afe1LvBiasTel.**

Hardware **LCB:AFE_CLKBIASIO48:49:53:77, LCB:XA1J1, LCB:XA2J1, AFE:U41, AFE:U141, AFE:/DAC_SYNC0, AFE:DAC_SCLK, AFE:DAC_SDIN, AFE:U48, AFE:DAC0_VOUT00:07.**

Notes

More information

Attribute name **Afe2LvBiasVal** array size 8

Function
Establishes the voltage of the low voltage biases produced by the AFE2 board.

Firmware module AFE version 2.21

Description
These eight attributes establish the voltage applied to the detector by the low voltage bias generators of AFE2. The attribute association is linear i.e. lowest address corresponds to the LVBias[0] channel, the highest address corresponds to the LVBias[7] channel

Usage
Read / Write.

Address
0x4040 => 0x4047

Calibration
Units Volts **Slope** 113.96 **Offset** 2047.48

Limits
Maximum 16.9 **Minimum** -16.9 **Default** 0.0

Associations
Attributes **Afe2LvBiasTel.**

Hardware **LCB:AFE_CLKBIASIO48:49:53:77, LCB:XA1J1, LCB:XA2J1, AFE:U41, AFE:U141, AFE:/DAC_SYNC0, AFE:DAC_SCLK, AFE:DAC_SDIN, AFE:U48, AFE:DAC0_VOUT00:07.**

Notes

More information

Attribute name **Afe1LvBiasTel** array size 8

Function
Returns the actual low voltage bias present at the detector produced by the AFE1 board.

Firmware module AFE version 2.21

Description
These attributes return the voltage of the low voltage bias signal at the input side of the detector isolation switches i.e they represent the voltage at the output of the bias amplifier device.

Usage
Read only.

Address
0x8000 => 0x8007

Calibration
Units Volts **Slope** 100.21 **Offset** 1792.63

Limits
Maximum 18.0 **Minimum** -18.0 **Default** 0.0

Associations
Attributes
Afe1LvBiasVal.

Hardware
LCB:AFE_CLKBIASIO57-58-59-61-62-63, AFE:U41, AFE:/TELMON0_SYNC, AFE:/TELMON1_SYNC, AFE:/TELADC0_SYNC, AFE:/TELMUX0_SYNC, AFE:TELMUX1_SYNC, AFE:TELADC_DIN, AFE:U141, AFE:TEL_SCLK, AFE:TELADC_DOUT, AFE:/TELMON_DOUT0, AFE:/TELMON_DOUT1. AFE:AFE_DATA14-16-17, LCB:AFE_PWRDATA14-16-17-32-34-35.

Notes

More information
See the description of the **TelScanCmd** attribute.

Attribute name **Afe2LvBiasTel** **array size** 8

Function Returns the actual low voltage bias present at the detector produced by the AFE2 board.

Firmware module AFE **version** 2.21

Description

These attributes return the voltage of the low voltage bias signal at the input side of the detector isolation switches i.e they represent the voltage at the output of the bias amplifier device.

Usage Read only.

Address 0x8040 => 0x8047

Calibration **Units** Volts **Slope** 100.21 **Offset** 1792.63

Limits **Maximum** 18.0 **Minimum** -18.0 **Default** 0.0

Associations

Attributes **Afe2LvBiasVal.**

Hardware **LCB:AFE_CLKBIASIO57-58-59-61-62-63, AFE:U41, AFE:/TELMON0_SYNC, AFE:/TELMON1_SYNC, AFE:/TELADC0_SYNC, AFE:/TELMUX0_SYNC, AFE:TELMUX1_SYNC, AFE:TELADC_DIN, AFE:U141, AFE:TEL_SCLK, AFE:TELADC_DOUT, AFE:/TELMON_DOUT0, AFE:/TELMON_DOUT1. AFE:AFE_DATA14-16-17, LCB:AFE_PWRDATA14-16-17-32-34-35.**

Notes

More information

See the description of the **TelScanCmd** attribute.

Attribute name **Afe1HvBiasVal** array size 8

Function

Establishes the voltage of the High voltage biases produced by the AFE1 board.

Firmware module AFE version 2.21

Description

These eight attributes establish the voltage applied to the detector by the High voltage bias generators of AFE1. The attribute association is linear i.e. lowest address corresponds to the HvBias[0] channel, the highest address corresponds to the HvBias[7] channel.

The polarity of these biases are controlled by the **VhvPolaritySlct** attribute.

Usage

Read / Write.

Address

0x4008 => 0x400F

Calibration

Units Volts **Slope** 72.82 **Offset** 2047.78

Limits

Maximum 28.0 **Minimum** -28.0 **Default** 0.0

Associations

Attributes

Afe1HvBiasTel, VhvPolaritySlct.

Hardware

LCB:AFE_CLKBIASIO48:49:53:77, LCB:XA1J1, LCB:XA2J1, AFE:U41, AFE:U141, AFE:/DAC_SYNC0, AFE:DAC_SCLK, AFE:DAC_SDIN, AFE:U48, AFE:DAC0_VOUT08:15.

Notes

More information

Attribute name **Afe2HvBiasVal** array size 8

Function

Establishes the voltage of the High voltage biases produced by the AFE2 board.

Firmware module AFE version 2.21

Description

These eight attributes establish the voltage applied to the detector by the High voltage bias generators of AFE2. The attribute association is linear i.e. lowest address corresponds to the HvBias[0] channel, the highest address corresponds to the HvBias[7] channel

The polarity of these biases are controlled by the **VhvPolaritySlct** attribute.

Usage

Read / Write.

Address

0x4048 => 0x404F

Calibration

Units Volts **Slope** 72.82 **Offset** 2047.78

Limits

Maximum 28.0 **Minimum** -28.0 **Default** 0.0

Associations

Attributes

Afe2HvBiasTel, VhvPolaritySlct.

Hardware

LCB:AFE_CLKBIASIO48:49:53:77, LCB:XA1J1, LCB:XA2J1, AFE:U41, AFE:U141, AFE:/DAC_SYNC0, AFE:DAC_SCLK, AFE:DAC_SDIN, AFE:U48, AFE:DAC0_VOUT08:15.

Notes

More information

Attribute name **Afe1HvBiasTel** array size 8

Function
Returns the actual High voltage bias present at the detector produced by the AFE1 board.

Firmware module AFE version 2.21

Description
These attributes return the voltage of the High voltage bias signal at the input side of the detector isolation switches i.e they represent the voltage at the output of the bias amplifier device.

Usage
Read only.

Address
0x8008 => 0x800F

Calibration
Units Volts **Slope** 66.8 **Offset** 1880.45

Limits
Maximum 33.0 **Minimum** -28.0 **Default** 0.0

Associations
Attributes
Afe1HvBiasVal.

Hardware
LCB:AFE_CLKBIASIO57-58-59-61-62-63, AFE:U41, AFE:/TELMON0_SYNC, AFE:/TELMON1_SYNC, AFE:/TELADC0_SYNC, AFE:/TELMUX0_SYNC, AFE:TELMUX1_SYNC, AFE:TELADC_DIN, AFE:U141, AFE:TEL_SCLK, AFE:TELADC_DOUT, AFE:/TELMON_DOUT0, AFE:/TELMON_DOUT1. AFE:AFE_DATA14-16-17, LCB:AFE_PWRDATA14-16-17-32-34-35.

Notes

More information
See the description of the **TelScanCmd** attribute.

Attribute name **Afe2HvBiasTel** array size 8

Function
Returns the actual High voltage bias present at the detector produced by the AFE2 board.

Firmware module AFE version 2.21

Description
These attributes return the voltage of the High voltage bias signal at the input side of the detector isolation switches i.e they represent the voltage at the output of the bias amplifier device.

Usage
Read only.

Address
0x8048 => 0x804F

Calibration
Units Volts **Slope** 66.8 **Offset** 1880.45

Limits
Maximum 33.0 **Minimum** -28.0 **Default** 0.0

Associations
Attributes
Afe2HvBiasVal.

Hardware
LCB:AFE_CLKBIASIO57-58-59-61-62-63, AFE:U41, AFE:/TELMON0_SYNC, AFE:/TELMON1_SYNC, AFE:/TELADC0_SYNC, AFE:/TELMUX0_SYNC, AFE:TELMUX1_SYNC, AFE:TELADC_DIN, AFE:U141, AFE:TEL_SCLK, AFE:TELADC_DOUT, AFE:/TELMON_DOUT0, AFE:/TELMON_DOUT1. AFE:AFE_DATA14-16-17, LCB:AFE_PWRDATA14-16-17-32-34-35.

Notes

More information
See the description of the **TelScanCmd** attribute.

Attribute name **Afe1Vn50Tel** array size 1

Function
Returns the telemetry voltage corresponding to the AFE1 local -5v power supply.

Firmware module AFE version 2.21

Description
This is the analog negative supply voltage used for the video processor circuitry.

Usage
Read only.

Address
0x802A

Calibration
Units Volts **Slope** 204.14 **Offset** 3074.3

Limits
Maximum 5.0 **Minimum** -15.0 **Default** 0.0

Associations
Attributes
VanaPowerEnable, PwrUpAfeSupplies, Vana-Amps.

Hardware
See the description for the **TelScanCmd** attribute

Notes

More information
See the description of the **TelScanCmd** attribute

Attribute name **Afe2Vn50Tel** array size 1

Function
Returns the telemetry voltage corresponding to the AFE2 local -5v power supply.

Firmware module AFE version 2.21

Description
This is the analog negative supply voltage used for the video processor circuitry.

Usage
Read only.

Address
0x806A

Calibration **Units** Volts **Slope** 204.14 **Offset** 3074.3

Limits **Maximum** 5.0 **Minimum** -15.0 **Default** 0.0

Associations

Attributes
VanaPowerEnable, PwrUpAfeSupplies, Vana-Amps.

Hardware
See the description for the **TelScanCmd** attribute

Notes

More information
See the description of the **TelScanCmd** attribute

Attribute name **Afe1Vp50Tel** **array size** 1

Function Returns the telemetry voltage corresponding to the AFE1 local +5v power supply.

Firmware module AFE **version** 2.21

Description This is the analog positive supply voltage used for the interface logic circuitry and some analog functions.

Usage Read only.

Address 0x8027

Calibration **Units** Volts **Slope** 409.6 **Offset** 0.0

Limits **Maximum** 10.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes **VanaPowerEnable, PwrUpAfeSupplies, Vana+Amps.**

Hardware See the description for the **TelScanCmd** attribute

Notes

More information See the description of the **TelScanCmd** attribute

Attribute name **Afe2Vp50Tel** **array size** 1

Function Returns the telemetry voltage corresponding to the AFE2 local +5v power supply.

Firmware module AFE **version** 2.21

Description This is the analog positive supply voltage used for the interface logic circuitry and some analog functions.

Usage Read only.

Address 0x8067

Calibration **Units** Volts **Slope** 409.6 **Offset** 0.0

Limits **Maximum** 10.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes **VanaPowerEnable, PwrUpAfeSupplies, Vana+Amps.**

Hardware See the description for the **TelScanCmd** attribute

Notes

More information See the description of the **TelScanCmd** attribute

Attribute name **Afe1Vp55Tel** **array size** 1

Function Returns the telemetry voltage corresponding to the AFE1 local +5.5v power supply.

Firmware module AFE **version** 2.21

Description

This is the analog positive supply voltage used for the analog video processor, reference supplies, and DAC biasing circuitry.

Usage Read only.

Address 0x8028

Calibration **Units** Volts **Slope** 409.6 **Offset** 0.0

Limits **Maximum** 10.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes **VanaPowerEnable, PwrUpAfeSupplies, Vana+Amps.**

Hardware See the description for the **TelScanCmd** attribute

Notes

More information

See the description of the **TelScanCmd** attribute

Attribute name **Afe2Vp55Tel** **array size** 1

Function Returns the telemetry voltage corresponding to the AFE2 local +5.5v power supply.

Firmware module AFE **version** 2.21

Description This is the analog positive supply voltage used for the analog video processor, reference supplies, and DAC biasing circuitry.

Usage Read only.

Address 0x8068

Calibration **Units** Volts **Slope** 409.6 **Offset** 0.0

Limits **Maximum** 10.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes **VanaPowerEnable, PwrUpAfeSupplies, Vana+Amps.**

Hardware See the description for the **TelScanCmd** attribute

Notes

More information See the description of the **TelScanCmd** attribute

Attribute name **Afe1Vp33Tel** array size 1

Function
Returns the telemetry voltage corresponding to the AFE1 local +3.3 power supply.

Firmware module AFE version 2.21

Description
This is the digital positive supply voltage used for the board interface circuitry.

Usage
Read only.

Address
0x8026

Calibration
Units Volts **Slope** 819.2 **Offset** 0.0

Limits
Maximum 5.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes
VanaPowerEnable, PwrUpAfeSupplies, Vana+Amps.

Hardware
See the description for the **TelScanCmd** attribute

Notes

More information
See the description of the **TelScanCmd** attribute

Attribute name **Afe2Vp33Tel** **array size** 1

Function Returns the telemetry voltage corresponding to the AFE2 local +3.3v power supply.

Firmware module AFE **version** 2.21

Description

This is the digital positive supply voltage used for the board interface circuitry.

Usage Read only.

Address 0x8066

Calibration **Units** Volts **Slope** 819.2 **Offset** 0.0

Limits **Maximum** 5.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes **VanaPowerEnable, PwrUpAfeSupplies, Vana+Amps.**

Hardware See the description for the **TelScanCmd** attribute

Notes

More information

See the description of the **TelScanCmd** attribute

Attribute name **Afe1VpIfcTel** array size 1

Function
Returns the telemetry voltage corresponding to the AFE1⇔LCB interface power supply.

Firmware module AFE version 2.21

Description
This is the digital positive supply voltage used for the inter-board digital signals. It is derived from the AFE Vp33 supply.

Usage
Read only.

Address
0x8029

Calibration
Units Volts **Slope** 819.2 **Offset** 0.0

Limits
Maximum 5.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
VanaPowerEnable, PwrUpAfeSupplies, Vana+Amps.

Hardware
See the description for the **TelScanCmd** attribute

Notes

More information
See the description of the **TelScanCmd** attribute

Attribute name **Afe2VpIfcTel** array size 1

Function
Returns the telemetry voltage corresponding to the AFE2⇔LCB interface power supply.

Firmware module AFE version 2.21

Description
This is the digital positive supply voltage used for the inter-board digital signals. It is derived from the AFE Vp33 supply.

Usage
Read only.

Address
0x8069

Calibration
Units Volts **Slope** 819.2 **Offset** 0.0

Limits
Maximum 5.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes
VanaPowerEnable, PwrUpAfeSupplies, Vana+Amps.

Hardware
See the description for the **TelScanCmd** attribute

Notes

More information
See the description of the **TelScanCmd** attribute

Attribute name **Afe1Vp100Tel** **array size** 1

Function Returns the telemetry voltage corresponding to the AFE1 +10v analog power supply.

Firmware module AFE **version** 2.21

Description This is the analog positive supply voltage used for the video processor circuitry – In particular, the analog switching functions.

Usage Read only.

Address 0x8034

Calibration **Units** Volts **Slope** 204.14 **Offset** 0.0

Limits **Maximum** 20.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes **VanaPowerEnable, PwrUpAfeSupplies, Vana+Amps.**

Hardware See the description for the **TelScanCmd** attribute

Notes

More information See the description of the **TelScanCmd** attribute

Attribute name **Afe2Vp100Tel** **array size** 1

Function Returns the telemetry voltage corresponding to the AFE2 +10v analog power supply.

Firmware module AFE **version** 2.21

Description This is the analog positive supply voltage used for the video processor circuitry – In particular, the analog switching functions.

Usage Read only.

Address 0x8074

Calibration **Units** Volts **Slope** 204.14 **Offset** 0.0

Limits **Maximum** 20.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes **VanaPowerEnable, PwrUpAfeSupplies, Vana+Amps.**

Hardware See the description for the **TelScanCmd** attribute

Notes

More information See the description of the **TelScanCmd** attribute

Attribute name **Afe1Vn100Tel** **array size** 1

Function Returns the telemetry voltage corresponding to the AFE1 -10v analog power supply.

Firmware module AFE **version** 2.21

Description

This is the analog positive supply voltage used for the video processor circuitry – In particular, the analog switching functions.

Usage Read only.

Address 0x8035

Calibration **Units** Volts **Slope** 136.5 **Offset** 3412.5

Limits **Maximum** 5.0 **Minimum** -25.0 **Default** 0.0

Associations

Attributes **VanaPowerEnable, PwrUpAfeSupplies, Vana-Amps.**

Hardware See the description for the **TelScanCmd** attribute

Notes

More information

See the description of the **TelScanCmd** attribute

Attribute name **Afe2Vn100Tel** **array size** 1

Function Returns the telemetry voltage corresponding to the AFE2 -10v analog power supply.

Firmware module AFE **version** 2.21

Description

This is the analog positive supply voltage used for the video processor circuitry – In particular, the analog switching functions.

Usage Read only.

Address 0x8075

Calibration **Units** Volts **Slope** 136.5 **Offset** 3412.5

Limits **Maximum** 5.0 **Minimum** -25.0 **Default** 0.0

Associations

Attributes **VanaPowerEnable, PwrUpAfeSupplies, Vana-Amps.**

Hardware See the description for the **TelScanCmd** attribute

Notes

More information

See the description of the **TelScanCmd** attribute

Attribute name **Afe1TpClk1** array size 1

Function
Controls the multiplexor for the AFE test point JT3 pin 2.

Firmware module AFE version 2.21

Description
Set this attribute to view the clock waveforms on AFE1 JT3 pin 2. The clocks that can be selected are:

Value	Clock waveform
0	AFE1 CLK00
1	AFE1 CLK04
2	AFE1 CLK08
3	AFE1 CLK12

Usage
Read / Write.

Address
0x7000

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 3.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **AfeClkStateReg, Afe1ClkLoVal, Afe1ClkHiVal.**

Hardware .

Notes

More information

Attribute name **Afe2TpClk1** array size 1

Function
Controls the multiplexor for the AFE2 test point JT3 pin 2.

Firmware module AFE version 2.21

Description
Set this attribute to view the clock waveforms on AFE2 JT3 pin 2. The clocks that can be selected are:

Value	Clock waveform
0	AFE2 CLK00
1	AFE2 CLK04
2	AFE2 CLK08
3	AFE2 CLK12

Usage
Read / Write.

Address
0x7008

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 3.0 **Minimum** 0.0 **Default** 0.0

Associations

Attributes **AfeClkStateReg, Afe2ClkLoVal, Afe2ClkHiVal.**

Hardware .

Notes

More information

Attribute name **Afe1TpClk2** array size 1

Function
Controls the multiplexor for the AFE test point JT3 pin 4.

Firmware module AFE version 2.21

Description
Set this attribute to view the clock waveforms on AFE1 JT3 pin 4. The clocks that can be selected are:

Value	Clock waveform
0	AFE1 CLK01
1	AFE1 CLK05
2	AFE1 CLK09
3	AFE1 CLK13

Usage
Read / Write.

Address
0x7001

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 3.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **AfeClkStateReg, Afe1ClkLoVal, Afe1ClkHiVal.**

Hardware .

Notes

More information

Attribute name **Afe2TpClk2** array size 1

Function
Controls the multiplexor for the AFE2 test point JT3 pin 4.

Firmware module AFE version 2.21

Description
Set this attribute to view the clock waveforms on AFE2 JT3 pin 4. The clocks that can be selected are:

Value	Clock waveform
0	AFE2 CLK01
1	AFE2 CLK05
2	AFE2 CLK09
3	AFE2 CLK13

Usage
Read / Write.

Address
0x7009

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 3.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **AfeClkStateReg, Afe2ClkLoVal, Afe2ClkHiVal.**

Hardware .

Notes

More information

Attribute name **Afe1TpClk3** array size 1

Function
Controls the multiplexor for the AFE test point JT3 pin 6.

Firmware module AFE version 2.21

Description
Set this attribute to view the clock waveforms on AFE1 JT3 pin 6. The clocks that can be selected are:

Value	Clock waveform
0	AFE1 CLK02
1	AFE1 CLK06
2	AFE1 CLK10
3	AFE1 CLK14

Usage
Read / Write.

Address
0x7002

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 3.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **AfeClkStateReg, Afe1ClkLoVal, Afe1ClkHiVal.**

Hardware .

Notes

More information

Attribute name **Afe2TpClk3** array size 1

Function
Controls the multiplexor for the AFE2 test point JT3 pin 6.

Firmware module AFE version 2.21

Description
Set this attribute to view the clock waveforms on AFE2 JT3 pin 6. The clocks that can be selected are:

Value	Clock waveform
0	AFE2 CLK02
1	AFE2 CLK06
2	AFE2 CLK10
3	AFE2 CLK14

Usage
Read / Write.

Address
0x700A

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 3.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **AfeClkStateReg, Afe2ClkLoVal, Afe2ClkHiVal.**

Hardware .

Notes

More information

Attribute name **Afe1TpClk4** array size 1

Function
Controls the multiplexor for the AFE test point JT3 pin 8.

Firmware module AFE version 2.21

Description
Set this attribute to view the clock waveforms on AFE1 JT3 pin 8. The clocks that can be selected are:

Value	Clock waveform
0	AFE1 CLK03
1	AFE1 CLK07
2	AFE1 CLK11
3	AFE1 CLK15

Usage
Read / Write.

Address
0x7003

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 3.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **AfeClkStateReg, Afe1ClkLoVal, Afe1ClkHiVal.**

Hardware .

Notes

More information

Attribute name **Afe2TpClk4** array size 1

Function
Controls the multiplexor for the AFE2 test point JT3 pin 8.

Firmware module AFE version 2.21

Description
Set this attribute to view the clock waveforms on AFE2 JT3 pin 8. The clocks that can be selected are:

Value	Clock waveform
0	AFE2 CLK03
1	AFE2 CLK07
2	AFE2 CLK11
3	AFE2 CLK15

Usage
Read / Write.

Address
0x700B

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 3.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **AfeClkStateReg, Afe2ClkLoVal, Afe2ClkHiVal.**

Hardware .

Notes

More information

Attribute name **Afe1TpLvBias1** array size 1

Function
Controls the low voltage bias multiplexor for the AFE test point JT2 pin 2.

Firmware module AFE version 2.21

Description
Set this attribute to view the low voltage bias waveforms on AFE1 JT2 pin 2.
The low voltage biases that can be selected are:

Value	Bias waveform
0	AFE1 LvBias0
1	AFE1 LvBias2
2	AFE1 LvBias4
3	AFE1 LvBias6

Usage
Read / Write.

Address
0x7004

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 3.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **Afe1LvBiasVal.**

Hardware .

Notes

More information

Attribute name **Afe2TpLvBias1** array size 1

Function
Controls the low voltage bias multiplexor for the AFE2 test point JT2 pin 2.

Firmware module AFE version 2.21

Description
Set this attribute to view the low voltage bias waveforms on AFE2 JT2 pin 2.
The biases that can be selected are:

Value	Bias waveform
0	AFE2 LvBias0
1	AFE2 LvBias2
2	AFE2 LvBias4
3	AFE2 LvBias6

Usage
Read / Write.

Address
0x700C

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 3.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **Afe2LvBiasVal.**

Hardware

Notes

More information

Attribute name **Afe1TpLvBias2** array size 1

Function
Controls the low voltage bias multiplexor for the AFE test point JT2 pin 4.

Firmware module AFE version 2.21

Description
Set this attribute to view the low voltage bias waveforms on AFE1 JT2 pin 4.
The low voltage biases that can be selected are:

Value	Bias waveform
0	AFE1 LvBias1
1	AFE1 LvBias2
2	AFE1 LvBias5
3	AFE1 LvBias7

Usage
Read / Write.

Address
0x7005

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 3.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **Afe1LvBiasVal.**

Hardware .

Notes

More information

Attribute name **Afe2TpLvBias2** array size 1

Function
Controls the low voltage bias multiplexor for the AFE2 test point JT2 pin 4.

Firmware module AFE version 2.21

Description
Set this attribute to view the low voltage bias waveforms on AFE2 JT2 pin 4.
The biases that can be selected are:

Value	Bias waveform
0	AFE2 LvBias1
1	AFE2 LvBias3
2	AFE2 LvBias5
3	AFE2 LvBias7

Usage
Read / Write.

Address
0x700D

Calibration
Units Boolean **Slope** 1.0 **Offset** 0.0

Limits
Maximum 3.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **Afe2LvBiasVal.**

Hardware

Notes

More information

Attribute name **Afe1TpHvBias1** array size 1

Function
Controls the High voltage bias multiplexor for the AFE test point JT2 pin 6.

Firmware module AFE version 2.21

Description
Set this attribute to view the High voltage bias waveforms on AFE1 JT2 pin 6.
The High voltage biases that can be selected are:

Value	Bias waveform
4	AFE1 HvBias0
5	AFE1 HvBias2
6	AFE1 HvBias4
7	AFE1 HvBias6

Usage
Read / Write.

Address
0x7006

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 3.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **Afe1HvBiasVal, VhvPolaritySlct.**

Hardware .

Notes

More information

Attribute name **Afe2TpHvBias1** array size 1

Function
Controls the High voltage bias multiplexor for the AFE2 test point JT2 pin 6.

Firmware module AFE version 2.21

Description
Set this attribute to view the High voltage bias waveforms on AFE2 JT2 pin 6.
The biases that can be selected are:

Value	Bias waveform
0	AFE2 HvBias0
1	AFE2 HvBias2
2	AFE2 HvBias4
3	AFE2 HvBias6

Usage
Read / Write.

Address
0x700E

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 3.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **Afe2HvBiasVal, VhvPolaritySlct.**

Hardware

Notes

More information

Attribute name **Afe1TpHvBias2** array size 1

Function
Controls the High voltage bias multiplexor for the AFE test point JT2 pin 8.

Firmware module AFE version 2.21

Description
Set this attribute to view the High voltage bias waveforms on AFE1 JT2 pin 8.
The High voltage biases that can be selected are:

Value	Bias waveform
0	AFE1 HvBias1
1	AFE1 HvBias2
2	AFE1 HvBias5
3	AFE1 HvBias7

Usage
Read / Write.

Address
0x7007

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 3.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **Afe1HvBiasVal, VhvPolaritySlct.**

Hardware .

Notes

More information

Attribute name **Afe2TpHvBias2** array size 1

Function
Controls the High voltage bias multiplexor for the AFE2 test point JT2 pin 8.

Firmware module AFE version 2.21

Description
Set this attribute to view the High voltage bias waveforms on AFE2 JT2 pin 8.
The biases that can be selected are:

Value	Bias waveform
0	AFE2 HvBias1
1	AFE2 HvBias3
2	AFE2 HvBias5
3	AFE2 HvBias7

Usage
Read / Write.

Address
0x700F

Calibration **Units** Boolean **Slope** 1.0 **Offset** 0.0

Limits **Maximum** 3.0 **Minimum** 0.0 **Default** 0.0

Associations
Attributes **Afe2HvBiasVal, VhvPolaritySlct.**

Hardware

Notes

More information

System status word decoding

The system status word is generated by the Wishbone bus interconnect logic (Intercon). Each bus slave puts its module specific 8-bit status word on the individual 'SlaveDataOut' bus signals whenever the bus is unused by that slave ('SlaveStrobeIn'=low). The intercon latches the data from each slave and maps it to the 32-bit 'SlaveDataIn' bus, common to all slave interfaces during each unused Wishbone bus cycles. The status information is latched in the slave bus interface module and used control its function. This status transport method allows the individual modules to communicate with each other without overhead.

The PAN can read this common status word from every slave module by accessing the xxxModInStatus attribute at address 0xFFFD.

The mapping of the status bits is:

Bit	Signal	Origin	Used by	Significance when true
0	TempChanSlct(0)	PSM	CFG	1 of 8 decoder for the source of the DHE temperature stabilization servo feedback.
1	TempChanSlct(1)	PSM	CFG	
2	TempChanSlct(2)	PSM	CFG	
3	AFE1_Detected	CFG	PSM,AFE	AFE1 I2C bus detected. AFE1 is physically present
4	AFE2_Detected	CFG	PSM,AFE	AFE2 I2C bus detected. AFE1 is physically present
5	PackedPixels	PIX	LCB	Pack two 16-bit pixels into every PAN pix data word
6	Pixels16	PIX	LCB	Pixel data has been truncated to16-bit values
7	DheIsSlave	CFG	LCB,CLK	DHE is operating as a slave controller
8	StreamMode	PIX	AFE	Pix data to bypass the image buffer memory.
9:20	Not Used			
21	AFE1_Enabled	AFE	PSM	AFE1 is in use – supply power to it.
22	AFE2_Enabled	AFE	PSM	AFE2 is in use – supply power to it.
23	VhvPolarity	PSM	AFE	High voltage biases are positive potentials
24	AFEPowerIsOn	PSM	AFE	The power is on and stable to the AFE boards
25	ClocksAreLocked	CLK	PIX	The clock generator device has acquired lock
26	MemPwrEnabled	PSM	PIX	The image buffer memory is available
27	LineStart	CFG	AFE	Sequencer strobe – New line is next pixel
28	FrameStart	CFG	AFE	Sequencer strobe – New frame is next pixel
29	ReadoutInProgress	CFG	AFE	Sequencer strobe – Keep quiet, readout in progress
30	AsyncFlag	LCB	CFG	DHE is not synchronized to a PAN
31	ShutDownQuick	PSM	AFE	Everything is cocked up – Shutdown is in progress. Save what you can.

Firmware debug signals

Debug signal group selection

Use the **DbgSigSlct** attribute to bring sets of diagnostic signals out of the FPGA and onto **LCB:J4** (**LCB:CFG_DATA(0:7)**). These signals can be used to identify certain problems (buss congestion – look at system or auxiliary groups) and to provide triggers to observe hardware functions (power supply – look at sync clocks to identify switch mode regulator ripple, etc.).

The signals brought out to this port are multiplexed at the system level of firmware from 8-bit wide busses coming from each module. You can change the significance of these signals by editing the schematic at the module level and regenerating the boot loader files. For transitory occasions you might want to just program the FPGA directly while leaving the eeprom store code intact.

This table shows the signals available at each bit position for all legal values of the **DbgSigSlct** attribute.

	DbgSigSlct attribute value									
	0	1	2	3	4	5	6 & 7	8	9	10
Bit	Not used	LCB Control	PSM Services	CFG Services	PIX Services	AFE Control	Not used	CLK Services	System group	Auxiliary group
0		GIGe_PIXEL DATA(0)	V33_SYNC	SYNC_POWER	app_af_cmd(0)	DacCntrlDataRdy		ClkCntrlClk	WbSlaveAck(0)	WbSlaveStbIn(0)
1		GIGe_PIXEL DATA(1)	VANA_SYNC	SE_READY	app_af_wren	SerialClk(0)		ClkCntrlData	WbSlaveAck(1)	WbSlaveStbIn(1)
2		GIGe_PIXEL DATA(2)	VCB_SYNC	FrameStart	app_af_addr(2)	StrmData(0)		ClkCntrlSync	WbStatCycle	WbSlaveStbIn(2)
3		GIGeDataOutRdy	VHV_SYNC	LineStart	app_af_addr(1)	Strmdata(1)		ClkLoopLock	WbSlaveErr	WbSlaveStbIn(3)
4		GIGe_DVAL	LOGIC_SYNC	MstrWrtEn	app_wdf_wren	StrmFrameStart		ClkCntrlGoe	WbSlaveWrt	WbSlaveStbIn(4)
5		GIGe_LVAL	SEQ_SYNC_CLK	MstrSdaOut(2)	app_wdf_afull	StrmLineStart		ClkCntrlCs-n	WbSlaveCycle	WbSlaveStbIn(5)
6		GIGe_FVAL	RunServo	MstrSdaIn	app_af_afull	StrmDataRdy		BCLK_FEED	Mstr0Grant	WbSlaveStbIn(6)
7		GIGe_PIXEL_CLK	AFEPwrIsOn	MstrScl	MemDataClk	StrDataClk		DCLK_FEED	Mstr1Grant	WbSlaveStbIn(7)

Debug trigger selection

Use the **DbgTrigSlct** attribute to create a trigger on the **LCB:TSM_PRESENT** signal on **LCB:J13:1**. This signal can be used to synchronize an oscilloscope or trigger a logic analyzer for diagnostic purposes. The **DbgTrigSlct** attribute has two fields: the module select bits (bits 6:3) which has the same coding as the **DbgSigSlct** attribute and the signal select bits (2:0) which select the individual signal from the selected module group