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# MONSOON

TORRENT DHE PSM ↔ LCB  
INTERFACE DESCRIPTION

Interface Control Document 7.4  
NOAO Document TRNT-AD-01-0004  
Version: 0

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# 1.0 Introduction

## 1.1 Purpose

This document defines the mechanical and electrical interface for the Monsoon Torrent Detector Controller. It is to be used as the reference for the design of all Power Supply Module (PSM) circuit boards that connect to the Local Control Board (LCB) using LCB Power connector (P1).

## 1.2 Reference Documents

The following documents contain additional information and are referenced in the text:

Torrent LCB Schematic Drawing – NOAO Document TRNT-EL-04-2002

Torrent DHE Hardware Description – NOAO Document TRNT-AD-08-0007

## 1.3 Acronyms and Glossary

### 1.3.1 Abbreviations and Acronyms

<b>12C</b>	A high speed serial communication bus
<b>AC</b>	Acquisition Camera
<b>ADC</b>	Analog to Digital Converter
<b>AFE</b>	Analog Front End (CCD or IR)
<b>BORG</b>	Basic Observer Response GUI
<b>CCD</b>	Charge Coupled Device
<b>CCDACQ</b>	CCD Acquisition Board
<b>CDS</b>	Correlated Double Sampler
<b>CLKBRD</b>	Clock and Bias Board
<b>COTS</b>	Commercial Off the Shelf
<b>CPCI</b>	Compact PCI
<b>CPLD</b>	Complex Programmable Logic Device
<b>CTC</b>	Command To Convert
<b>DAC</b>	Digital to Analog Converter
<b>DCS</b>	Detector Controller System (software)
<b>DHE</b>	Detector Head Electronics
<b>DHS</b>	Data Handling System
<b>DOP</b>	Data Output Port
<b>DTR</b>	Data Transfer Request
<b>ECS</b>	Enclosure Control System
<b>EEPROM</b>	Electrically Erasable Programmable Read Only Memory
<b>EIDN</b>	Electronic Identification Number
<b>EM</b>	Electromagnetic
<b>EMI</b>	Electromagnetic Interference
<b>ES</b>	Embedded System
<b>FITS</b>	Flexible Image Transport System

### 1.3.1 Abbreviations and Acronyms (Cont.)

<b>FP</b>	Focal Plane
<b>FPA</b>	Focal Plane Array
<b>FPDP</b>	Front Panel Data Port -
<b>FPGA</b>	Field Programmable Gate Array
<b>FPM</b>	Focal Plane Module
<b>GPX</b>	Generic Pixel Server
<b>HV</b>	High Voltage. In this application that is +30V or -30V.
<b>IAS</b>	Image Analysis System
<b>IC</b>	Integrated Circuit
<b>ICD</b>	Interface Control Document
<b>ICS</b>	Instrument Control System
<b>ID</b>	Identifier
<b>IDPS</b>	Image Data Preprocessor System
<b>IR</b>	Infrared
<b>JTAG</b>	The usual name used for the <u>IEEE</u> 1149.1 standard entitled <i>Standard Test Access Port and Boundary-Scan Architecture</i>
<b>KOSMOS</b>	Kitt Peak Ohio State Multi-Object Spectrograph
<b>LAN</b>	Local Area Network
<b>LCB</b>	Local Control Board
<b>MCB</b>	Master Control Board
<b>MEC</b>	MONSOON Engineering Console
<b>MHz</b>	MegaHertz
<b>MONSOON</b>	Not an acronym
<b>MOP</b>	MONSOON Observer Platform
<b>MSL</b>	MONSOON Supervisory Layer
<b>N/A</b>	Not Applicable
<b>NICD</b>	NOAO Interface Control Document
<b>NOCS</b>	NEWFIRM Observation Control System
<b>OCS</b>	Observatory Control System
<b>ODI</b>	One Degree Imager
<b>OTA</b>	Orthogonal Transfer Array
<b>PAN</b>	Pixel Acquisition Node
<b>PCB</b>	Printed Circuit Board
<b>PDF</b>	Parameter Description File
<b>PDT</b>	Parameter Description Table
<b>PRE</b>	Pre-amp Board (resides in the transition module)
<b>PSM</b>	Power Supply Module
<b>PWM</b>	Pulse Width Modulated
<b>QUOTA</b>	Quad Orthogonal Transfer Arrays
<b>RAM</b>	Random Access Memory
<b>ROI</b>	Region of Interest
<b>SCA</b>	Sensor Chip Assembly
<b>SUS</b>	Status Update System

### 1.3.1 Abbreviations and Acronyms (Cont.)

<b>SYSTRAN</b>	A high speed fibre optic communications board made by Systran.
<b>TBD</b>	To Be Decided
<b>Torrent</b>	Not an acronym
<b>TPA</b>	Transition Pre-amp Board
<b>TSM</b>	Transition Module
<b>TUB</b>	Transition Utility Board
<b>UDP</b>	User datagram Protocol
<b>UTIL</b>	Utility Board (Control for shutter, temperature, etc. reside in transition module)
<b>VHDL</b>	Verilog Hardware Description Language

### 1.3.2 Glossary

<b><i>.asm File</i></b>	A text file containing the assembly language program for a sequencer program to control a particular detector or focal plane segment.
<b><i>.cgf File</i></b>	A colon separated value file used by Torrent systems to describe the hardware attributes provided by the FPGA firmware. Read at run time to assist in the automatic creation of the .csv file for the detector system being run.
<b><i>.csv File</i></b>	Comma separated value file used by MONSOON and Torrent systems to describe the hardware and software attributes accessible to the GPX clients that control the pixel acquisition system through the GPX interface. Also used by Torrent systems to describe the desired attribute layout by page, column and positions for each attribute to be displayed.
<b><i>.dsc File</i></b>	A colon separated value file used by the Torrent focal planes configuration system to describe arrays, connectors and dewars and the common connections between them.
<b><i>.mod File</i></b>	Mode file, which is a text file containing a list of attribute setting commands to be used to put a MONSOON or Torrent system into a particular readout mode.
<b><i>.txt File</i></b>	A plain text file that contains lists of GUI categories or attributes either created at PAN process startup or read from the DHE and PAN to be stored in the attribute tables in a MONSOON formatted FITS file in the before and after housekeeping ASCII table extents.
<b><i>.ucd File</i></b>	A microcode file. A text file containing the sequencer memory addresses and hex values to be stored in that address. The values represent the machine language output of the asm5 program used to create a detector control sequencer program for a MONSOON or Torrent system from an .asm file.

### 1.3.2 Glossary (Cont.)

<b><i>.vhd File</i></b>	A firmware source code file read by assimilate to create the .cfg files required to describe the Torrent firmware. Also used to describe the PAN level software attributes used by the PAN processes.
<b><i>Byte</i></b>	Eight bits
<b><i>Command</i></b>	An instruction requiring a system to start some action. The action may result in a voltage changing or some internal parameters being set to particular values. A command may have command parameters (arguments) that contain the details of the instruction to be obeyed.
<b><i>Data Array</i></b>	The data, while it is stored in data processing memory, which resulted from one or more readouts of an IR array or CCD detector.
<b><i>Data Set</i></b>	A self-contained collection of data generated as a result of a Pixel Server obeying a <i>gpxStartExp</i> command. Each <i>gpxStartExp</i> command results in one and only one data set.
<b><i>Detector Head Electronics</i></b>	The lowest level hardware system. It is normally closely connected to the photon detector and coupled to the dewar in which the detector resides.
<b><i>Exposure</i></b>	The name used to describe the process and the data resulting from the process of resetting/clearing a detector, exposing it to photons and then reading one or more frames to determine the photon levels. These frames are processed into a data array, called an exposure, which may be further processed. (For example, an exposure would be the data array that results when a single Reset-Readout-Integrate-Readout cycle is performed on an IR detector or a single CCD Clear-Integrate-Readout cycle.)
<b><i>Exposure Sequence</i></b>	The process by which valid data is produced. Various levels of exposure sequencing occur during an observing run. At the lowest level there are the Reset-Readout-Integrate-Readout or Clear-Integrate-Readout cycles that result in a single IR or OUV exposure. At the highest level are the observing sequences that move the telescope, configure the instrument and take a series of exposures that create an observation.
<b><i>Focal Plane</i></b>	The geometrical plane where the image from an optical instrument is formed. This is the physical location of the detector device.
<b><i>Focal Plane Segment</i></b>	A collection of one or more detectors arranged to collect photons from an instrument. A Focal Plane Segment is controlled by a single Pixel Acquisition Node (PAN).



### 1.3.2 Glossary (Cont.)

<b>Frame</b>	The result of one or more readouts of an array averaged pixel by pixel. Each frame represents the signal values obtained from reading the entire ROI being read out of the detector. Multiple frames may be processed into a single exposure.
<b>Generic Pixel Server</b>	A pixel server that conforms to the GPX Interface description.
<b>Guide Core</b>	The software routines that calculate the centroids and image shifts required for controlling an Orthogonal Transfer Array (OTA).
<b>Guide Map</b>	An array of eight bytes that have a 1 in each position corresponding to an orthogonal transfer array (OTA) cell that will be used in the guide calculation.
<b>Guide Region</b>	A portion of an OTA guide cell as defined by the Guide Map that contains a guide star.
<b>Image</b>	The array of detector pixel and description data representing a science or diagnostic image or spectrum. An <i>image</i> is capable of being displayed or processed as a discrete entity. The values in the array may be stored in memory or on disk and are related to the data taken by the detector by some processing algorithm, (for example an <i>image</i> may consist of all the coadded and averaged exposures in one beam of a chop mode <i>gpxStartExp</i> command).
<b>Image Acquisition System</b>	A system of software and hardware capable of producing images from a focal plane on command.
<b>Image Server</b>	See Image Acquisition System.
<b>MONSOON Image Acquisition System</b>	A Generic Pixel Server. An extensible, modular Image Acquisition System. The system design is, to the extent possible, independent of the hardware being used in a particular implementation. Each component of the system should be capable of replacement by a similar component without having to redesign the rest of the system. Each component of the software is, as far as possible, independent of the underlying hardware and as modular as possible.
<b>MONSOON Star Date</b>	A date/time value that gives a unique ID to exposures in MONSOON systems. The MSD is formed using the JulianDay + TimeOfDay (to the nearest 86.4 ms .000001 of a day). The exposure ID is calculated to the nearest ms but on display is truncated to six decimal places.
<b>Observation</b>	The process of exposing the focal plane to photons in one or more exposures. The result of an observation is an image.

### 1.3.2 Glossary (Cont.)

<b><i>Pixel Acquisition Node</i></b>	The computer that handles the interface to the detector head electronics and the image pre-processing of the data stream from the <i>Detector Head Electronics</i> .
<b><i>Pixel Server</i></b>	A system which produces pixel values when requested to do so by some client system.
<b><i>Pixel Server System</i></b>	The combination of the <i>Detector Head Electronics</i> and a <i>Pixel Acquisition Node</i> which are coordinating the task of taking exposures and archive the resulting <i>data set</i> .
<b><i>Read</i></b>	When used as a noun to describe instrument data, this refers to a single read of a pixel on the detector. A read may consist of several A/D conversions of the pixel data that are averaged or processed in some other way to produce a single integer output value for the pixel. A Readout is made up of one read of each pixel in the detector ROI being read.
<b><i>Readout</i></b>	When used as a noun to describe instrument data, this refers to a single read of every pixel in the detector. One or more readouts can be averaged pixel by pixel to create a frame.
<b><i>Region of Interest</i></b>	A sub-array of the available detector area. There are two types of sub-arrays that can be defined. The Sequence ROI is on the active surface of the array used to increase the frequency of the Array readout. The Data Reduction ROI is an arbitrary rectangle of any size that fits on the Array. Data Reduction ROIs are defined to reduce the volume of data sent to the disk or DHS even when the entire array is being read out.
<b><i>Supervisory Node</i></b>	A computer capable of controlling multiple Image Acquisition systems. The computer that runs the software that conforms to the GPS interface.
<b><i>Value</i></b>	The value associated with an “attribute”.
<b><i>Word</i></b>	Four bytes or 32 bits.

## 1.4 Standard Terminology

To avoid confusion and to make very clear what the requirements for compliance are, many of the paragraphs in this standard are labeled with keywords that indicate the type of information they contain. The keywords are listed below:

RULE

RECOMMENDATION

SUGGESTION

PERMISSION

OBSERVATION

These keywords are used as follows:

### ***RULE***

**<Paragraph Number> Subject Describing Text**

### **RULE**

Rules form the basic framework of this draft standard. They are sometimes expressed in text form and sometimes in the form of figures, tables or drawings. All rules shall be followed to ensure compatibility between components. All rules use the “SHALL” or “SHALL NOT” words to emphasize the importance of the rule. The upper case “SHALL” or “SHALL NOT” words are reserved exclusively for stating rules in this standard and are not used for any other purpose.

### ***RECOMMENDATION***

**<Paragraph Number> Subject Describing Text**

### **RECOMMENDATION**

Wherever a recommendation appears, designers would be wise to take the advice given. Doing otherwise might result in some awkward problems or poor performance. It is possible to design a system that complies with all the rules but has poor performance. Recommendations found in this standard are based on this kind of experience and are provided to designers to speed their traversal of the learning curve. All recommendations use the “SHOULD” or “SHOULD NOT” words to emphasize the importance of the recommendation. The upper case “SHOULD” or “SHOULD NOT” words are reserved exclusively for stating recommendations in this draft standard and are not used for any other purpose.

### ***SUGGESTION***

**<Paragraph Number> Subject Describing Text**

### **SUGGESTION**

A suggestion contains advice that is helpful but not vital. The reader is encouraged to consider the advice before discarding it. Some design decisions that need to be made are difficult until experience has been gained. Suggestions are included to help a designer who has not yet gained this experience.

### ***PERMISSION***

**<Paragraph Number> Subject Describing Text**

### **PERMISSION**

In some cases a rule does not specifically prohibit a certain design approach, but the reader might be left wondering whether that approach might violate the spirit of the rule or whether it might lead to some subtle problem. Permissions reassure the reader that a certain approach is acceptable and will cause no problems. All permissions use the “MAY” word to emphasize the importance of the permission. The upper case word ”MAY” is reserved exclusively for stating permissions in this draft standard and is not used for any other purpose.

### ***OBSERVATION***

**<Paragraph Number> Subject Describing Text**

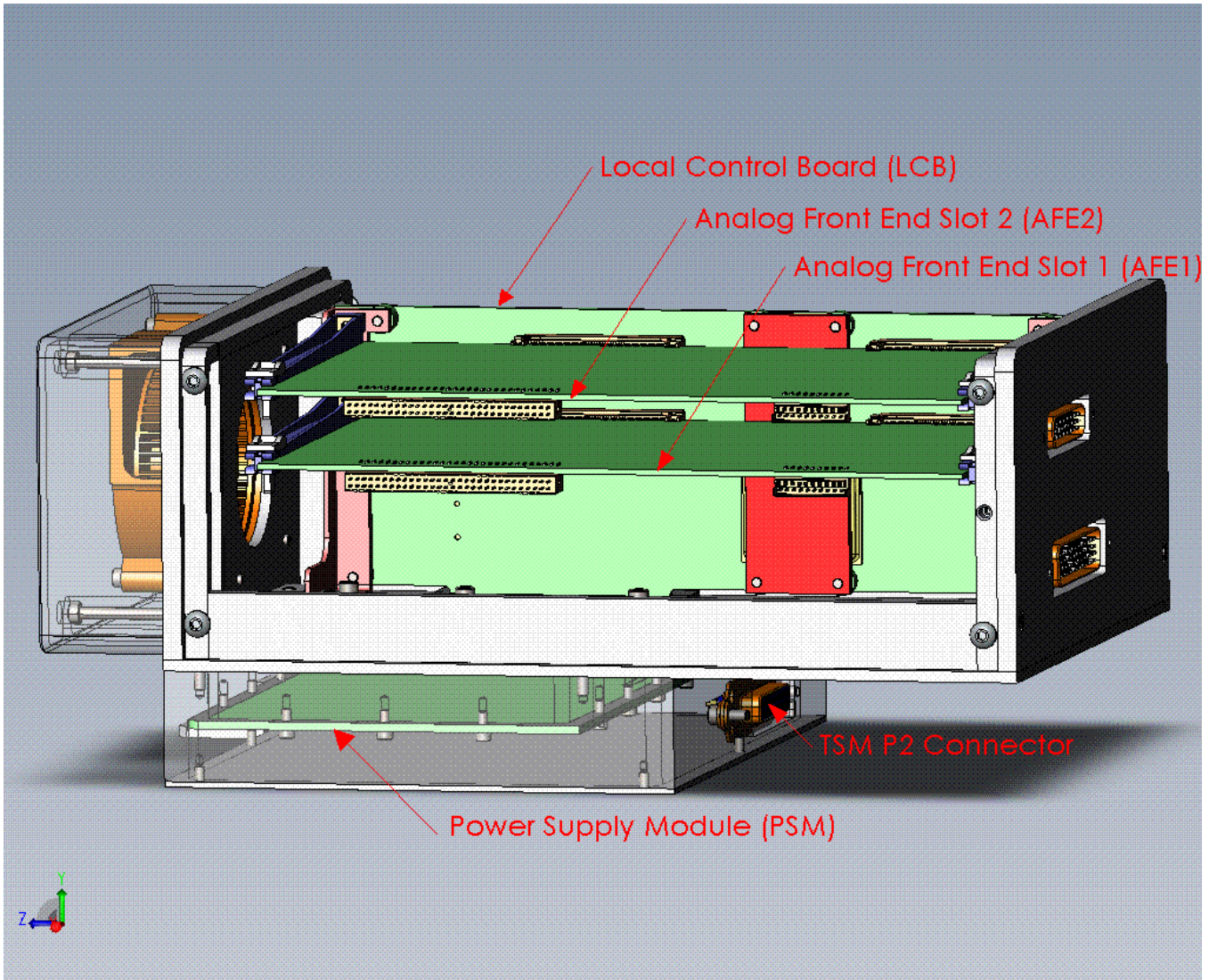
### **OBSERVATION**

Observations do not offer any specific advice. They usually follow naturally from what has just been discussed. They spell out the implications of certain rules and bring attention to things that might otherwise be overlooked. They also give the rationale behind certain rules so that the reader understands why the rules shall be followed.

## **2.0 Mechanical Interface**

### **2.1 Overview**

The Torrent Detector Head Electronics (DHE) requires power sources of appropriate voltage and capacity to function within the requirements of its application. The mechanical structure of the DHE provides a physical space to supply these requirements. The space provided for the Power Supply Module (PSM) is shown in Figure 1. The power supply module that fits into this space has provision to connect to the Local Control Board (LCB) using LCB connector P1 and to the Transition Module (TSM) via TSM connector P2. Provision is usually made on the rear bulkhead of the power supply chassis to support additional connectors for the supply of raw power and auxiliary signals required by the application of a Torrent controller.



Relative Position of the Power Supply Module (PSM) with Respect to the LCB  
Figure 1

## 2.1 Mechanical Specifications

### 2.2.1 Board Dimensions

#### RULE

The PSM circuit board SHALL comply with the dimensions given in Appendix I. This coincides with Torrent drawing TRNT-AD-01-xxxx.

### 2.2.2 PSM Board Thickness

#### RECOMMENDATION

The AFE circuit board SHOULD be nominally 0.090 inches (2.286mm) thick.

### **2.2.3 PSM Circuit Board Face Definition**

**RULE**

The 'TOP' side (layer one) of the circuit board SHALL be the side that is closest to the LCB board.

### **2.2.4 PSM ⇔ LCB Circuit Board Connector**

**RULE**

The PSM circuit board SHALL provide a connector position to interface to the LCB. The naming of this connector SHALL be J1 (mates to the LCB connector P1). The position of this connector SHALL be in accordance with the drawing shown in Appendix I.

### **2.2.5 PSM ⇔ LCB Circuit Board Connector Type**

**RULE**

The PSM circuit board connector J1 SHALL be of type SAMTEC LS2-130-01-L-D (60 position straight surface mount, 2.00mm pitch).

### **2.2.6 PSM ⇔ TSM Circuit Board Connector**

**PERMISSION**

The PSM circuit board MAY provide a connector position to interface to the TSM bulkhead connector if the DHE application requires it. The naming of the PSM mounted connector should be J2 (mates to bulkhead connector P2 and then to the TSM mounted connector J2). The position of this connector should facilitate connection to the floating bulkhead connector P2.

### **2.2.7 PSM ⇔ TSM Circuit Board Connector Type**

**PERMISSION**

If the PSM circuit board utilizes connector J2 it MAY be of any suitable type to connect to the DB25 type connector P2 on the bulkhead.

## **3.0 Electrical Interface**

### **3.1 Overview**

The electrical interface between the LCB and the PSM board has four groups of signals;

- Power supplies
- Control and status signals to / from the power supplies
- Control and status signals to / from the transition module
- Special purpose signals used to identify the PSM board characteristics.

The PSM ⇔ LCB interface connector provides the primary power supply required by the logic of the LCB. This one supply must be provided in any PSM configuration. In the standard design there is provision for another seven power supply paths on the LCB P1 connector, none of which are directly used by the LCB. One of these supply paths is designed for use by a cooling fan that regulates the operating temperature in the DHE enclosure. The six remaining supplies are, by current design, routed directly to the LCB Mezzanine board for power control and telemetry, and from there directly to the Analog Front End boards. The current design specifies these supplies and current limits as shown in Table 1.

**Table 5 – J1 Current Design Power Supply Potentials and Limits**

DESIG	DESCRIPTION	MIN V	MAX V	MIN I	AVG I	MAX I
VCC	PRIMARY LOGIC POWER SUPPLY	3.00V	3.60V	0.2	1.2	2.5
VFAN	DHE TEMPERATURE STABILIZATION	6V	14V	0.1	0.3	0.4
VCB+	POSITIVE CLOCK GENERATOR SUPPLY	+9V	+18V	0.006	0.35	0.65
VCB-	NEGATIVE CLOCK GENERATOR SUPPLY	-18V	-9V	0.006	0.35	0.65
VANA+	POSITIVE VIDEO CHAIN SUPPLY	+5V	+10V	0.006	0.4	0.72
VANA-	NEGATIVE VIDEO CHAIN SUPPLY	-10V	-5V	0.006	0.25	0.72
VHV+	POSITIVE HIGH VOLTAGE BIAS SUPPLY	+5V	+30V	0.006	0.12	0.2
VHV-	NEGATIVE HIGH VOLTAGE BIAS SUPPLY	-30V	-5V	0.006	0.12	0.2

All control signals going to the PSM and TSM are buffered by 3.3v LVTTL buffers of type 74ALVC244. All status signals coming the PSM and TSM are likewise buffered by the same LVTTL buffer type to provide isolation, increase drive capability and provide some first line protection to the LCB Virtex FPGA from possible faults and unexpected conditions on these signals.

The function of the LVTTL level control and status signals are determined entirely by firmware in the LCB Virtex FPGA, that is, these signals go directly to the I/O of the FPGA without any intervening logic. However, since buffers are employed on the control and status signals, the direction of the signals must be observed as shown in Table 2.

All signals in the special purpose group are also buffered by level translators for the same reasons. These signals use a NLSV2T244 driver type and NLSX3014 receiver type on the LCB. Signals in the special purpose group are used to provide board identification. The PSM board is expected to have this facility and employs a minimal standard circuit that provides PSM board identification, AFE board temperature monitoring and a modest amount of local EEPROM storage space for constants and calibration value saving. These functions are carried out by a dedicated I2C two-wire interface controlled by the LCB. See Appendix III.

Table 2 shows the PSM and TSM power, control and status signal assignments for J1 in the current design.

**Table 6 – PSM Control and Status Signals on the J1 Connector**

Signal Name	Pin Num J1	Sig Type	Direction (relative to LCB)	Description
VCC	1,3	PWR	IN	LOGIC POWER SUPPLY
GND	2,4,11,12,34,38,40,42,44,48,50,52	PWR	OUT	COMMON GROUND POINT OF DHE
VCC_SYNC	5	PULSE	OUT	SYNCHRONIZE THE SWITCHING FREQUENCY
SHUTTER	6	LEVEL	OUT	COMMAND TO TSM
/SHUTTER_CLOSE	7	LEVEL	IN	STATUS FROM TSM
/SHUTTER_OPEN	8	LEVEL	IN	STATUS FROM TSM
TEMP_1	9	FREQ	IN	DETECTOR TEMPERATURE SIGNAL
TEMP_2	10	FREQ	IN	DETECTOR TEMPERATURE SIGNAL
PREFLASH	13	LEVEL	OUT	COMMAND TO TSM
/PWR_KILL	14	LEVEL	OUT	COMMAND TO PSM – POWER SHUTDOWN
/PWR_INT	15	LEVEL	IN	STATUS FROM PSM – USER SHUTDOWN REQ
HTR_CURRENT	16	FREQ	IN	TELEMETRY FROM PSM – HEATER CURRENT
HTR_VOLTAGE	17	FREQ	IN	TELEMETRY FROM PSM – HEATER VOLTAGE
PSM_SDA_SRC	18	I2C	OUT	INTERFACE TO PCM SPECIAL CIRCUITS
TSM_SDA_SRC	19	I2C	OUT	INTERFACE TO TSM SPECIAL CIRCUITS
VANA_SYNC	20	PULSE	OUT	COMMAND TO PSM – VIDEO PS SYNC
VANA_ENBL	21	LEVEL	OUT	COMMAND TO PSM – VIDEO PS ENABLE
VCB_ENBL	22	LEVEL	OUT	COMMAND TO PSM – CLK & BIA PS ENABLE
VCB_SYNC	23	PULSE	OUT	COMMAND TO PSM – CLK & BIAS PS SYNC
/VHTR_SUSPEND	24	LEVEL	OUT	COMMAND TO PSM – DET HTR SUSPEND
VHTR_ENBL	25	LEVEL	OUT	COMMAND TO PSM – DET HTR ENABLE
PSM_SCL_SRC	26	I2C	OUT	INTERFACE TO PCM SPECIAL CIRCUITS
TSM_SCL_SRC	27	I2C	OUT	INTERFACE TO TSM SPECIAL CIRCUITS
VHTR_ADJ	28	PWM	OUT	COMMAND TO PSM – DET HTR ADJUST
PSM_SDA_SNS	29	I2C	IN	INTERFACE FROM PCM SPECIAL CIRCUITS
TSM_SDA_SNS	30	I2C	IN	INTERFACE FROM TSM SPECIAL CIRCUITS
VANA+_ADJ	31	PWM	OUT	COMMAND TO PSM – VIDEO PS ADJUST
VCB+_ADJ	32	PWM	OUT	COMMAND TO PSM – CLK & BIAS PS ADJUST
VCB-_ADJ	33	PWM	OUT	COMMAND TO PSM – CLK & BIAS PS ADJUST
VANA-	35,37	PWR	IN	NEGATIVE VIDEO POWER SUPPLY
VANA-_ADJ	36	PWM	OUT	COMMAND TO PSM – VIDEO PS ADJUST
VCB-	39,41	PWR	IN	NEGATIVE CLOCK & BIAS SUPPLY
VHV-	43	PWR	IN	NEGATIVE HIGH VOLTAGE SUPPLY
VHV_POLSLCT	45	LEVEL	OUT	COMMAND TO PSM – HV PS POLARITY
VHV_SYNC	46	PULSE	OUT	COMMAND TO PSM – HV PS SYNC
VHV+	47	PWR	IN	POSITIVE HIGH VOLTAGE BIAS SUPPLY



**Table 7 – PSM Control and Status Signals on the J1 Connector (cont.)**

Signal Name	Pin Num J1	Sig Type	Direction (relative to LCB)	Description
VCB+	49,51	PWR	IN	POSITIVE CLOCK & BIAS SUPPLY
VANA+	53,55	PWR	IN	POSITIVE VIDEO POWER SUPPLY
INPWR_SHLD	54,56	PWR	OUT	UNCOMMITTED SHIELD GROUND
VFAN_ADJ	57	PWM	OUT	COMMAND TO PSM – FAN ADJUST
VFAN_ENBL	58	LEVEL	OUT	COMMAND TO PSM – FAN ENABLE
VFAN	59	PWR	IN	FAN POWER SUPPLY POSITIVE
VFAN_RTN	60	PWR	OUT	FAN POWER SUPPLY NEGATIVE

## 3.2 Power Supply Specifications

### 3.2.1 LCB Digital Power Interface (VCC)

#### **RULE**

The PSM board SHALL incorporate circuitry to supply to a voltage potential of 3.3v +/- 10% to the LCB. This potential SHALL be capable of supporting a maximum continuous current of 2.5 Amps.

### 3.2.2 Grounding Scheme

#### **RULE**

The PSM circuit board SHALL provide a sufficiently low impedance path to the primary power source to limit the fluctuations of the PSM ⇔ LCB ground connector pins to within a 2mv pk-pk envelope based on a 2.5Amp current delta in the LCB.

### 3.2.3 Maximum Current Allowed on J1 Connector Pins

#### **RULE**

The maximum current allowed on each connected pin of the J1 connector SHALL be in accordance to the maximum specifications of the connector pair used for the interface. For the SAMTEC part connector (LS2-130-01-I-D) this limits the maximum current to be 5 Amps per contact at 20 Deg. C. ambient.

## 3.3 Digital Signal Specifications

### 3.3.1 LCB Interface Logic Input Voltage Levels

#### **RULE**

All digital interface signals that are directly connected to the J1 connector pins SHALL be defined as LVTTTL compatible. The minimum high level SHALL be 2.0volts into a 6ma load. The maximum low level input SHALL be 0.8 volts into a 6ma load.

### **3.3.2 LCB Interface Logic Output Voltage Levels**

### **RULE**

All digital interface signals that are directly connected to the J1 connector pins SHALL be defined as LVTTTL compatible. The minimum high level for signals coming from the LCB SHALL be defined as 2.4 volts into a 6ma load. The maximum low level for signals coming from the LCB SHALL be 0.4 volts into a 6ma load.

### **3.3.3 LCB Interface Signal Bandwidth**

### **RULE**

The maximum switching rate for digital signals supported by the LCB ⇔ PSM interface SHALL be 120 MHz.

### **3.3.4 LCB Pulse Width Modulation Control Signal**

### **RULE**

Circuits that use a pulse width modulation scheme (PWM) generated by the LCB for control SHALL be capable of interpreting a control range between 0% and 100% of the PWM signal. The PWM signal generated by the LCB SHALL have a minimum pulse repetition frequency of 300KHz and a maximum frequency of 500 KHz. The modulation depth of the PWM signal SHALL be 128:1.

### **3.3.4 LCB Pulse Control Signal**

### **RECOMMENDATION**

Circuits that are required to use a pulse control (PULSE) signal generated by the LCB SHOULD use the negative edge of the pulse signal for synchronization. The pulse signal generated by the LCB will have a minimum negative pulse width of 500ns and a maximum pulse width 50000ns. The minimum pulse repetition frequency will be 0 Hz and the maximum pulse frequency will be 1MHz.

## **3.4 Special Signal Specifications**

### **3.4.1 Reserved Connector Pin Numbers For Special Signals**

### **RULE**

Connector J1 pin numbers 18, 19, 26, 27, 29, and 30 SHALL NOT be used for other purposes than those specified in this section.

### **3.4.2 PSM Board Serial Number**

### **RULE**

The PSM circuit board SHALL include a circuit to provide unique identification to the LCB (silicon serial number). The interface to this circuit SHALL be via the I2C protocol using three wired connections. See Appendix III for the circuit.

### **3.4.3 PSM Silicon Serial Number Identification Device**

### **RULE**

The silicon serial number device type SHALL be electrically and functionally equivalent to the DS28CM00 device from Maxim / Dallas Semiconductor. This device has a fixed address code of 0x50.

### 3.4.4 PSM Temperature Telemetry

### RECOMMENDATION

The PSM circuit board SHOULD include a circuit to provide temperature measurement of the circuit board surface temperatures to the LCB (silicon temperature sensors). There SHOULD be two sensors; ideally mounted to provide a representative indication of the heat generated by the PSM. The interface to this circuit SHOULD be via the I2C protocol using three wired connections. See Appendix III for the circuit.

### 3.4.5 PSM Temperature Telemetry Device

### RULE

If the temperature telemetry facility is implemented (3.4.4) then the device used to implement this SHALL be electrically and functionally equivalent to the MCP9803 device from Microchip and the addresses SHALL be programmed as 0x48 and 0x49 respectively.

### 3.4.6 PSM Configuration Parameter EEPROM

### RECOMMENDATION

The PSM circuit board SHOULD include a circuit to provide access to a non-volatile memory device that can be used to store calibration constants and parameters that are unique to the PSM Board. The interface to this circuit SHOULD be via the I2C protocol using three wired connections. See Appendix III for the circuit.

### 3.4.7 PSM EEPROM Address

### RULE

If the Non-Volatile Parameter EEPROM facility is implemented (3.4.6), then the EEPROM type SHALL be electrically and functionally equivalent to the 24AA128 device from Microchip and the address SHALL be programmed as 0x54 by tying pins A0 and A1 low with pin A2 high.

### 3.4.8 Special Signal Power Supply

### RULE

The semiconductor devices SHALL be powered by the principal 3.3v VCC power supply provided by the PSM. Ground pins of these devices SHALL be connected to the 3.3v VCC power supply return point.

### 3.4.9 TSM Special Circuit Signal Pass-through

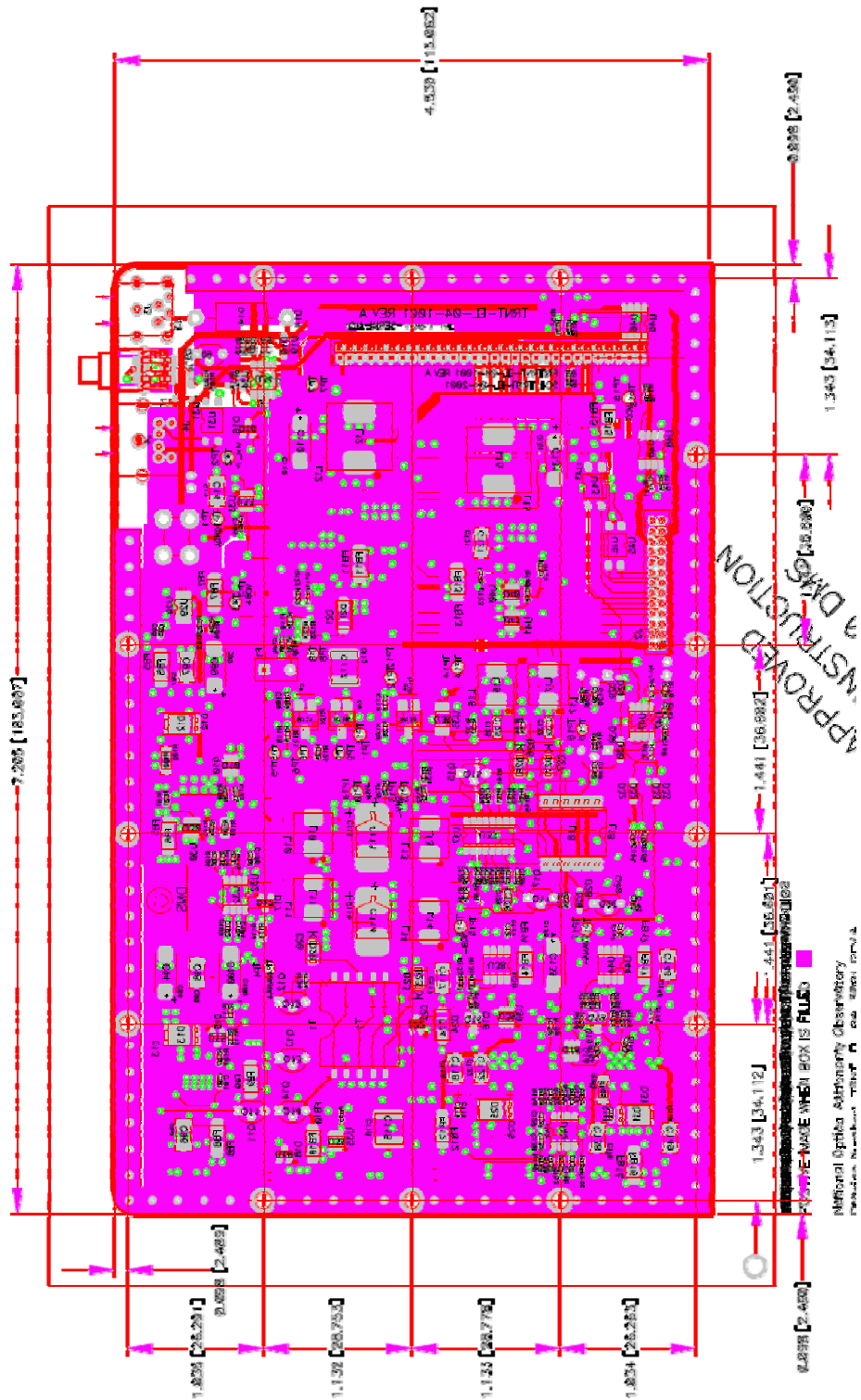
### RULE

If the optional TSM connector is supplied then the PSM SHALL provide a feedthrough for the special circuit signals required by the TSM between PSM connectors J1 and P2. These feed-through connections SHALL be in accordance with Table 3.

**Table 8 - Special Signal Pass Through to TSM**

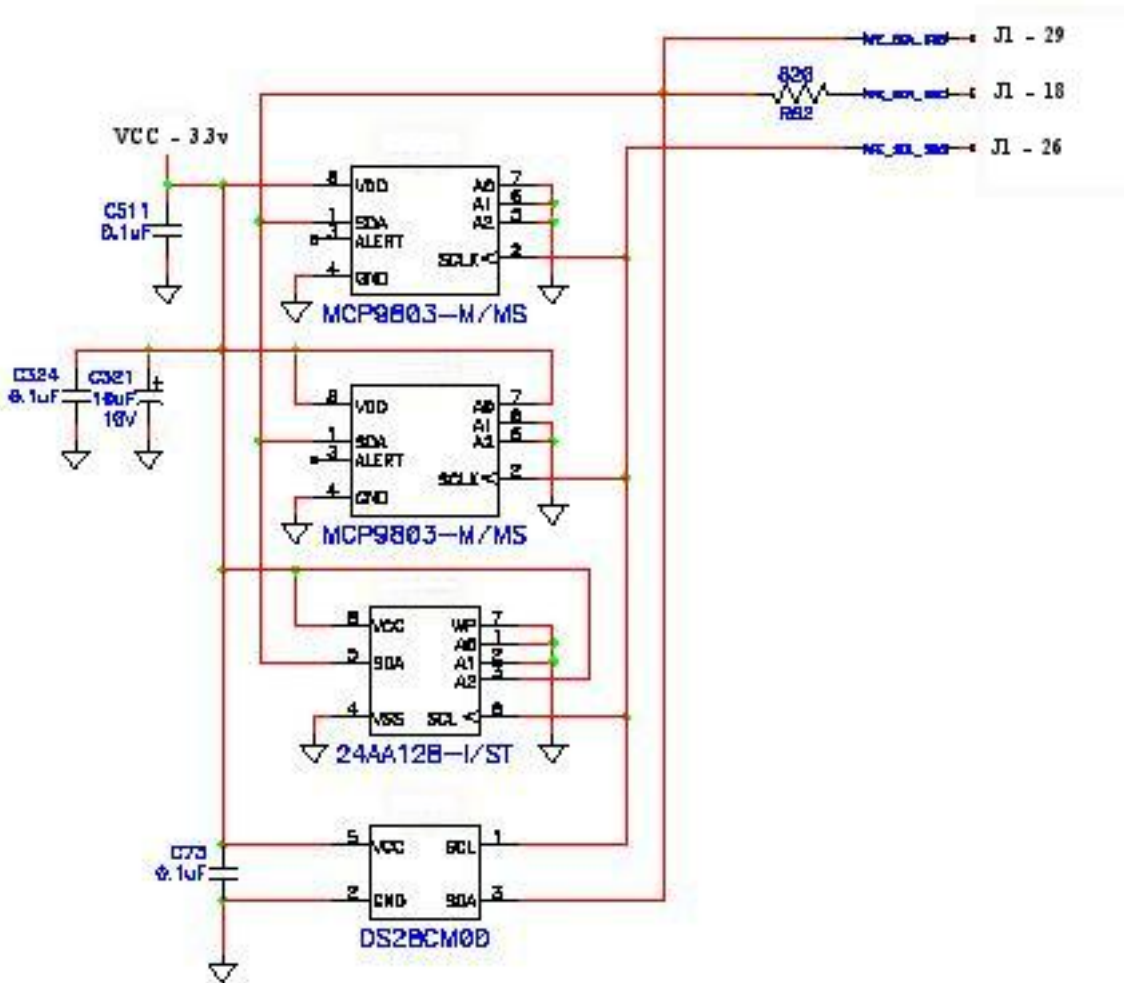
PSM J1 Pin	Signal	PSM P2 Pin
19	TSM_SDA_SRC	15
30	TSM_SDA_SNS	16
27	TSM_SCL_SRC	14

# 4.0 Appendix I – Board Dimensions



Board Dimensions  
Figure 2

## 5.0 Appendix II – Special Signal Circuitry



Special Signal Circuitry  
Figure 3