NATIONAL
OPTICAL
ASTRONOMY
OBSERVATORY

SYSTEM INSTRUMENTATION GROUP
950 N. Cherry Ave.
P. O. Box 26732
Tucson, Arizona 85726-6732
(520) 318-8000 FAX: (520) 318-8303

MONSOON

TORRENT DHE BUS
INTERFACE DESCRIPTION

Interface Control Document 7.3
NOAO Document TRNT-AD-01-0003
Version: 0

Authored by:
Peter Moore

Please send comments:
pmoore@noao.edu

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0	8/10/2009	All	Initial draft release - aro

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1.0 Introduction

1.1 Purpose

This document defines the mechanical and electrical interface for the Monsoon Torrent Detector Controller. It is to be used as the reference for the design of all Analog Front End (AFE) circuit boards that connect to the Local Control Board (LCB) at positions AFE 1 and AFE 2.

1.2 Reference Documents

The following documents contain additional information and are referenced in the text:

Torrent LCB Schematic Drawing – NOAO Document TRNT-EL-04-2002_rOD
Torrent AFE Board Outline Drawing – NOAO Document TRNT-AD-01-0001
Torrent DHE Hardware Description – NOAO Document TRNT-AD-08-0007

1.3 Acronyms and Glossary

1.3.1 Abbreviations and Acronyms

12C	A high speed serial communication bus
AC	Acquisition Camera
ADC	Analog to Digital Converter
AFE	Analog Front End (CCD or IR)
BORG	Basic Observer Response GUI
CCD	Charge Coupled Device
CCDACQ	CCD Acquisition Board
CDS	Correlated Double Sampler
CLKBRD	Clock and Bias Board
COTS	Commercial Off the Shelf
CPCI	Compact PCI
CPLD	Complex Programmable Logic Device
CTC	Command To Convert
DAC	Digital to Analog Converter
DCS	Detector Controller System (software)
DHE	Detector Head Electronics
DHS	Data Handling System
DOP	Data Output Port
DTR	Data Transfer Request
ECS	Enclosure Control System
EEPROM	Electrically Erasable Programmable Read Only Memory
EIDN	Electronic Identification Number
EM	Electromagnetic
EMI	Electromagnetic Interference
ES	Embedded System
FITS	Flexible Image Transport System

1.3.1 Abbreviations and Acronyms (Cont.)

FP	Focal Plane
FPA	Focal Plane Array
FPDP	Front Panel Data Port -
FPGA	Field Programmable Gate Array
FPM	Focal Plane Module
GPX	Generic Pixel Server
HV	High Voltage. In this application that is +30V or -30V.
IAS	Image Analysis System
IC	Integrated Circuit
ICD	Interface Control Document
ICS	Instrument Control System
ID	Identifier
IDPS	Image Data Preprocessor System
IR	Infrared
JTAG	The usual name used for the IEEE 1149.1 standard entitled ***Standard Test Access Port and Boundary-Scan Architecture***
KOSMOS	Kitt Peak Ohio State Multi-Object Spectrograph
LAN	Local Area Network
LCB	Local Control Board
MCB	Master Control Board
MEC	MONSOON Engineering Console
MHz	MegaHertz
MONSOON	Not an acronym
MOP	MONSOON Observer Platform
MSL	MONSOON Supervisory Layer
N/A	Not Applicable
NICD	NOAO Interface Control Document
NOCS	NEWFIRM Observation Control System
OCS	Observatory Control System
ODI	One Degree Imager
OTA	Orthogonal Transfer Array
PAN	Pixel Acquisition Node
PCB	Printed Circuit Board
PDF	Parameter Description File
PDT	Parameter Description Table
PRE	Pre-amp Board (resides in the transition module)
PSM	Power Supply Module
PWM	Pulse Width Modulated
QUOTA	Quad Orthogonal Transfer Arrays
RAM	Random Access Memory
ROI	Region of Interest
SCA	Sensor Chip Assembly
SUS	Status Update System

1.3.1 Abbreviations and Acronyms (Cont.)

SYSTRAN	A high speed fibre optic communications board made by Systran.
TBD	To Be Decided
Torrent	Not an acronym
TPA	Transition Pre-amp Board
TSM	Transition Module
TUB	Transition Utility Board
UDP	User datagram Protocol
UTIL	Utility Board (Control for shutter, temperature, etc. reside in transition module)
VHDL	Verilog Hardware Description Langauge

1.3.2 Glossary

.asm File A text file containing the assembly language program for a sequencer program to control a particular detector or focal plane segment.

.cgf File A colon separated value file used by Torrent systems to describe the hardware attributes provided by the FPGA firmware. Read at run time to assist in the automatic creation of the .csv file for the detector system being run.

.csv File Comma separated value file used by MONSOON and Torrent systems to describe the hardware and software attributes accessible to the GPX clients that control the pixel acquisition system through the GPX interface. Also sued by Torrent systems to describe the desired attribute layout by page, column and positions for each attribute to be displayed.

.dsc File A colon separated value file used by the Torrent focal planes configuration system to describe arrays, connectors and dewars and the common connections between them.

.mod File Mode file, which is a text file containing a list of attribute setting commands to be sued to put a MONSOON or Torrent system into a particular readout mode.

.txt File A plain text file that contains lists of GUI categories or attributes either created at PAN process startup or read from the DHE and PAN to be stored in the attribute tables in a MONSOON formatted FITS file in the before and after housekeeping ASCII table extents.

.ucd File A microcode file. A text file containing the sequencer memory addresses and hex values to be stored in that address. The values represent the machine language output of the asm5 program used to create a detector control sequencer program for a MONSOON or Torrent system from an .asm file.

1.3.2 Glossary (Cont.)

.vhd File	A firmware source code file read by assimilate to create the .cfg files required to describe the Torrent firmware. Also used to describe the PAN level software attributes used by the PAN processes.
Byte	Eight bits
Command	An instruction requiring a system to start some action. The action may result in a voltage changing or some internal parameters being set to particular values. A command may have command parameters (arguments) that contain the details of the instruction to be obeyed.
Data Array	The data, while it is stored in data processing memory, which resulted from one or more readouts of an IR array or CCD detector.
Data Set	A self-contained collection of data generated as a result of a Pixel Server obeying a *gpxStartExp* command. Each *gpxStartExp* command results in one and only one data set.
Detector Head Electronics	The lowest level hardware system. It is normally closely connected to the photon detector and coupled to the dewar in which the detector resides.
Exposure	The name used to describe the process and the data resulting from the process of resetting/clearing a detector, exposing it to photons and then reading one or more frames to determine the photon levels. These frames are processed into a data array, called an exposure, which may be further processed. (For example, an exposure would be the data array that results when a single Reset-Readout-Integrate-Readout cycle is performed on an IR detector or a single CCD Clear-Integrate-Readout cycle.)
Exposure Sequence	The process by which valid data is produced. Various levels of exposure sequencing occur during an observing run. At the lowest level there are the Reset-Readout-Integrate-Readout or Clear-Integrate-Readout cycles that result in a single IR or OUV exposure. At the highest level are the observing sequences that move the telescope, configure the instrument and take a series of exposures that create an observation.
Focal Plane	The geometrical plane where the image from an optical instrument is formed. This is the physical location of the detector device.
Focal Plane Segment	A collection of one or more detectors arranged to collect photons from an instrument. A Focal Plane Segment is controlled by a single Pixel Acquisition Node (PAN).

1.3.2 Glossary (Cont.)

Frame	The result of one or more readouts of an array averaged pixel by pixel. Each frame represents the signal values obtained from reading the entire ROI being read out of the detector. Multiple frames may be processed into a single exposure.
Generic Pixel Server	A pixel server that conforms to the GPX Interface description.
Guide Core	The software routines that calculate the centroids and image shifts required for controlling an Orthogonal Transfer Array (OTA).
Guide Map	An array of eight bytes that have a 1 in each position corresponding to an orthogonal transfer array (OTA) cell that will be used in the guide calculation.
Guide Region	A portion of an OTA guide cell as defined by the Guide Mapthat contains a guide star.
Image	The array of detector pixel and description data representing a science or diagnostic image or spectrum. An *image* is capable of being displayed or processed as a discrete entity. The values in the array may be stored in memory or on disk and are related to the data taken by the detector by some processing algorithm, (for example an *image* may consist of all the coadded and averaged exposures in one beam of a chop mode *gpxStartExp* command).
Image Acquisition System	A system of software and hardware capable of producing images from a focal plane on command.
Image Server	See Image Acquisition System.
MONSOON Image Acquisition System	A Generic Pixel Server. An extensible, modular Image Acquisition System. The system design is, to the extent possible, independent of the hardware being used in a particular implementation. Each component of the system should be capable of replacement by a similar component without having to redesign the rest of the system. Each component of the software is, as far as possible, independent of the underlying hardware and as modular as possible.
MONSOON Star Date	A date/time value that gives a unique ID to exposures in MONSOON systems. The MSD is formed using the JulianDay + TimeOfDay (to the nearest 86.4 ms .000001 of a day). The exposure ID is calculated to the nearest ms but on display is truncated to six decimal places.
Observation	The process of exposing the focal plane to photons in one or more exposures. The result of an observation is an image.

1.3.2 Glossary (Cont.)

Pixel Acquisition Node	The computer that handles the interface to the detector head electronics and the image pre-processing of the data stream from the *Detector Head Electronics.*
Pixel Server	A system which produces pixel values when requested to do so by some client system.
Pixel Server System	The combination of the *Detector Head Electronics* and a *Pixel Acquisition Node* which are coordinating the task of taking exposures and archive the resulting *data set.*
Read	When used as a noun to describe instrument data, this refers to a single read of a pixel on the detector. A read may consist of several A/D conversions of the pixel data that are averaged or processed in some other way to produce a single integer output value for the pixel. A Readout is made up of one read of each pixel in the detector ROI being read.
Readout	When used as a noun to describe instrument data, this refers to a single read of every pixel in the detector. One or more readouts can be averaged pixel by pixel to create a frame.
Region of Interest	A sub-array of the available detector area. There are two types of sub-arrays that can be defined. The Sequence ROI is on the active surface of the array used to increase the frequency of the Array readout. The Data Reduction ROI is an arbitrary rectangle of any size that fits on the Array. Data Reduction ROIs are defined to reduce the volume of data sent to the disk or DHS even when the entire array is being read out.
Supervisory Node	A computer capable of controlling multiple Image Acquisition systems. The computer that runs the software that conforms to the GPS interface.
Value	The value associated with an “attribute”.
Word	Four bytes or 32 bits.

1.4 Standard Terminology

To avoid confusion and to make very clear what the requirements for compliance are, many of the paragraphs in this standard are labeled with keywords that indicate the type of information they contain. The keywords are listed below:

RULE

RECOMMENDATION

SUGGESTION

PERMISSION

OBSERVATION

These keywords are used as follows:

RULE

<Paragraph Number> Subject Describing Text RULE

Rules form the basic framework of this draft standard. They are sometimes expressed in text form and sometimes in the form of figures, tables or drawings. All rules shall be followed to ensure compatibility between components. All rules use the “SHALL” or “SHALL NOT” words to emphasize the importance of the rule. The upper case “SHALL” or “SHALL NOT” words are reserved exclusively for stating rules in this standard and are not used for any other purpose.

RECOMMENDATION

<Paragraph Number> Subject Describing Text RECOMMENDATION

Wherever a recommendation appears, designers would be wise to take the advice given. Doing otherwise might result in some awkward problems or poor performance. It is possible to design a system that complies with all the rules but has poor performance. Recommendations found in this standard are based on this kind of experience and are provided to designers to speed their traversal of the learning curve. All recommendations use the “SHOULD” or “SHOULD NOT” words to emphasize the importance of the recommendation. The upper case “SHOULD” or “SHOULD NOT” words are reserved exclusively for stating recommendations in this draft standard and are not used for any other purpose.

SUGGESTION

<Paragraph Number> Subject Describing Text SUGGESTION

A suggestion contains advice that is helpful but not vital. The reader is encouraged to consider the advice before discarding it. Some design decisions that need to be made are difficult until experience has been gained. Suggestions are included to help a designer who has not yet gained this experience.

PERMISSION

<Paragraph Number> Subject Describing Text PERMISSION

In some cases a rule does not specifically prohibit a certain design approach, but the reader might be left wondering whether that approach might violate the spirit of the rule or whether it might lead to some subtle problem. Permissions reassure the reader that a certain approach is acceptable and will cause no problems. All permissions use the “MAY” word to emphasize the importance of the permission. The upper case word ”MAY” is reserved exclusively for stating permissions in this draft standard and is not used for any other purpose.

OBSERVATION

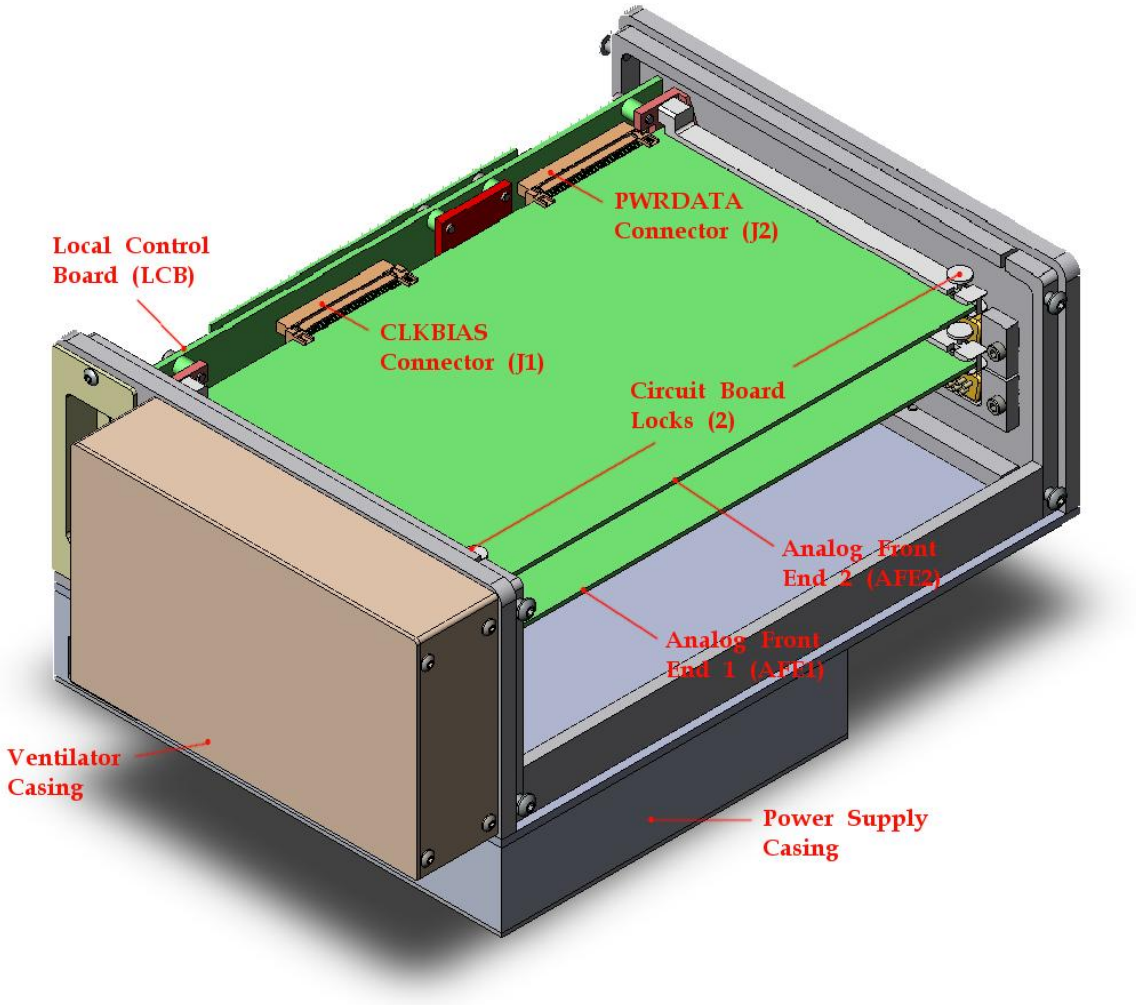
<Paragraph Number> Subject Describing Text OBSERVATION

Observations do not offer any specific advice. They usually follow naturally from what has just been discussed. They spell out the implications of certain rules and bring attention to things that might otherwise be overlooked. They also give the rationale behind certain rules so that the reader understands why the rules shall be followed.

2.0 Mechanical Interface

2.1 Overview

The Torrent Local Control Board (LCB) provides support for two circuit boards that are plugged directly into the LCB assembly. These boards are the Analog Front End (AFE) boards since the primary design purpose of them is to provide an interface to some specific type of detector via analog circuitry. However, the use of these boards is not limited to analog circuitry and the interface provides ample flexibility for whatever purpose may be invented for it. Each AFE board connects to the LCB via two identical inline connectors that provide power, bi-directional digital signals for control and data, and a common ground reference and power return. There are two positions provided for AFE boards referenced as AFE1 and AFE2. The relative position of these basic interface components is shown in Fig 1.



Relative Positions of the AFE with Respect to the LCB
Figure 1

2.2 Mechanical Specifications

2.2.1 AFE Board Dimensions RULE

The AFE circuit board SHALL comply with the dimensions given in Appendix I. This coincides with Torrent drawing TRNT-AD-01-0001.

2.2.2 AFE Board Thickness RULE

The AFE circuit board SHALL be nominally 0.062 inches (1.60mm) thick.

2.2.3 AFE Circuit Board Face Definition RECOMMENDATION

The 'TOP' side (layer one) of the circuit board SHALL be the side that is closest to the power supply casing.

2.2.4 AFE Circuit Board Connectors RECOMMENDATION

The AFE circuit board SHOULD utilize both (two) connector positions to interface to the LCB. The naming of these connectors SHOULD be P1 (mates to the LCB connector J1) and P2 (mates to the LCB connector J2).

2.2.5 AFE Circuit Board Connector Type RULE

The AFE circuit board connectors SHALL be of type SAMTEC ERM8-050-01-S-D-EM2 (100 position edge mount, 0.8mm pitch, for 0.062" board thickness).

3.0 Electrical Interface

3.1 Overview

The electrical interface between the LCB and each AFE board has three groups of signals; power supplies, bi-directional digital signals used for control and data transfer, and a small group of dedicated purpose signals. There are seven separate power supplies available to each AFE with a common ground reference and power return. The LCB supplies 134 digital signals that are split into two named groups according to which connector they are present on (CLKBIAS on LCB J1 or PWRDATA on LCB J2). There are seven dedicated signals used for board identification, temperature telemetry, on board constant storage and provision of a failsafe shutdown signal. There are three unassigned pins (out of a total of 200) that should not be used and are marked as **RESERVED**.

The power supplies that are available to each AFE are used to derive all the potentials and power that is required to supply all of the circuitry between the detector and the LCB, that is, there is no provision for external or additional power supplies to enter the AFE boards. There are six general-purpose supplies that are controlled by the LCB. These supplies can be adjusted in voltage, enabled or disabled, and their current draw is monitored by the LCB.

These supplies also have electronic over-current protection and controlled turn-on times. One supply is dedicated to furnishing standby potential to the digital receiver devices on the AFE. This supply, called the VPIFC, is powered from the LCB side when power is disabled on the AFE. After power is enabled to the AFE, the AFE board is required to supply sufficient potential on the VPIFC supply rail to back bias the diode on the LCB side of this supply. The potential generated by the AFE board must be sufficient to ensure that any digital noise from the LCB power supply cannot contaminate the AFE circuits. The available supplies and current limits (for combined consumption of AFE1 and AFE2) are shown in Table 1.

Table 6 - Power Supply Potentials and Limits

DESIG	DESCRIPTION	MIN V	MAX V	MIN I	AVG I	MAX I
VCB+	POSITIVE CLOCK GENERATOR SUPPLY	+9V	+18V	0.006	0.35	0.65
VCB-	NEGATIVE CLOCK GENERATOR SUPPLY	-18V	-9V	0.006	0.35	0.65
VANA+	POSITIVE VIDEO CHAIN SUPPLY	+5V	+10V	0.006	0.4	0.72
VANA-	NEGATIVE VIDEO CHAIN SUPPLY	-10V	-5V	0.006	0.25	0.72
VHV+	POSITIVE HIGH VOLTAGE BIAS SUPPLY	+5V	+30V	0.006	0.12	0.2
VHV-	NEGATIVE HIGH VOLTAGE BIAS SUPPLY	-30V	-5V	0.006	0.12	0.2

All signals in the digital group are buffered by bi-directional voltage translators and connect to the Virtex 5 FPGA device on the LCB. The assignment of digital signals is accomplished through the firmware that is loaded to the FPGA and by the hardware that is present on the AFE. Therefore it is important to make sure that any particular AFE board version is only used with a compatible LCB firmware version. All signal directions can be allocated as LCB ⇨ AFE (control), AFE ⇨ LCB (data), or AFE ⇔ LCB (bi-directional and not recommended). Some of the pin assignments for signals in the digital group are interleaved to allow a common AFE board layout to have independent signal lines depending on whether the board is inserted into the AFE1 or AFE2 LCB position. To facilitate this, the odd/even signal number pairs in this group are pin swapped on the LCB connectors between the AFE1 board slot and the AFE2 board slot. This allows two AFE boards with a common design, (with identical P1 and P2 pin out assignments) to be independently controlled by the LCB Virtex FPGA. A typical interface circuit for the AFE is shown in Appendix II. This example has been adapted from the current Torrent CCD AFE interface design and shows signals typical to CCD controller use.

Each AFE board is expected to have a minimal standard circuit that provides AFE board identification, AFE board temperature monitoring and a modest amount of local EEPROM storage space for constants and calibration value saving. These functions are carried out by a dedicated I2C two-wire interface controlled by the LCB. See Appendix III.

Table 2 and Table 3 show the signal assignments for the two interface connectors P1 (CLKBIAS) and P2 (PWRDATA) on the AFE board.

Table 7 - P1 Signal Descriptions – AFE CLKBIAS Connector

Signal Name	Pin Num AFE1	Pin Num AFE2	Direction (relative to AFE)	Description
VPIFC	1	1	IN/PWR	Digital interface power ~2.7v
VPIFC	2	2	IN/PWR	
AFE_CLKBIASIO[0]	3	3	IN/OUT	
AFE_CLKBIASIO[1]	4	4	IN/OUT	
AFE_CLKBIASIO[2]	5	5	IN/OUT	
AFE_CLKBIASIO[3]	6	6	IN/OUT	
AFE_CLKBIASIO[4]	7	7	IN/OUT	
AFE_CLKBIASIO[5]	8	8	IN/OUT	
AFE_CLKBIASIO[6]	9	9	IN/OUT	
AFE_CLKBIASIO[7]	10	10	IN/OUT	
AFE_CLKBIASIO[8]	11	11	IN/OUT	
AFE_CLKBIASIO[9]	12	12	IN/OUT	
AFE_CLKBIASIO[10]	13	13	IN/OUT	
AFE_CLKBIASIO[11]	14	14	IN/OUT	
AFE_CLKBIASIO[12]	15	15	IN/OUT	
AFE_CLKBIASIO[13]	16	16	IN/OUT	
AFE_CLKBIASIO[14]	17	17	IN/OUT	
AFE_CLKBIASIO[15]	18	18	IN/OUT	
AFE_CLKBIASIO[16]	19	19	IN/OUT	
AFE_CLKBIASIO[17]	20	20	IN/OUT	
AFE_CLKBIASIO[18]	21	21	IN/OUT	
AFE_CLKBIASIO[19]	22	22	IN/OUT	
AFE_CLKBIASIO[20]	23	23	IN/OUT	
AFE_CLKBIASIO[21]	24	24	IN/OUT	
AFE_CLKBIASIO[22]	25	25	IN/OUT	
AFE_CLKBIASIO[23]	26	26	IN/OUT	
AFE_CLKBIASIO[24]	27	27	IN/OUT	
AFE_CLKBIASIO[25]	28	28	IN/OUT	
AFE_CLKBIASIO[26]	29	29	IN/OUT	
AFE_CLKBIASIO[27]	30	30	IN/OUT	
AFE_CLKBIASIO[28]	31	31	IN/OUT	
AFE_CLKBIASIO[29]	32	32	IN/OUT	
AFE_CLKBIASIO[30]	33	33	IN/OUT	
AFE_CLKBIASIO[31]	34	34	IN/OUT	

Table 8 - P1 Signal Descriptions – AFE CLKBIAS Connector (cont.)

Signal Name	Pin Num AFE1	Pin Num AFE2	Direction (relative to AFE)	Description
AFE_CLKBIASIO[32]	35	35	IN/OUT	
AFE_CLKBIASIO[33]	36	36	IN/OUT	
AFE_CLKBIASIO[34]	37	37	IN/OUT	
AFE_CLKBIASIO[35]	38	38	IN/OUT	
AFE_CLKBIASIO[36]	39	39	IN/OUT	
AFE_CLKBIASIO[37]	40	40	IN/OUT	
AFE_CLKBIASIO[38]	41	41	IN/OUT	
AFE_CLKBIASIO[39]	42	42	IN/OUT	
AFE_CLKBIASIO[40]	43	43	IN/OUT	
AFE_CLKBIASIO[41]	44	44	IN/OUT	
AFE_CLKBIASIO[42]	45	45	IN/OUT	
AFE_CLKBIASIO[43]	46	46	IN/OUT	
AFE_CLKBIASIO[44]	47	47	IN/OUT	
AFE_CLKBIASIO[45]	48	48	IN/OUT	
AFE_CLKBIASIO[46]	49	49	IN/OUT	
AFE_CLKBIASIO[47]	50	50	IN/OUT	
AFE_CLKBIASIO[48]	51	51	IN/OUT	
AFE_CLKBIASIO[49]	52	52	IN/OUT	
AFE_CLKBIASIO[50]	53	53	IN/OUT	
AFE_CLKBIASIO[51]	54	54	IN/OUT	
AFE_CLKBIASIO[52]	55	55	IN/OUT	
AFE_CLKBIASIO[53]	56	56	IN/OUT	
AFE_CLKBIASIO[54]	57	57	IN/OUT	
AFE_CLKBIASIO[55]	58	58	IN/OUT	
AFE_CLKBIASIO[56]	59	59	IN/OUT	
AFE_CLKBIASIO[57]	60	60	IN/OUT	
AFE_CLKBIASIO[58]	61	61	IN/OUT	
AFE_CLKBIASIO[59]	62	62	IN/OUT	
AFE_CLKBIASIO[60]	63	63	IN/OUT	
AFE_CLKBIASIO[61]	64	64	IN/OUT	
AFE_CLKBIASIO[62]	65	65	IN/OUT	
AFE_CLKBIASIO[63]	66	66	IN/OUT	
AFE_CLKBIASIO[64]	67	67	IN/OUT	
AFE_CLKBIASIO[65]	68	68	IN/OUT	

Table 9 - P1 Signal Descriptions – AFE CLKBIAS Connector (cont.)

Signal Name	Pin Num AFE1	Pin Num AFE2	Direction (relative to AFE)	Description
AFE_CLKBIASIO[66]	69	69	IN/OUT	
AFE_CLKBIASIO[67]	70	70	IN/OUT	
AFE_CLKBIASIO[68]	71	71	IN/OUT	
AFE_CLKBIASIO[69]	72	72	IN/OUT	
AFE_CLKBIASIO[70]	73	73	IN/OUT	
AFE_CLKBIASIO[71]	74	74	IN/OUT	
AFE_CLKBIASIO[72]	75	75	IN/OUT	
AFE_CLKBIASIO[73]	76	76	IN/OUT	
AFE_CLKBIASIO[74]	77	77	IN/OUT	
AFE_CLKBIASIO[75]	78	78	IN/OUT	
AFE_CLKBIASIO[76]	79	79	IN/OUT	
AFE_CLKBIASIO[77]	80	80	IN/OUT	
AFE_CLKBIASIO[78]	81	81	IN/OUT	
AFE_CLKBIASIO[79]	82	82	IN/OUT	
AFE_CLKBIASIO[80]	83	84	IN/OUT	
AFE_CLKBIASIO[81]	84	83	IN/OUT	
AFE_CLKBIASIO[82]	85	86	IN/OUT	
AFE_CLKBIASIO[83]	86	85	IN/OUT	
AFE_CLKBIASIO[84]	87	88	IN/OUT	
AFE_CLKBIASIO[85]	89	90	IN/OUT	
AFE_CLKBIASIO[86]	88	87	IN/OUT	
AFE_CLKBIASIO[87]	90	89	IN/OUT	
AFE_CLKBIASIO[88]	91	92	IN/OUT	
AFE_CLKBIASIO[89]	93	94	IN/OUT	
AFE_CLKBIASIO[90]	92	91	IN/OUT	
AFE_CLKBIASIO[91]	94	93	IN/OUT	
AFE_SDA_SRC[0]	95	96	IN/OUT	
AFE_SDA_SRC[1]	96	95	IN/OUT	
AFE_SDA_SENSE[0]	97	98	IN/OUT	
AFE_SDA_SENSE[1]	98	97	IN/OUT	
AFE_SCL_SRC[0]	99	100	IN/OUT	
AFE_SCL_SRC[1]	100	99	IN/OUT	

Table 10 - P2 Signal Descriptions – AFE PWRDATA Connector

Signal Name	Pin Num AFE1	Pin Num AFE2	Direction (relative to AFE)	Description
AFE_ANA+	1	1	IN/PWR	Adjustable between +5v => +10v
AFE_ANA+	2	2	IN/PWR	
AFE_GND	3	3	IN/PWR	
AFE_GND	4	4	IN/PWR	
AFE_CB+	5	5	IN/PWR	Adjustable between +10v => +18v
AFE_CB+	6	6	IN/PWR	
AFE_GND	7	7	IN/PWR	
AFE_GND	8	8	IN/PWR	
AFE_VHV+	9	9	IN/PWR	Switchable between +5v and +30v
AFE_VHV+	10	10	IN/PWR	
AFE_GND	11	11	IN/PWR	
AFE_GND	12	12	IN/PWR	
AFE_VANA-	13	13	IN/PWR	Adjustable between -5v => -10v
AFE_VANA-	14	14	IN/PWR	
AFE_GND	15	15	IN/PWR	
AFE_GND	16	16	IN/PWR	
AFE_VCB-	17	17	IN/PWR	Adjustable between -10v => -18v
AFE_VCB-	18	18	IN/PWR	
AFE_VHV-	19	19	IN/PWR	Switchable between -30v and -5v
AFE_VHV-	20	20	IN/PWR	
AFE_SHIELD	21	21	IN/OUT	For cable shields, etc.
AFE_SHIELD	22	22	IN/OUT	
RESERVED	23	23		
RESERVED	24	24		
RESERVED	25	25		
/WATCHDOG_FAIL	26	26	IN	Normally high when system stable
AFE_PWRDATAIO[0]	27	28	IN/OUT	
AFE_PWRDATAIO[18]	28	27	IN/OUT	
AFE_PWRDATAIO[1]	29	30	IN/OUT	
AFE_PWRDATAIO[19]	30	29	IN/OUT	
AFE_PWRDATAIO[2]	31	32	IN/OUT	
AFE_PWRDATAIO[20]	32	31	IN/OUT	
AFE_PWRDATAIO[3]	33	34	IN/OUT	
AFE_PWRDATAIO[21]	34	33	IN/OUT	
AFE_PWRDATAIO[4]	35	36	IN/OUT	
AFE_PWRDATAIO[22]	36	35	IN/OUT	
AFE_PWRDATAIO[5]	37	38	IN/OUT	
AFE_PWRDATAIO[23]	38	37	IN/OUT	
AFE_PWRDATAIO[6]	39	40	IN/OUT	

Table 11 - P2 Signal Descriptions – AFE PWRDATA Connector (cont.)

Signal Name	Pin Num AFE1	Pin Num AFE2	Direction (relative to AFE)	Description
AFE_PWRDATAIO[24]	40	39	IN/OUT	
AFE_PWRDATAIO[7]	41	42	IN/OUT	
AFE_PWRDATAIO[25]	42	41	IN/OUT	
AFE_PWRDATAIO[8]	43	44	IN/OUT	
AFE_PWRDATAIO[26]	44	43	IN/OUT	
AFE_PWRDATAIO[9]	45	46	IN/OUT	
AFE_PWRDATAIO[27]	46	45	IN/OUT	
AFE_PWRDATAIO[10]	47	48	IN/OUT	
AFE_PWRDATAIO[28]	48	47	IN/OUT	
AFE_PWRDATAIO[11]	49	50	IN/OUT	
AFE_PWRDATAIO[29]	50	49	IN/OUT	
AFE_PWRDATAIO[12]	51	52	IN/OUT	
AFE_PWRDATAIO[30]	52	51	IN/OUT	
AFE_PWRDATAIO[13]	53	54	IN/OUT	
AFE_PWRDATAIO[31]	54	53	IN/OUT	
AFE_PWRDATAIO[14]	55	56	IN/OUT	
AFE_PWRDATAIO[32]	56	55	IN/OUT	
AFE_PWRDATAIO[15]	57	58	IN/OUT	
AFE_PWRDATAIO[33]	58	57	IN/OUT	
AFE_PWRDATAIO[16]	59	60	IN/OUT	
AFE_PWRDATAIO[34]	60	59	IN/OUT	
AFE_PWRDATAIO[17]	61	62	IN/OUT	
AFE_PWRDATAIO[35]	62	61	IN/OUT	
AFE_PWRDATAIO[36]	63	63	IN/OUT	
AFE_PWRDATAIO[37]	64	64	IN/OUT	
AFE_PWRDATAIO[38]	65	65	IN/OUT	
AFE_PWRDATAIO[39]	66	66	IN/OUT	
AFE_PWRDATAIO[40]	67	67	IN/OUT	
AFE_PWRDATAIO[41]	68	68	IN/OUT	
AFE_PWRDATAIO[42]	69	69	IN/OUT	
AFE_PWRDATAIO[43]	70	70	IN/OUT	
AFE_PWRDATAIO[44]	71	72	IN/OUT	
AFE_PWRDATAIO[52]	72	71	IN/OUT	
AFE_PWRDATAIO[45]	73	74	IN/OUT	
AFE_PWRDATAIO[53]	74	73	IN/OUT	
AFE_PWRDATAIO[46]	75	76	IN/OUT	
AFE_PWRDATAIO[54]	76	75	IN/OUT	
AFE_PWRDATAIO[47]	77	78	IN/OUT	
AFE_PWRDATAIO[55]	78	77	IN/OUT	

Table 12 - P2 Signal Descriptions – AFE PWRDATA Connector (cont.)

Signal Name	Pin Num AFE1	Pin Num AFE2	Direction (relative to AFE)	Description
AFE_PWRDATAIO[48]	79	80	IN/OUT	
AFE_PWRDATAIO[56]	80	79	IN/OUT	
AFE_PWRDATAIO[49]	81	82	IN/OUT	
AFE_PWRDATAIO[57]	82	81	IN/OUT	
AFE_PWRDATAIO[50]	83	84	IN/OUT	
AFE_PWRDATAIO[58]	84	83	IN/OUT	
AFE_PWRDATAIO[51]	85	86	IN/OUT	
AFE_PWRDATAIO[59]	86	85	IN/OUT	
AFE_PWRDATAIO[60]	87	88	IN/OUT	
AFE_PWRDATAIO[62]	88	87	IN/OUT	
AFE_PWRDATAIO[61]	89	90	IN/OUT	
AFE_PWRDATAIO[63]	90	89	IN/OUT	
AFE_PWRDATAIO[64]	91	92	IN/OUT	
AFE_PWRDATAIO[66]	92	91	IN/OUT	
AFE_PWRDATAIO[65]	93	94	IN/OUT	
AFE_PWRDATAIO[67]	94	93	IN/OUT	
AFE_PWRDATAIO[68]	95	96	IN/OUT	
AFE_PWRDATAIO[70]	96	95	IN/OUT	
AFE_PWRDATAIO[69]	97	98	IN/OUT	
AFE_PWRDATAIO[71]	98	97	IN/OUT	
AFE_PWRDATAIO[72]	99	100	IN/OUT	
AFE_PWRDATAIO[73]	100	99	IN/OUT	

3.2 Power Supply Specifications

3.2.1 AFE Digital Interface Power (VPIFC) RULE

The AFE board SHALL incorporate circuitry to drive the VPIFC supply to a potential of 3.3v or higher. This implies that the circuits used to interface the AFE to the LCB SHALL operate at a signaling level of 3.3v or higher. The maximum potential for VPIFC SHALL be 4.5v.

3.2.2 AFE Grounding Scheme RULE

The AFE circuit board SHALL have separate ground planes for the analog and digital signal and power returns. These grounds SHALL be physically connected together at a position as close as possible to the AFE_GND pins of connector P2.

3.2.3 AFE Maximum Current Draw (Two Identical AFE Boards) RULE

For DHE configurations that use two identical AFE circuit boards, each AFE circuit board SHALL limit the current draw on the power supply rails to one half of the ‘Max I’ value shown in Table 1.

3.2.4 AFE Maximum Current Draw (Single AFE Board) PERMISSION

For a DHE configuration that one AFE circuit board, The AFE circuit board MAY limit the current draw on the power supply rails to that of the ‘Max I’ value shown in Table 1.

3.2.5 AFE Maximum Current Draw (Mixed AFE Boards) OBSERVATION

Obviously for DHE configurations that employ mixed AFE circuit board types, the combined AFE circuit board current draw on the power supply rails must not exceed the ‘Max I’ value shown in Table 1. There is an electronic current limiter that will shut down the power supplies to the AFE circuit boards should a current draw exceeding 1.3 times the ‘MAX I’ persist for more than 50ms.

3.2.6 Reverse Voltage Protection SUGGESTION

Since the power supplies to the AFE circuit boards may be interrupted (power enables, over voltage / over current shutdown, etc.), there is the possibility of leakage currents from an active supply forcing a reverse potential into another inactive supply rail. It is suggested that polarized components (e.g. capacitors, semiconductors, etc) that may be damaged from having a reverse potential applied to them be protected by clamp diodes on the power supply rails to limit this possibility.

3.3 Digital Signal Specifications

3.3.1 AFE Interface Logic Input Voltage Levels RULE

All digital interface signals that are directly connected to the P1 / P2 connector pins SHALL be defined as CMOS with a supply voltage of VPIFC. The minimum high level for signals coming from the LCB and driving the AFE circuitry SHALL be defined as 0.8 x VPIFC. The maximum low level for signals coming from the LCB and driving the AFE circuitry shall be 0.2 x VPIFC.

3.3.2 AFE Interface Logic Output Voltage Levels RULE

The minimum high level for signals coming from the AFE and going to the LCB SHALL be defined as 0.8 x VPIFC. The maximum low level for signals coming from the AFE and going to the LCB SHALL be 0.2 x VPIFC.

3.3.3 AFE Interface Bandwidth RULE

The maximum switching rate for digital signals supported by the LCB ⇔ AFE interface SHALL be 40 MHz.

3.3.4 AFE Interface Bandwidth OBSERVATION

The LCB ⇔ AFE interface is clocked at a 80Mhz rate, which guarantees that a 50% duty cycle pulse train at 40MHz will be seen and correctly interpreted. However, a single pulse that is 12.5ns wide will be distorted in pulse width due the asynchronous nature of the relationship between the LCB register clock and the occurrence of the AFE pulse. This implies that where pulse width is important the minimum pulse width sent by the AFE or the LCB should be 4 x LCB register clocks wide (50ns).

3.3.5 AFE Interface Clock Source RECOMMENDATION

Where signals generated by the AFE are required to be accompanied by a synchronous clock (e.g. Synchronous Serial Interface, etc.) the clock source SHOULD be generated by the LCB Firmware sourced to the AFE through the interface to the AFE. This clock can then be used to latch the data signals on the AFE circuit board and convert the signal(s) into synchronous edge aligned data.

3.4 Special Signal Specifications

3.4.1 Reserved Connector Pin Numbers for Special Signals RULE

Connector P1 pin number 95 through to 100 inclusive SHALL NOT be used for other purposes than those specified in this section.

3.4.2 AFE Board Type Identification RULE

Connector P1 pin 99 (AFE_SCL_SRC[0]) is reserved to provide an identification of the AFE board type to the LCB during power up. This pin SHALL be left floating with respect to DGnd for AFE boards that are classified as CCD types and SHALL have an impedance of 4.99K to DGnd for all other AFE board types.

3.4.3 AFE Board Serial Number RECOMMENDATION

The AFE circuit board SHOULD include a circuit to provide unique identification to the LCB (silicon serial number). The interface to this circuit SHOULD be via the I2C protocol using three wired connections (see Appendix III for the circuit).

3.4.4 AFE Silicon Serial Number Identification Device RULE

If the identification facility is implemented (3.4.1) then the device type SHALL be electrically and functionally equivalent to the DS28CM00 device from Maxim / Dallas Semiconductor. This device has a fixed address code of 0x50.

3.4.5 AFE Temperature Telemetry RECOMMENDATION

The AFE circuit board SHOULD include a circuit to provide measurement of the circuit board surface temperatures to the LCB (silicon temperature sensors). There SHOULD be two sensors; one mounted on the upper face and one on the lower face of the circuit board. The position of these sensors is not critical but SHOULD indicate a representative value of the hottest parts of the board where heat dissipation is greatest. The interface to this circuit SHOULD be via the I2C protocol using three wired connections. See Appendix III for the circuit.

3.4.6 AFE Temperature Telemetry Device RULE

If the temperature telemetry facility is implemented (3.4.3) then the device used to implement this SHALL be electrically and functionally equivalent to the MCP9803 device from Microchip and the addresses SHALL be programmed as 0x48 and 0x49 respectively.

3.4.7 AFE Configuration Parameter EEPROM RECOMMENDATION

The AFE circuit board SHOULD include a circuit to provide access to a non-volatile memory device that can be used to store calibration constants and parameters that are specific to the AFE Board. The interface to this circuit SHOULD be via the I2C protocol using three wired connections. See Appendix III for the circuit.

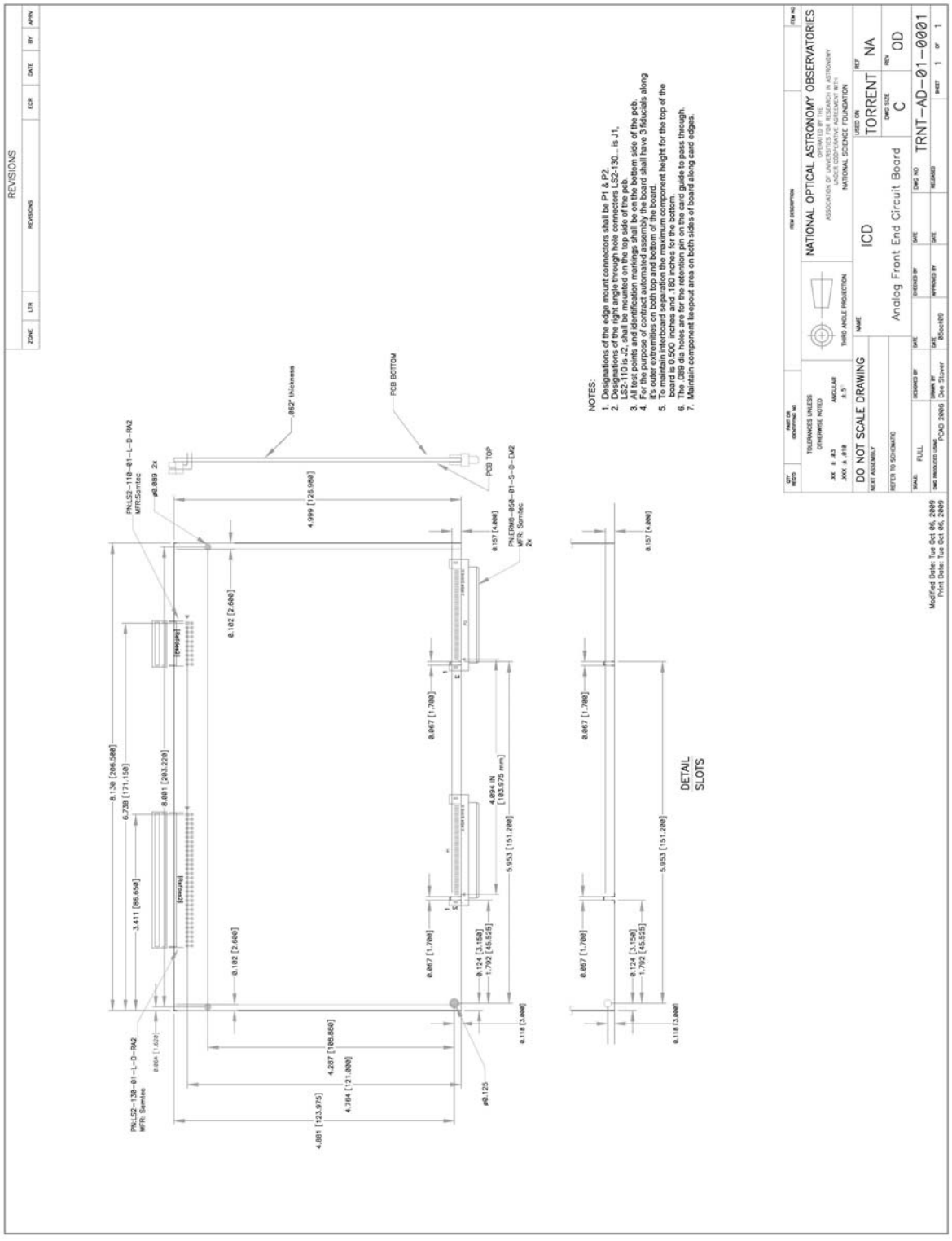
3.4.8 AFE EEPROM Address RULE

If the Non-Volatile Parameter EEPROM facility is implemented (3.4.5) then the EEPROM type SHALL be electrically and functionally equivalent to the 24AA128 device from Microchip and the address SHALL be programmed as 0x54 by tying pins A0 and A1 low with pin A2 high.

3.4.9 Special Signal Power Supply RULE

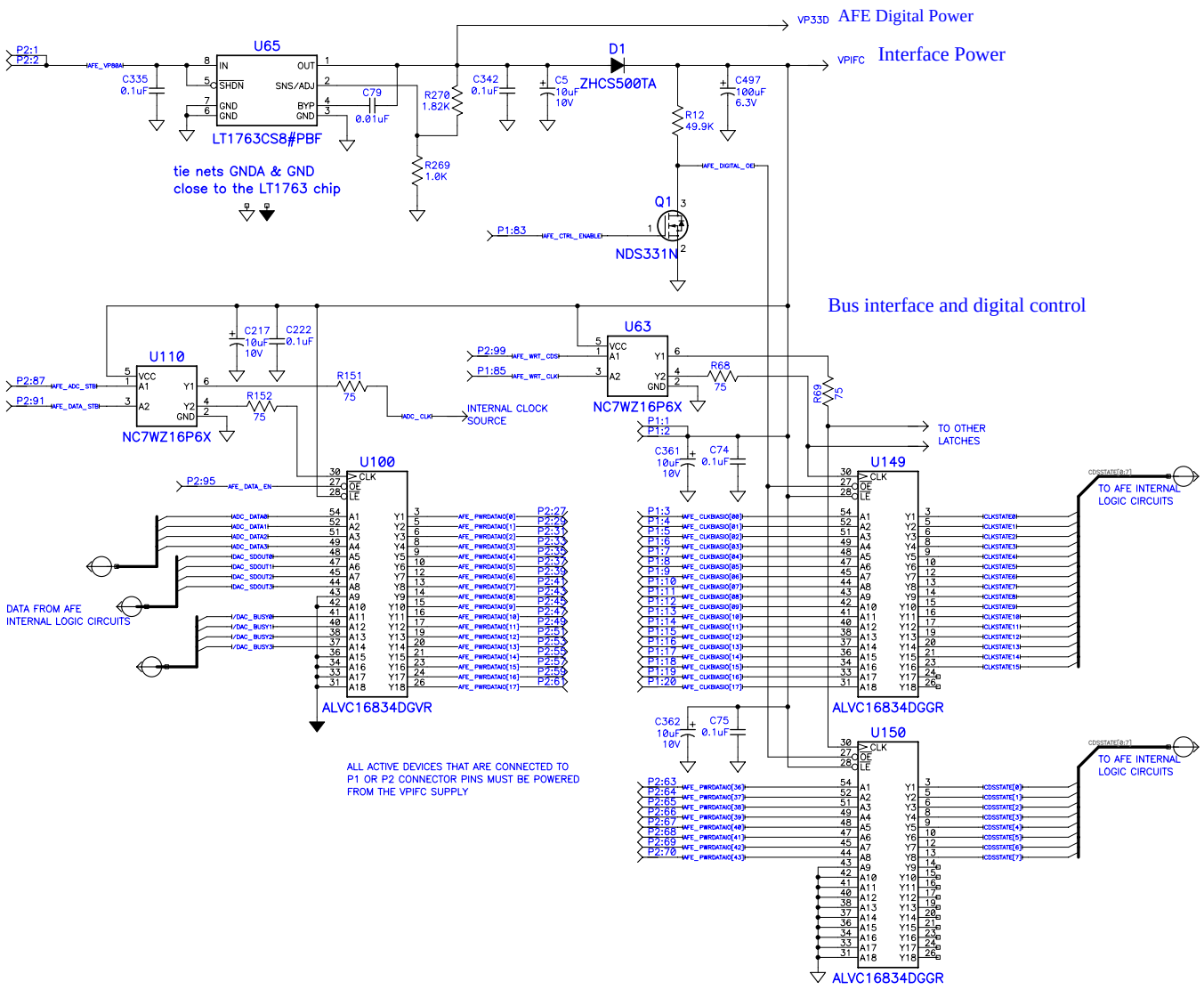
If any of the “Special Signal” facilities are implemented (3.4.1, 3.4.3, or 3.4.5) then the semiconductor devices SHALL only be powered by the VPIFC supply and the power Gnd pins of these devices SHALL be connected to the AFE ‘DGnd’.

4.0 Appendix I – Board Dimensions



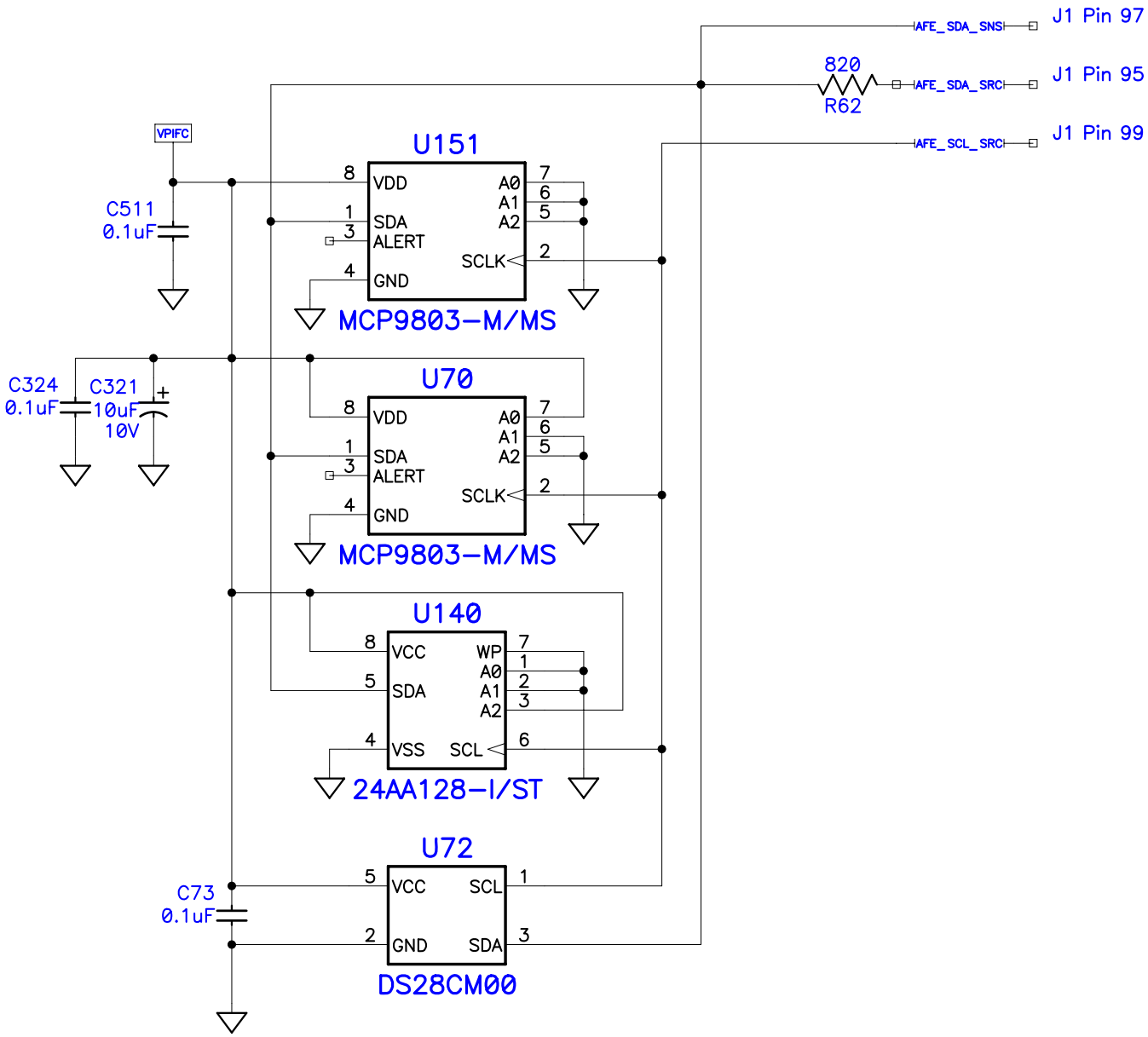
Board Dimensions
Figure 2

5.0 Appendix II – Recommended Digital Interface Circuit



Recommended Digital Interface Circuit
Figure 3

6.0 Appendix III – Special Signal Circuitry



Special Signal Circuitry
Figure 3

7.0 Appendix IV – CCD AFE Connector Assignments

Table 13 - CCD AFE P1 Connector Assignments

Signal Name	Pin Num AFE1	Direction (relative to AFE)	CCD AFE Signal Name
VPIFC	1	IN/PWR	VPIFC
VPIFC	2	IN/PWR	VPIFC
AFE_CLKBIASIO[0]	3	IN	CLKSTATE0
AFE_CLKBIASIO[1]	4	IN	CLKSTATE1
AFE_CLKBIASIO[2]	5	IN	CLKSTATE2
AFE_CLKBIASIO[3]	6	IN	CLKSTATE3
AFE_CLKBIASIO[4]	7	IN	CLKSTATE4
AFE_CLKBIASIO[5]	8	IN	CLKSTATE5
AFE_CLKBIASIO[6]	9	IN	CLKSTATE6
AFE_CLKBIASIO[7]	10	IN	CLKSTATE7
AFE_CLKBIASIO[8]	11	IN	CLKSTATE8
AFE_CLKBIASIO[9]	12	IN	CLKSTATE9
AFE_CLKBIASIO[10]	13	IN	CLKSTATE10
AFE_CLKBIASIO[11]	14	IN	CLKSTATE11
AFE_CLKBIASIO[12]	15	IN	CLKSTATE12
AFE_CLKBIASIO[13]	16	IN	CLKSTATE13
AFE_CLKBIASIO[14]	17	IN	CLKSTATE14
AFE_CLKBIASIO[15]	18	IN	CLKSTATE15
AFE_CLKBIASIO[16]	19		
AFE_CLKBIASIO[17]	20		
AFE_CLKBIASIO[18]	21		
AFE_CLKBIASIO[19]	22	IN	CLKENABLE0
AFE_CLKBIASIO[20]	23	IN	CLKENABLE1
AFE_CLKBIASIO[21]	24	IN	CLKENABLE2
AFE_CLKBIASIO[22]	25	IN	CLKENABLE3
AFE_CLKBIASIO[23]	26	IN	TP_CLK
AFE_CLKBIASIO[24]	27	IN	TP_DATA0
AFE_CLKBIASIO[25]	28	IN	TP_DATA1
AFE_CLKBIASIO[26]	29	IN	TP_DATA2
AFE_CLKBIASIO[27]	30	IN	TP_DATA3
AFE_CLKBIASIO[28]	31	IN	/TP_LOAD0
AFE_CLKBIASIO[29]	32	IN	/TP_LOAD1
AFE_CLKBIASIO[30]	33	IN	/TP_LOAD2
AFE_CLKBIASIO[31]	34	IN	/TP_LOAD3
AFE_CLKBIASIO[32]	35		
AFE_CLKBIASIO[33]	36		

Table 14 - CCD AFE P1 Connector Assignments (cont.)

Signal Name	Pin Num AFE1	Direction (relative to AFE)	CCD AFE Signal Name
AFE_CLKBIASIO[34]	37		
AFE_CLKBIASIO[35]	38		
AFE_CLKBIASIO[36]	39		
AFE_CLKBIASIO[37]	40		
AFE_CLKBIASIO[38]	41		
AFE_CLKBIASIO[39]	42		
AFE_CLKBIASIO[40]	43		
AFE_CLKBIASIO[41]	44		
AFE_CLKBIASIO[42]	45		
AFE_CLKBIASIO[43]	46		
AFE_CLKBIASIO[44]	47		
AFE_CLKBIASIO[45]	48		
AFE_CLKBIASIO[46]	49		
AFE_CLKBIASIO[47]	50		
AFE_CLKBIASIO[48]	51	IN	DAC_SDIN
AFE_CLKBIASIO[49]	52	IN	/DAC_SYNC0
AFE_CLKBIASIO[50]	53	IN	/DAC_SYNC1
AFE_CLKBIASIO[51]	54	IN	/DAC_SYNC2
AFE_CLKBIASIO[52]	55	IN	/DAC_SYNC3
AFE_CLKBIASIO[53]	56	IN	/DAC_LDAC0
AFE_CLKBIASIO[54]	57	IN	/DAC_LDAC1
AFE_CLKBIASIO[55]	58	IN	/DAC_LDAC2
AFE_CLKBIASIO[56]	59	IN	/DAC_LDAC3
AFE_CLKBIASIO[57]	60	IN	/TELMON0_SYNC
AFE_CLKBIASIO[58]	61	IN	/TELMON1_SYNC
AFE_CLKBIASIO[59]	62	IN	/TELADC0_SYNC
AFE_CLKBIASIO[60]	63		
AFE_CLKBIASIO[61]	64	IN	/TELMUX0_SYNC
AFE_CLKBIASIO[62]	65	IN	/TELMUX1_SYNC
AFE_CLKBIASIO[63]	66	IN	TELADC_DIN
AFE_CLKBIASIO[64]	67	IN	BIAS_EN0
AFE_CLKBIASIO[65]	68	IN	BIAS_EN1
AFE_CLKBIASIO[66]	69	IN	BIAS_EN2
AFE_CLKBIASIO[67]	70	IN	BIAS_EN3
AFE_CLKBIASIO[68]	71	IN	DAC_PD0
AFE_CLKBIASIO[69]	72	IN	DAC_PD1
AFE_CLKBIASIO[70]	73	IN	DAC_PD2
AFE_CLKBIASIO[71]	74	IN	DAC_PD3

Table 15 - CCD AFE P1 Connector Assignments (cont.)

Signal Name	Pin Num AFE1	Direction (relative to AFE)	CCD AFE Signal Name
AFE_CLKBIASIO[72]	75	IN	/DAC_CLR0
AFE_CLKBIASIO[73]	76	IN	/DAC_CLR1
AFE_CLKBIASIO[74]	77	IN	/DAC_CLR2
AFE_CLKBIASIO[75]	78	IN	/DAC_CLR3
AFE_CLKBIASIO[76]	79	IN	/DAC_RESET
AFE_CLKBIASIO[77]	80	IN	DAC_SCLK
AFE_CLKBIASIO[78]	81	IN	TEL_SCLK
AFE_CLKBIASIO[79]	82		
AFE_CLKBIASIO[80]	83	IN	AFE_CTRL_ENABLE
AFE_CLKBIASIO[81]	84		
AFE_CLKBIASIO[82]	85	IN	AFE_WRT_CLK
AFE_CLKBIASIO[83]	86		
AFE_CLKBIASIO[84]	87	IN	AFE_SPR_DIN
AFE_CLKBIASIO[86]	88		
AFE_CLKBIASIO[85]	89	IN	AFE_WRT_UTIL
AFE_CLKBIASIO[87]	90		
AFE_CLKBIASIO[88]	91	OUT	AFE_SPR_DOUT
AFE_CLKBIASIO[90]	92		
AFE_CLKBIASIO[89]	93		
AFE_CLKBIASIO[91]	94		
AFE_SDA_SRC[0]	95	IN	AFE_SDA_SRC
AFE_SDA_SRC[1]	96		
AFE_SDA_SENSE[0]	97	OUT	AFE_SDA_SNS
AFE_SDA_SENSE[1]	98		
AFE_SCL_SRC[0]	99	IN/OUT	AFE_SCL_SRC
AFE_SCL_SRC[1]	100		

Table 16 - CCD AFE Board P2 Connector Assignments

Signal Name	Pin Num AFE1	Direction (relative to AFE)	CCD AFE Signal Name
AFE_VP80A	1	IN/PWR	AFE_VP80A
AFE_VP80A	2	IN/PWR	AFE_VP80A
AFE_GND	3	IN/PWR	AFE_GND
AFE_GND	4	IN/PWR	AFE_GND
AFE_VP180A	5	IN/PWR	AFE_VP180A
AFE_VP180A	6	IN/PWR	AFE_VP180A
AFE_GND	7	IN/PWR	AFE_GND
AFE_GND	8	IN/PWR	AFE_GND
AFE_VP300A	9	IN/PWR	AFE_VP300A
AFE_VP300A	10	IN/PWR	AFE_VP300A
AFE_GND	11	IN/PWR	AFE_GND
AFE_GND	12	IN/PWR	AFE_GND
AFE_VN80A	13	IN/PWR	AFE_VN80A
AFE_VN80A	14	IN/PWR	AFE_VN80A
AFE_GND	15	IN/PWR	AFE_GND
AFE_GND	16	IN/PWR	AFE_GND
AFE_VN180A	17	IN/PWR	AFE_VN180A
AFE_VN180A	18	IN/PWR	AFE_VN180A
AFE_VN300A	19	IN/PWR	AFE_VN300A
AFE_VN300A	20	IN/PWR	AFE_VN300A
AFE_SHIELD	21	IN/OUT	AFE_SHIELD
AFE_SHIELD	22	IN/OUT	AFE_SHIELD
RESERVED	23		
RESERVED	24		
RESERVED	25		
/WATCHDOG_FAIL	26	IN	~WATCHDOG_FAIL
AFE_PWRDATAIO[0]	27	OUT	AFE_DATA00
AFE_PWRDATAIO[18]	28		
AFE_PWRDATAIO[1]	29	OUT	AFE_DATA01
AFE_PWRDATAIO[19]	30		
AFE_PWRDATAIO[2]	31	OUT	AFE_DATA02
AFE_PWRDATAIO[20]	32		
AFE_PWRDATAIO[3]	33	OUT	AFE_DATA03
AFE_PWRDATAIO[21]	34		
AFE_PWRDATAIO[4]	35	OUT	AFE_DATA04
AFE_PWRDATAIO[22]	36		
AFE_PWRDATAIO[5]	37	OUT	AFE_DATA05
AFE_PWRDATAIO[23]	38		

Table 17 - CCD AFE Board P2 Connector Assignments (cont.)

Signal Name	Pin Num AFE1	Direction (relative to AFE)	CCD AFE Signal Name
AFE_PWRDATAIO[6]	39	OUT	AFE_DATA06
AFE_PWRDATAIO[24]	40		
AFE_PWRDATAIO[7]	41	OUT	AFE_DATA07
AFE_PWRDATAIO[25]	42		
AFE_PWRDATAIO[8]	43	OUT	AFE_DATA08
AFE_PWRDATAIO[26]	44		
AFE_PWRDATAIO[9]	45	OUT	AFE_DATA09
AFE_PWRDATAIO[27]	46		
AFE_PWRDATAIO[10]	47	OUT	AFE_DATA10
AFE_PWRDATAIO[28]	48		
AFE_PWRDATAIO[11]	49	OUT	AFE_DATA11
AFE_PWRDATAIO[29]	50		
AFE_PWRDATAIO[12]	51	OUT	AFE_DATA12
AFE_PWRDATAIO[30]	52		
AFE_PWRDATAIO[13]	53	OUT	AFE_DATA13
AFE_PWRDATAIO[31]	54		
AFE_PWRDATAIO[14]	55	OUT	AFE_DATA14
AFE_PWRDATAIO[32]	56		
AFE_PWRDATAIO[15]	57	OUT	AFE_DATA15
AFE_PWRDATAIO[33]	58		
AFE_PWRDATAIO[16]	59	OUT	AFE_DATA16
AFE_PWRDATAIO[34]	60		
AFE_PWRDATAIO[17]	61	OUT	AFE_DATA17
AFE_PWRDATAIO[35]	62		
AFE_PWRDATAIO[36]	63	IN	CDSBUS0
AFE_PWRDATAIO[37]	64	IN	CDSBUS1
AFE_PWRDATAIO[38]	65	IN	CDSBUS2
AFE_PWRDATAIO[39]	66	IN	CDSBUS3
AFE_PWRDATAIO[40]	67	IN	CDSBUS4
AFE_PWRDATAIO[41]	68	IN	CDSBUS5
AFE_PWRDATAIO[42]	69	IN	CDSBUS6
AFE_PWRDATAIO[43]	70	IN	CDSBUS7
AFE_PWRDATAIO[44]	71	IN	/AFE_CHANSLCT0
AFE_PWRDATAIO[52]	72		
AFE_PWRDATAIO[45]	73	IN	/AFE_CHANSLCT1
AFE_PWRDATAIO[53]	74		
AFE_PWRDATAIO[46]	75	IN	/AFE_CHANSLCT2
AFE_PWRDATAIO[54]	76		

Table 18 - CCD AFE Board P2 Connector Assignments (cont.)

Signal Name	Pin Num AFE1	Direction (relative to AFE)	CCD AFE Signal Name
AFE_PWRDATAIO[47]	77	IN	/AFE_CHANSLCT3
AFE_PWRDATAIO[55]	78		
AFE_PWRDATAIO[48]	79		
AFE_PWRDATAIO[56]	80		
AFE_PWRDATAIO[49]	81		
AFE_PWRDATAIO[57]	82		
AFE_PWRDATAIO[50]	83		
AFE_PWRDATAIO[58]	84		
AFE_PWRDATAIO[51]	85		
AFE_PWRDATAIO[59]	86		
AFE_PWRDATAIO[60]	87	IN	AFE_ADC_STB
AFE_PWRDATAIO[62]	88		
AFE_PWRDATAIO[61]	89		
AFE_PWRDATAIO[63]	90		
AFE_PWRDATAIO[64]	91	IN	AFE_DATA_STB
AFE_PWRDATAIO[66]	92		
AFE_PWRDATAIO[65]	93		
AFE_PWRDATAIO[67]	94		
AFE_PWRDATAIO[68]	95	IN	AFE_DATA_EN
AFE_PWRDATAIO[70]	96		
AFE_PWRDATAIO[69]	97		
AFE_PWRDATAIO[71]	98		
AFE_PWRDATAIO[72]	99	IN	AFE_WRT_CDS
AFE_PWRDATAIO[73]	100		