MONSOON

Torrent DHE Requirements Compliance Testing.

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Revision History

Version	Date Issued	Sections Affected	Remarks
2.0	06/03/2011 Moore	All	Document compiled on information contained in documents MNSN56.01.01, TRNT-AD-04-0001 rev 1.0, and TRNT-AD-11-0001rev 5.0
2.1	06/29/2011 Moore	All	Addition of tests – Details defined
2.2	07/06/2011 Moore	All	Added testing methods and comments
2.3	07/19/2011 Moore	All	Additional tests and details added after document discussion in Tucson. Added section 5.5.x for temperature control.
2.4	7/20/11 Hunten	Page 5	Inserted paragraph specifying acceptance of test results.
2.5	9/5/11 Moore	All	Draft release after completion of testing.

MONSOON Torrent Detector Head Electronics (DHE)

The Torrent hardware (Detector Head Electronics – DHE) is built from four major modules:

The Power Supply Module (PSM). This module generates all power supply requirements for the DHE. There is one fixed voltage digital supply, seven adjustable analog power supplies, and one adjustable detector heater power supply. All supplies are controlled and monitored by the digital control system. Primary power is from a small laptop brick supply.

The Local Control Board (LCB). This module contains all the required digital logic to support the functions of the DHE. It includes GIGe and Systran (FiberLink) high speed communications channels, power supply control and sequencing, temporal clock and cds sequencing for detector readout, clock and bias voltage control, and telemetry functions. Functionality is programmable through firmware that resides on a Xilinx Virtex 5 FPGA.

One or two Analog Front End modules (AFE). Up to two AFE boards can be supported in each DHE. These boards supply the required analog circuitry to develop clean clock and bias signals, process the detector analog signal, and perform analog to digital conversion on samples of the detector analog signals to provide telemetry. These boards are able to support both N and P channel CCD technology for either deep depletion or standard devices.

One Transition Module (TSM). This module transitions between the standard DHE Controller box (containing items 1,2, and 3 above) to the specific detector mounted in a dewar. The module is designed to bolt permanently to the detector dewar and supports electronics for wiring the detector for clocks and biases, the protection of the detector from static and accidental over voltage situations, the pre-amplifiers for the detector video signals, and the detector temperature sensing circuitry.

The design of the MONSOON Torrent DHE addresses the NOAO requirement to minimize the number of different detector controller technologies required to support NIR and CCD detectors. The DHE occupies a minimum of space on the instrument while supporting a wide range of detector technologies and configurations using one standard electronics box.

Special note of consideration is the support for both N and P-Channel Deep Depletion CCDs. In addition to the fact that all signals are inverted in polarity between the N and P types, there is an additional high-voltage bias applied to the backside of the device to repel ‘charge’ from the backside surface. This is an opposite polarity potential to the principle biases used for the output stage and must be considered in the design.

Detector Device (CCD) Interface Parameters

Detector technology should be the limiting system performance parameter for this system. A formal analysis and requirements flowdown to the interface electronics has been performed based on the most optimistic and demanding CCD performance parameters based on the current and anticipated state-of-the-art in scientific CCDs. These include devices from Lincoln Labs, E2V, and STA.

Current devices have broken the 1e- readnoise barrier at slow scan rates of 20Khz, with the same devices typically performing at the 5e- readnoise at 1Mhz rates. Typical performance numbers are in the 3-5 e- readnoise at the 100KHz rate. These devices have high-gain output stages with gains ranging from 10-15uv/e- for LL, 3-6uV/e- for E2V, to 1-5uV/e- for the STA devices. Fullwell capacities are well in excess of 100ke- and the need for greater than 16-bit dynamic range for numerous applications, particularly spectroscopy, is already upon us. Spatial fidelity is key, MTF concerns should not be overlooked, so pixel to pixel crosstalk, and channel to channel crosstalk issues must be addressed as well as readnoise, dynamic range and linearity. In order to meet these requirements sufficient bandwidth in the acquisition channel will need to be provided for adequate settling chahracteristics.

The requirements for the design are taken from the NOAO Document TRNT-AD-11-0001 version 5.0. The original version of this document was titled 'Requirements for a generic MONSOON replacement CCD controller'. The document was later renamed to be 'TORRENT DHE Architecture'

This document maps the requirements from TRNT-AD-11-0001 version 5.0 to the actual performance of pre-production DHE hardware to assess the level of compliance by the hardware, firmware, and software design to the requirements of the observatory. Since the hardware does not have any provision for adjustment of calibration, testing strategies have been developed to test the level of compliance of the design of the hardware (i.e. test the ability of the hardware design to comply to the requirements). Once the design has been shown to comply to the performance requirements, any board that is built with that design will be capable of the required performance. Testing of the Torrent production hardware becomes simplified to testing only the functionality of the hardware to assure correct manufacture, and should not require the performance of each piece of hardware to be tested since it is inferred by the design.

These performance and functional requirements, and the result matrix of testing to compliance are shown in the following tables. Please note that at this time that the order in which these tests are performed has not been optimized. In addition the list may still be incomplete and there may be redundency in them. Future versions of this document will address these shorcomings.

Torrent Acceptance

Using this document, the Torrent project will be performing tests that will lead to acceptance of the project and the move from Development to Production. This report will include a one page executive summary and a complete write-up covering what passed and what did not meet specification. The report will specify the test procedure and the results.

One section will cover items that do not meet specification due to not being finished, such as the buffer memory and another section items that only need a component tweak, such as the regulator on the AFE board to get higher V_{HV}.

The report will be sent to David Sprayberry, Torrent project sponsor, Abi Saha, KPNO director, and Chris Smith, CTIO director, for approval. The assigned recipients are free to reassign their approval responsibilities to some other person.

What the Torrent project expects from the review of the completed Compliance Report is an approval to go forward with the production run of 20 total systems. The Torrent project will then proceed to procure the remainder of the required parts and assemblies ordered or in house by the end of FY2011.

4. Generic qualities:

Requirement 4.1	The application of the controller to specific functionality shall be through selection of a board suite, hardware configuration, and 'runtime' configuration options.
Specification	Minimize hardware configuration options to minimize spare compatibility issues.
Goal	Eliminate hardware configuration options to eliminate spare compatibility issues.
Test method	By design.
Compliance	**Fail**
Comment	1. No IR capability as is specified in TRNT-AD-11-0001 version 5.0 section 4.1.4. 2. All detector and application specific hardware option settings now reside in the Transition module (TSM) which is the fixed portion of the DHE relative to the detector.
Suggestion	Implement IR capability.
Notes	

Requirement 4.2	The cost to purchase shall be consistent to the required capabilities i.e. cost should scale with number of video channels, etc.
Specification	Baseline manufacturing parts cost for a four channel VIS system is $10k
Goal	Baseline assembled and tested cost for a four channel VIS system is $10k
Test method	Total the parts cost for one of the design validation DHE's.
Compliance	**Pass**
Comment	Torrent Project Manager estimates the DHE cost to be under $10K. Actual verified cost of assembly and mechanical components is $7751.00. Estimated cost of electronic components and parts is <$2249.00. Together these = $10K. Per M. Hunten email 8/8/11.
Suggestion	Get a better idea of the cost of a DHE.
Notes	

Requirement 4.3	The controller hardware will be compatible with existing Pixel Acquisition Node (PAN) hardware and software.
Specification	100% Compliance
Goal	100% Compliance + capabilities for self configuration and calibration
Test method	Verified with existing PAN software MecStart command and DHE checkout.
Compliance	**Pass**
Comment	
Suggestion	
Notes	Used tom_pcm code on ctiola to test this with the existing PAN software.

Requirement 4.4	Support for card serial numbers, self-configuration, and self-calibration using expanded NOAO software suite.
Specification	Manual system with operator intervention
Goal	Automated system without operator intervention
Test method	By design / Verified by testing self-configuration and SN support.
Compliance	**Partial Pass**
Comment	Mezzanine and Preamplifier modules do not have serial numbers.
Suggestion	
Notes	Collector now working well. Self-configuration and self-calibration operational.

Requirement 4.5	Support for comprehensive telemetry sensing
Specification	All power supply, clock, bias, and reference voltages
Goal	All power supply, clock, bias, and reference voltages and currents
Test method	See Requirement 5.3.7 Test method
Compliance	**Partial Pass**
Comment	See Requirement 5.3.7 Comments
Suggestion	
Notes	

Requirement 4.6	Support for card temperature sensing
Specification	All modules with one temperature sensor
Goal	All modules with two temperature sensors to measure hottest and coldest areas of the module
Test method	Verify Temperature readout for each module (one sensor or two).
Compliance	**Partial Pass**
Comment	Mezzanine & preamplifier modules do not have temperature sensing.
Suggestion	Evaluate the need/benefit of mezzanine & preamplifier temperature sensing.
Notes	

5. Specific hardware capabilities – All Detectors:

Requirement 5.1.1	Sequencer control : Timing resolution
Specification	25 ns.
Goal	10 ns
Test method	Measure the difference between two clocks after adding one system clock delay using a NOP in ucode.
Compliance	**Fail**
Comment	One system clock delay is 37ns.
Suggestion	
Notes	Sequencer code required for this test. Found that a DSC =1 instruction actually takes two system clocks.

Requirement 5.1.2	Sequencer control : Timing jitter
Specification	2 ns.
Goal	Un-measurable
Test method	Measured using TSM clock output signal and AFE board CDS signal
Compliance	**Partial Pass (~5ns very close to spec.)**
Comment	Measured on Chile1 and Chile2 is 5ns within a 9ms accumulative period.
Suggestion	
Notes	Sequencer code required for this test

Requirement 5.1.3	Sequencer control : Pattern memory store size
Specification	> 1000 pattern values.
Goal	> 2000 pattern values.
Test method	Verified using ppxpass write and read commands to beginning and end addresses of sequencer pattern memory.
Compliance	**Pass**
Comment	2048 32 bit address locations in pattern memory. Goal met.
Suggestion	
Notes	

Requirement 5.1.4	Sequencer control : Sequencer code store size
Specification	> 1000 code values.
Goal	> 2000 code values.
Test method	Verified using ppxpass write and read commands to beginning and end addresses of sequencer program memory.
Compliance	**Pass**
Comment	1024 16 bit addresses of sequencer program memory.
Suggestion	
Notes	

Requirement 5.2.1	PAN ⇔ DHE communications :
Specification	Serial FPDP fiber port @ 1.0625 Gbps (Systran compatible).
Goal	N/A
Test method	By connectivity demonstration to SL100 in PAN computer.
Compliance	**Pass**
Comment	
Suggestion	
Notes	

Requirement 5.2.2	PAN ⇔ DHE communications : Ethernet with TCP/IP
Specification	100/1000BaseT Basic pixel server using UDP packets
Goal	100/1000BaseT with full duplex control using an industry standard protocol
Test method	
Compliance	**Fail**
Comment	As yet not fully supported in firmware
Suggestion	
Notes	

Requirement 5.2.3	PAN ⇔ DHE communications : Onboard image buffer. 256Mbytes capable of storing 2 x 8k x 4k pixel arrays @ 18-bit precision
Specification	Function as pixel data stream FIFO buffer.
Goal	Function as FIFO, backup raw image store, or as descrambled image store with science and quick look data read capabilities.
Test method	
Compliance	**Fail**
Comment	As yet not supported in firmware or software
Suggestion	
Notes	

Requirement 5.3.1	Auxiliary Functions : Support for shutter control via optical isolated open collector output.
Specification	One output port
Goal	N/A
Test method	Shutter or DPDT relay to simulate shutter. (DPDT relay used)
Compliance	**Pass verified with sequencer**
Comment	
Suggestion	Make a drawing for the pin-out of the shutter connector that graphically shows the pin 1 – 8 locations on the Lemo shutter connector. This drawing is to be delivered with every system as part of the document package.
Notes	

Requirement 5.3.2	Auxiliary Functions : Two optically isolated inputs for shutter position monitor function.
Specification	Provide simple feedback to sequencer concerning shutter status
Goal	Provide simple feedback to sequencer concerning shutter status and measure shutter open and close times.
Test method	Shutter or DPDT relay to simulate shutter. (DPDT relay used)
Compliance	**Pass verified with sequencer**
Comment	Open and close times not working.
Suggestion	
Notes	

Requirement 5.3.3	Auxiliary Functions : Support for pre-flash led control via optical isolated current source output.
Specification	Output port without current source
Goal	Output port with controllable current source
Test method	Drive a standard LED
Compliance	**Partial Pass (Did not work correctly with the sequencer)**
Comment	Preflash functionality under sequencer control does not allow preflash to be switched off. Manual control functions correctly.
Suggestion	
Notes	Simple firmware bug that defeats turning off the preflash

Requirement 5.3.4	Auxiliary Functions : Support for single channel temperature control with set point control via DAC and linear current sink output @ max 5 Watts.
Specification	1^{o} measurement resolution and 2^{o} control stability
Goal	0.1^{o} measurement resolution and 0.5^{o} control stability
Test method	Mounted 2 x 20 Ohm resistors to plate together with 1N918 temp sense diodes.
Compliance	**Partial pass**
Comment	Temperature measurement exceeds specification but controlled temperature stability is compromised by servo instability. Control oscillation is approx. 3 Degrees.
Suggestion	Improve servo
Notes	

Requirement 5.3.5	Auxiliary Functions : Maximum heater power shall be limited by user option to provide a safe limit for the detector.
Specification	Safety limit demonstrated at set point values of 0.5, 1, 2, 4, and 8 Watt.
Goal	N/A
Test method	Manually ramp up heater control with limiter set to various levels using a 40 Ohm load. Measured values corrected for 35 Ohm load values.
Compliance	**Partial Pass**
Comment	Safety limit functions but calibrated limit is higher than expected by between 17% to 20% (in lower ranges).
Suggestion	Re-calculate limiter resistor values.
Notes	See spreadsheet ‘heater properties.xls’

Requirement 5.3.6	Auxiliary Functions : Ability to isolate all clock and bias signals from detector via electronic switches. Detector safety interlock on principle power supply availability and health.
Specification	As per requirement
Goal	N/A
Test method	Isolation verified via direct measurement of clocks in both switch states. Safety interlock verified via direct scope measurement of clock and bias signals triggered by /power_good when AC power is removed. Additional verification of remote power on circuit.
Compliance	**Pass**
Comment	26mS for bias to react. 600uS for clocks to react.
Suggestion	
Notes	

Requirement 5.3.7	Auxiliary Functions : Voltage telemetry data functions for all clocks, biases, video offsets, power supply voltages, and references.
Specification	
Goal	
Test method	Verify actual telemetry read-back against hardware design for Voltage telemetry on all clocks, biases, power supply voltages, and references. For the offsets - take image frames with an initial offset of 2080 and 2100. Measure pixel values for each frame and verify the level changed proportionately.
Compliance	**Partial Pass**
Comment	AFE VN50 does not read (- offscale). AFE +10V and -10V are supported in the hardware design but are not read out in the current configuration.
Suggestion	See observation note 12.
Notes	Pixel values increase 25ADU per count of offset.

Requirement 5.3.8	Auxiliary Functions : Temperature control output current monitor.
Specification	
Goal	
Test method	
Compliance	**Pass**
Comment	Heater voltage and current telemetry is effective if calibrated.
Suggestion	
Notes	

Requirement 5.3.9	Auxiliary Functions : Telemetry data function for temperature control
Specification	One channel with 10µa current source for diode sensor.
Goal	Two channels with 10/50µa current sources for diodes or PT100 sensors.
Test method	Partially by design (one or two channels) and partially by measuring current sources.
Compliance	**Pass**
Comment	
Suggestion	
Notes	

Requirement 5.3.10	Auxiliary Functions : Detection for PAN disconnect with detector idle protection plan.
Specification	As per requirement
Goal	N/A
Test method	
Compliance	**Partial pass**
Comment	No plan for what to do in the event of a PAN disconnect has been developed (yet). Loss of PAN communication link is detected by currently not used.
Suggestion	
Notes	

Requirement 5.3.11	Auxiliary Functions : Detector protection during un-programmed power down event
Specification	No bias or clock rail to exceed 2.0 volts potential during these events
Goal	No bias or clock rail to exceed 0.0 volts potential during these events
Test method	Removal of power while monitoring bias and clock rails with scope, power removal triggered. See section 5.3.6 for more info.
Compliance	**Pass**
Comment	
Suggestion	
Notes	

Requirement 5.3.12	Auxiliary Functions : Detector protection during DHE Controller removal.
Specification	TSM Preamp GND pins shall be connected to Chassis when DHE controller is removed.
Goal	N/A
Test method	Removal of controller while monitoring clock and bias outputs with a scope Triggered on a psm output..
Compliance	**Pass**
Comment	Very nice and safe with no glitches positive or negative.
Suggestion	
Notes	

Requirement 5.4.1	Power, size, and weight : DHE Primary voltage supply
Specification	External inline 24VDC 60W Medical grade power supply.
Goal	N/A
Test method	Validate manufactures data sheet for leakage current specification OR measure current from DC outputs to AC GND with a meter.
Compliance	**Pass**
Comment	Model SPU60-108 datasheet does not specify output leakage current. Measurements show output leakage current to be <100 µa to AC GND pin.
Suggestion	
Notes	Supply output ground leakage value < 100 µa to AC GND pin

Requirement 5.4.2	Power, size, and weight : DHE Power dissipation
Specification	Less than 24 Watts average consumption for minimum (4 video channel) system.
Goal	Less than 30 Watts average consumption for maximum (8 video channel) system.
Test method	Measure 24Vdc input power on a fully loaded and configured 1 & 2 AFE DHE system.
Compliance	**Fail**
Comment	8 video channel system measures 37W. 4 video channel system measures 25.1W.
Suggestion	
Notes	

Requirement 5.4.3	Power, size, and weight : DHE size: As small as possible consistent with packaging and sufficient power dissipation factors.
Specification	190mm x 130mm x 300mm (7410 cm^3)
Goal	160mm x 110mm x 200mm (3520 cm^3)
Test method	Measure and record the dimensions and cubic volume of the DHE.
Compliance	**Fail**
Comment	Measures 195mm X 149.25mm X 313.69mm (9129.55 cm^3)
Suggestion	
Notes	

Requirement 5.4.4	Power, size, and weight : DHE weight
Specification	As light as possible consistent with ruggedness for deployment.
Goal	N/A
Test method	Measure and record the weight of the DHE. Evaluate for Ruggedness and ingress protection.
Compliance	**Pass**
Comment	DHE weighs in at 5.587 Kg or 12.31lbs. and is strongly made and capable of withstanding rough handling. Evaluated for Ingress Protection the Torrent DHE would rate IP50. (e.g. dust tight but not water protected.)
Suggestion	
Notes	

Requirement 5.5.1	DHE operating environment. Ambient temperature and humidity.
Specification	The operating temperature range of the DHE electronics shall be between -10° C. to +35° C. 15% to 90% non-condensing humidity.
Goal	N/A
Test method	Operate the DHE electronics in an environmental test chamber at the extents of all the specified combination temperature and humidity ranges.
Compliance	
Comment	Must be conducted in Tucson small enviro chamber.
Suggestion	
Notes	

Requirement 5.5.2	DHE operating environment. Internal temperature control
Specification	The internal operating temperature of the DHE electronics shall be actively controlled to remain constant to an accuracy of 2° C. during a change of 20° C. in ambient temperature.
Goal	N/A
Test method	Operate the DHE electronics in an environmental chamber while recording the internal temperature (FPGA temperature). Change the ambient temperature by 20° C. and evaluate the active control of the internal temperature for accuracy.
Compliance	
Comment	Must be conducted in Tucson small enviro chamber.
Suggestion	
Notes	As measured on the hottest point of the controller i.e. the internal FPGA temperature.

Requirement 5.5.3	DHE operating environment. Internal temperature of electronics
Specification	The internal operating temperature of the DHE electronics shall be operated at a temperature of 20 ^{o} C. above the maximum expected ambient temperature (+35^{o} C.).
Goal	The internal operating temperature of the DHE electronics shall be operated at a temperature of 10 ^{o} C. above the maximum expected ambient temperature (+35^{o} C.).
Test method	Operate the DHE electronics in an environmental chamber with the temperature at the maximum expected ambient (+35^{o} C.) while recording the internal temperature (FPGA temperature). Evaluate the temperature difference between ambient and internal.
Compliance	
Comment	Must be conducted in Tucson small enviro chamber.
Suggestion	
Notes	As measured on the hottest point of the controller i.e. the internal FPGA temperature.

6. Specific hardware capabilities – VIS Detectors:

Requirement 6.1.1	Video input (N and P Channel CCD) : Number of input channels
Specification	4 or 8 in increments of 4.
Goal	N/A
Test method	By design
Compliance	**Pass**
Comment	
Suggestion	
Notes	All specifications in this section apply to 8 video channels being read out simultaneously.

Requirement 6.1.2	Video input (N and P Channel CCD) : Sensitivity of input channels
Specification	0.5 µVolt => 10.0 µVolt / ADU
Goal	N/A
Test method	Take data set at 2uS dwell and 4uS dwell to establish gain & gain change of input. Extrapolate reasonable dwell times to the specification.
Compliance	**Pass**
Comment	Tested both Chile1 and Chile2 channels 1 & 2. Performance was Good. Very consistent between channels and between controllers.
Suggestion	
Notes	Dataset and spreadsheet exist to support these results.

Requirement 6.1.3	Video input (N and P Channel CCD) : Video input type.
Specification	Single ended AC coupled with characteristic source impedance termination.
Goal	N/A
Test method	By Design
Compliance	**Pass**
Comment	
Suggestion	
Notes	

Requirement 6.1.4	Video input (N and P Channel CCD) : Video input bandwidth.
Specification	Better than 1db response between 50KHz and 26MHz
Goal	N/A
Test method	Sine wave stimulus and direct measurement of -3dB point.
Compliance	**Pass**
Comment	The complete bandwidth does not need to be available on each TSM. However, the design must allow for a smaller bandwidth to be used with a flat response between these limits.
Suggestion	
Notes	This allows for a 16-bit accuracy response. The Preamplifier has a 15pf cap in the feedback which bandwidth limits it to 11Mhz. Video circuitry has a bandwidth of 9Mhz but has a peak @4Mhz. This peak will effect linearity and is 23% @4Mhz.

Requirement 6.1.5	Video input (N and P Channel CCD) : Controller noise contribution
Specification	< 8uV rms input referred @ 200Kpix/chan/sec
Goal	< 4uV rms input referred @ 100Kpix/chan/sec
Test method	2K Ohm source impedance and 2 µVolt / ADU gain.
Compliance	**Fail**
Comment	Front end @ 2us dwell is a gain of 2.58uV/ADU @ 4uS dwell is a gain of 1.24uV/ADU. Measured noise was 7.1 ADU. At 2uS dwell the measured noise is 18.32uV rms @84Kpix/chan/second. Additional noise tests were performed with the CDS circuit components held in various configurations. The results of these tests were: Clamp, common mode, with int =1.96 ADU or 5.068uV Clamp, Non-inverted, with int = 3.3 ADU or 8.514uV Clamp, Double integration = 4.46 ADU or 11.5uV
Suggestion	
Notes	This corresponds to 4 and 2 bits rms for the specification and goal values.

Requirement 6.1.6	Video input (N and P Channel CCD) : Conversion dynamic range
Specification	18-bit with no missing codes.
Goal	N/A
Test method	By design
Compliance	**Pass**
Comment	
Suggestion	
Notes	

Requirement 6.1.7	Video input (N and P Channel CCD) : Maximum conversion rate
Specification	500 KPix/channel/sec.
Goal	N/A
Test method	Serial readout as far as possible consistent with reliable acquisition.
Compliance	**Pass**
Comment	At 547KPix/channel/second the noise is 13.47 ADU or 34.75uV.
Suggestion	
Notes	

Requirement 6.1.8	Video input (N and P Channel CCD) : Linearity across system dynamic range
Specification	< 0.1% (260 ADU in a 0.525v range applied at input)
Goal	< 0.01% (26 ADU in a 0.525v range applied at input)
Test method	
Compliance	
Comment	This requirement was not part of the original document
Suggestion	
Notes	

Requirement 6.1.9	Video input (N and P Channel CCD) : Channel to channel crosstalk
Specification	< 0.01%
Goal	unmeasurable
Test method	Inject a synthetic step into channel 1 and observe offset shift in channel 2. Channel 2 is terminated in 2K Ohms. Synthetic shift created from clock 12 with divider network of 75K / 200 Ohms.
Compliance	**Fail**
Comment	This requirement was not part of the original document
Suggestion	
Notes	Measured 0.14% xtalk (33 ADU xtalk from 23,733 ADU step)

Requirement 6.1.10	Video input (N and P Channel CCD) : Pixel to pixel crosstalk
Specification	< 0.01%
Goal	unmeasurable
Test method	Inject two synthetic steps into serial read process. Critically tune to avoid clock dac settling time, observe effects in adjacent pixels. Step size is Approx. 24K ADU.
Compliance	**Pass** - Unmeasurable
Comment	This requirement was not part of the original document
Suggestion	
Notes	

Requirement 6.2.1	Clock voltage output (N and P Channel CCD) : Number of clocks
Specification	16 per 4 video inputs in 4 groups of 4.
Goal	N/A
Test method	By design
Compliance	**Pass**
Comment	
Suggestion	
Notes	

Requirement 6.2.2	Clock voltage output (N and P Channel CCD) : Clock voltage range
Specification	± 15V swing @ 30 ma peak.
Goal	
Test method	Into a 100pf shunted by 2K Ohm equivalent load.
Compliance	**Pass**
Comment	
Suggestion	
Notes	

Requirement 6.2.3	Clock voltage output (N and P Channel CCD) : Clock voltage setting resolution: 12 bits.
Specification	12-bits resolution
Goal	14-bits resolution
Test method	By Design
Compliance	**Pass**
Comment	
Suggestion	
Notes	

Requirement 6.2.4	Clock voltage output (N and P Channel CCD) : Clock 90% swing rise/fall time
Specification	Maximum 70 ns monotonic rise and fall
Goal	Minimum 70 ns with adjustable slope.
Test method	Into a 100pf shunted by 2K Ohm equivalent load.
Compliance	**Pass**
Comment	40 – 50 ns rise / fall time
Suggestion	
Notes	

Requirement 6.2.5	Clock voltage output (N and P Channel CCD) : Max ripple, overshoot and noise:
Specification	Ripple and noise < 5 mv.
Goal	N/A
Test method	Into 100pf shunted by 2K Ohm equivalent load.
Compliance	**Pass**
Comment	Critical damped to limit overshoot to < 0.01% of pk-pk value. Clock noise measured using the video input and subtracting the bias level noise from an adjacent channel with the same source impedance (2K). Clock noise measures 794uV using this technique.
Suggestion	
Notes	

Requirement 6.2.6	Clock voltage output (N and P Channel CCD) : Clock rails must power up disabled.
Specification	As per requirement
Goal	N/A
Test method	Trigger from TSM present switch clock and energize the DHE while measuring clock rails.
Compliance	**Pass**
Comment	
Suggestion	
Notes	

Requirement 6.2.7	Clock voltage output (N and P Channel CCD) : Clock rail cross talk (Clock transition of 90% of dynamic range)
Specification	Less than 10mv cross talk levels between any two clock transitions
Goal	Immeasurable
Test method	Set one clock to +/-.5V and an adjacent clock to +/-15V and measure the crosstalk on the lower voltage clock for worst case.
Compliance	**Partial Pass (adjacent channels show 100mV of cross talk, 2 channels**

	away have no crosstalk)
Comment	Needs to be evaluated better.
Suggestion	
Notes	

Requirement 6.2.8	Clock voltage output (N and P Channel CCD) : Clock rail cross talk (Clock transition of 90% of dynamic range)
Specification	Less than 10mv cross talk levels change when all other clock signals transition.
Goal	Immeasurable
Test method	Set and measure one (a) clock level and move all other (n) clocks from one rail to the other rail. Measure the level change of the first (a) clock.
Compliance	**Fail**
Comment	(a) clock measured 20mV of change when all others were moved full span.
Suggestion	
Notes	

Requirement 6.3.1	Bias voltage output (N and P Channel CCD) : Number of biases
Specification	16 per 4 video inputs in 4 groups of 4.
Goal	N/A
Test method	By Design
Compliance	**Pass**
Comment	
Suggestion	
Notes	

Requirement 6.3.2.1	Bias voltage output (N and P Channel CCD) : Bias voltage ranges: Low Voltage Biases:
Specification	± 15V@ 25ma.
Goal	N/A
Test method	Into 1000pf shunted by 5K Ohm equivalent load.
Compliance	**Fail**
Comment	Positive rail will only source ~16mA. Negative rail OK. This is a feature of the OP285.
Suggestion	
Notes	

Requirement 6.3.2.2	Bias voltage output (N and P Channel CCD) : Bias voltage ranges: High Voltage Biases:
Specification	Unipolar 0 Volts to +30 Volts @ 25mA or -30 Volts to 0 Volts @ 25 mA.
Goal	N/A
Test method	Into 1000pf shunted by 5K Ohm equivalent load.
Compliance	**Fail**
Comment	
Suggestion	
Notes	

Requirement 6.3.2.3	Bias voltage output (N and P Channel CCD) : Bias voltage ranges: Backside Bias Voltage:
Specification	Unipolar 0 Volts to +/-75 Volts @ 5mA. Polarity opposed to high voltage biases.
Goal	N/A
Test method	Into 1000pf shunted by 56K Ohm equivalent load.
Compliance	**Partial Pass**
Comment	Servo loop oscillates in both polarities. Voltage output is in spec., Maximum current at 15Kohm load is 1mA.
Suggestion	
Notes	

Requirement 6.3.3	Bias voltage output (N and P Channel CCD) : Bias voltage setting resolution:
Specification	12-bits resolution
Goal	14-bits resolution
Test method	By design
Compliance	**Pass**
Comment	
Suggestion	
Notes	

Requirement 6.3.4	Bias voltage output (N and P Channel CCD) : Max ripple, overshoot and noise:
Specification	0.001% of value or 20 µVolts rms.
Goal	N/A
Test method	Into 1000pf shunted by 5KOhm or 50KOhm (Vbb) equivalent load.
Compliance	**Pass**
Comment	Bias noise measured using the video input and subtracting the bias level

	noise from an adjacent channel with the same source impedance (2K). LV Bias noise measures 51uV using this technique. HV Bias noise measures 15.48uV. Vbb measures 105.78uV.
Suggestion	
Notes	

Requirement 6.3.5	Bias voltage output (N and P Channel CCD) : Bias voltages must power up disabled.
Specification	As per requirement
Goal	N/A
Test method	
Compliance	**Pass**
Comment	Trigger from TSM present switch clock and energize the DHE while measuring LV and HV bias rails.
Suggestion	
Notes	

7. System demonstration tests:

These tests are not derived from specific requirements but rather designed to demonstrate the performance of the equipment under real operating conditions using a detector with known characteristics.

Requirement 7.1.1	Demonstration test: Temporal : Time to read out, store image and display QL image (2k x 4k image using two video channels)
Specification	Less than 15 seconds.
Goal	Less than 10 seconds.
Test method	Using 5 second bias and measured from beginning of readout at 251 Kpix/chan/sec.
Compliance	**Partial pass – 19 seconds to display image**
Comment	The performance is limited by the capacity of the detector to shift parallel charge.
Suggestion	
Notes	

Requirement 7.1.2	Demonstration test: Temporal : Latency between two consecutive one second integrations using full readout
Specification	Less than 15 seconds.
Goal	Less than 10 seconds.
Test method	Using two one second biases and measuring from the beginning of the first readout to the beginning of second readout and subtracting the readout time (19 seconds). This should equal the system latency.
Compliance	**Pass – zero seconds system latency**

Comment	immeasurable by eye
Suggestion	
Notes	

Requirement 7.1.3	Demonstration test: Temporal : Time to warm boot MONSOON system, power on DHE and begin the first integration
Specification	Less than 20 seconds.
Goal	Less than 15 seconds.
Test method	
Compliance	**Fail – 2 minutes**
Comment	Consider the specification too severe.
Suggestion	
Notes	

Requirement 7.1.4	Demonstration test: Temporal : Time to cold boot PAN, load PAN software, power on DHE and begin the first integration
Specification	Less than 5 minutes.
Goal	Less than 2 minutes.
Test method	
Compliance	**Pass**
Comment	Approx. 4 minutes to boot LINUX, 1 minute to load Pan sw y connect
Suggestion	
Notes	Using Centos 2.6.18 running on a Dell Power Edge 2850 machine

Requirement 7.1.5	Demonstration test: Temporal : Time to bring DHE down, make the detector safe, change DHE controller module, and bring the system back up ready for first integration.
Specification	Less than 5 minutes.
Goal	Less than 2 minutes.
Test method	Shutdown, changed chile1 controller for chile2, power up, reboot, run integration and check for image quality.
Compliance	**Fail**
Comment	Requires collect process to be fully functional – 9 Minutes required to complete test
Suggestion	The specification is too restrictive. 10 minutes is probably less time to complete a controller change than any other controller in the world.
Notes	This test emulates a field replacement operation of the DHE controller. Therefore, the DHE needs to be operational after the swap.

Requirement 7.2.1	Demonstration test: Noise: Total noise in image during test 7.1.1
Specification	Less than 7 –e rms.
Goal	Less than 4 –e rms.
Test method	
Compliance	**Partial Pass**
Comment	Total noise approx. 12 & 17 ADU in the two channels which calculates to 6 and 8 e- rms respectively. Of this the controller is contributing the approx. half of the noise i.e. 4e- rms. This data taken at 168 Kpix/chan/sec – not at the 251 Kpix/chan/sec used in test 7.1.1
Suggestion	
Notes	

Requirement 7.2.2	Demonstration test: Noise: Lowest demonstrable white noise on detector
Specification	Less than 4e- rms.
Goal	Less than 2e- rms.
Test method	
Compliance	**Not tested.**
Comment	Attempts to reduce noise where not carried out.
Suggestion	
Notes	

Requirement 7.2.3	Demonstration test: Noise: Sporadic noise components
Specification	Less than 7e- peak with less than 0.001% of pixels
Goal	Immeasurable
Test method	Measured std dev across active image areas while looking for excursions of > 20 ADU rms.
Compliance	**Pass**
Comment	Test method is somewhat basic and not very comprehensive.
Suggestion	
Notes	Some pattern noise in images which makes analysis difficult.

Requirement 7.3.1	Demonstration test: Stability: Bias level stability short term.
Specification	Less than 1e- equivalent in one readout.
Goal	Less than 0.5e- equivalent in one readout.
Test method	
Compliance	**Fail**
Comment	Measured delta of 8 ADU along column using 40x100 averaging box at y=100 and y=3900. At 2.65uv / ADU and 6uv/e- detector sensitivity this equates to 3.5 e- delta. However, this value is not stable (i.e there are variations from frame to frame) so these measurements may be

	measuring low frequency noise rather than electronic drift. This is confirmed by looking at the histograms for the data at the two measurement points.
Suggestion	
Notes	

Requirement 7.3.2	Demonstration test: Stability: Bias level stability medium term.
Specification	Less than 3e- equivalent in eight hours continuous operation.
Goal	Less than 1e- equivalent in eight hours continuous operation.
Test method	Comparison between two zero second bias frames taken 17 hours apart.
Compliance	**Fail**
Comment	Average of 23 ADU difference equivalent to 10 e-. Controller temperature was within 1 Deg. between the two integration sets.
Suggestion	
Notes	

Requirement 7.3.3	Demonstration test: Stability: Bias level stability over 20^{o} C. temperature change.
Specification	Less than 3e- equivalent.
Goal	Less than 1e- equivalent.
Test method	
Compliance	
Comment	
Suggestion	
Notes	Environmental chamber is necessary for this test.

Requirement 7.4.1	Demonstration test: Image Quality: Maximum residual in two sequential pixels i.e. pixel to pixel cross talk.
Specification	Less than 0.1% at 50% dynamic range
Goal	Immeasurable
Test method	Basic inspection of cosmic ray events.
Compliance	**Pass.**
Comment	
Suggestion	
Notes	Pixel value excursions did not reach the 50% of dynamic range as specified.

Requirement 7.4.2	Demonstration test: Image Quality: Maximum residual in two adjacent video channels i.e. channel to channel cross talk.
Specification	Less than 0.1% at 50% dynamic range
Goal	Immeasurable

Test method	Image analysis using the cosmetics apparent in one channel and compared to the other.
Compliance	**Fail**
Comment	Definitely more than specification – Measured 6% but this result was affected by the noise contribution.
Suggestion	
Notes	Pixel value excursions did not reach the 50% of dynamic range as specified.

Requirement 7.5.1	Demonstration test: Acquisition modifiers: Pixel binning
Specification	Pixel binning in X and Y axis with fixed 2, 4, 8, binning factors
Goal	Pixel binning in X and Y axis with any integer binning factor
Test method	
Compliance	**Fail**
Comment	See observation 25
Suggestion	
Notes	

Requirement 7.5.2	Demonstration test: Acquisition modifiers: Region of interest
Specification	One region of interest within detector image area
Goal	Multiple regions of interest within detector image area
Test method	Verify ROI support with PAN software designer, if supported take an ROI image.
Compliance	**Fail**
Comment	PAN software does not currently support ROI per N. Buchholz email 8/16/11.
Suggestion	
Notes	

Requirement 7.5.3	Demonstration test: Acquisition modifiers: FIFO image buffer
Specification	Capable of buffering a complete 4k x 4k image
Goal	Capable of buffering multiple 4k x 4k images
Test method	
Compliance	**Fail**
Comment	Not fully supported in firmware – debugging required
Suggestion	
Notes	

Requirement 7.5.4	Demonstration test: Acquisition modifiers: Descrambler image buffer
Specification	Capable of descrambling a two channel 2k x 4k image
Goal	Capable of descrambling a four channel 4k x 4k image
Test method	
Compliance	**Fail**
Comment	Requires image buffer to work (test item 5.2.3)
Suggestion	
Notes	

Requirement 7.5.5	Demonstration test: Acquisition modifiers: Pause integration
Specification	Capable of pausing an active integration and then returning to normal integration mode without effecting system stability.
Goal	N/A
Test method	
Compliance	**Pass**
Comment	
Suggestion	Use 120 second pause time to check compliance
Notes	

Requirement 7.5.6	Demonstration test: Acquisition modifiers: Abort image acquisition
Specification	Capable of aborting an integration and returning to idle mode without effecting system stability
Goal	N/A
Test method	
Compliance	**Pass**
Comment	Abort reactions should be stable when aborted during readout or during integration.
Suggestion	
Notes	

Observations:

1.) Failures and Sparing –

Although the repair concept for the Torrent DHE removes the need to troubleshoot a failed controller to a board or component level on site instead replace it with a spare controller, the issue of repairing the failed controllers should be fully addressed. The failed controller will have to be troubleshot to the board level, and the failed board will have to be troubleshot to the component level for repair and restoration of these “ready spare controllers”.

The 'LCB/AFE/Utility & Controller' test will diagnose a failed controller to the board or interconnect level in most cases but will not diagnose the identified failures to a component level. Technical expertise and time consuming component level troubleshooting will be required to identify and replace failed components on a board.

There is currently no plan to spare the boards and cable harnesses that make up a controller. Failed controllers will not be returned until the component level diagnosis and repair is complete, leaving the observatory without a "ready spare controller". One way to get around this issue would be to maintain an inventory of "ready spare boards" at the controller repair depot. These spares could then be used to repair and restore a failed controller back into service in a quick manner, leaving the component level troubleshooting and repair to be done later.
Once the component level board repair is completed, the board goes into the inventory of "ready spares boards" as a replacement for the board that was removed and used to repair the failed controller.

2.) -sysConfig

Using sysConfig –sysName chile1 OR SysConfig –fclPlane chile1 results in sysConfig loading but does not display the connections and assignments.

3.) – DHE Arrival & inspection

The DHE's Chile1 and Chile2 arrived in La Serena on Friday August 5th 2011. Upon unpacking the DHE's appeared to be in good order after the long trip south. It should be noted that neither DHE arrived with any documentation or mating connectors which will also be needed by a customer.
On Monday August 8th 2011 each DHE cover was opened and a brief internal inspection conducted. All internals were in proper order with the exception of the Mezzanine board on the Chile1 DHE being just slightly tilted on its connectors. Also of note was the fiber optic dust cover missing on the Chile2 DHE. A less consequential observation is the difference in the label placement between the Chile1 and Chile 2 DHE's.

4.) – Shutter and Preflash

Testing of the shutter was accomplished using a small 12V relay part # magnacraft 277XBX-12D as a shutter simulator.

5.) – FPGA boot revisioning documentation

Write description of how the FPGA prom boot revision selection works.

6.) – AFE_digital_OE

Remove U117 pins 1 and 28 and U102 pins 1 and 28 from AFE_digital_OE and tie to GND. Tie U107 to VPIFC supply instead of 3.3V and tie pins 1 and 19 to AFE_digital_OE. See last paragraph on the description of the latch in the first page of the data sheet for a clear explanation of the problem.

7.) – TSM present switch

The TSM present switch is mechanically sensitive on the Chile2 system. It can be accidentally actuated with a push of the end frame when the cover is removed. Suggest a review of the mechanical plunger throw and perhaps a re-adjustment to prevent accidental actuation. This may also present a problem when in a cold environment. This issue needs to be tested in depth to make sure we get it right for all conditions.

8.) – Vfan pinched wire

The +Vfan wire that runs to the blower was shorted to chassis on the Chile2 DHE. A repair was effected using heat shrink. It should be noted that this can charge chassis to the Vfan potential and should be an assembly checkpoint to measure the impedance of both Vfan signals from P11 to chassis after installation of the blower and blower cover.

9.) – Vbb leakage to chassis

The Chile1 DHE exhibits a leakage to chassis through the TSM. The leakage is around -10V when Vbb is set to -65V. The leakage has been verified to be on the utility board as it is not present without a TSM. Tying the chassis to AC ground drains the leakage to zero. The leakage path measures ~ 40Mohm impedance on the utility board or a leakage current of 2uA @80V.

10.) – AFE latch clock series resistors

R63 & R68 changed from 75 to 20 ohms. These are for the clock register strobe and the util register strobe on the AFE. Both these clocks showed to be attenuated when examined causing some intermittent clock edges.

11.) – Timing resolution for delay system clock instruction.

Found that a DSC 1 instruction actually takes two system clocks (76ns). A NOP takes one system clock to execute (37ns).

12.) – AFE1 & AFE2 Vn50 telemetry does not read.

Check resistive voltage divider in AFE design to ensure it is properly scaled.

13.) – TSM connector labeling

The MS connectors and the Shutter / Preflash connectors on the TSM should be labeled.

14.) – Vbb filter on utility board

It should be noted that the Vbb filter on the utility board limits the maximum Vbb output current to 1mA.

15.) – Power supplies instability

The primary power supplies are unstable due to the tuning of the servo control loop in the firmware. This needs to be addressed.

16.) – Chile1 PSM failure

On Tuesday 8/16/2011 the Vhv+ output on the Chile1 system abruptly failed to produce the Vhv+ output potential. The problem was diagnosed to a shorted C29 on the PSM module. Upon removing C29, the short to analog common went away. A check of the C29 component showed that indeed it was shorted. We then decided to continue running without the C29 component installed in the Vhv+ generator circuit.

17.) – Wire list output emailed is incomplete

The wirelist sent via email for the DHE transition module (TSM) wiring is not complete, as it does not contain any information concerning the video channel assignments and wiring.

18.) – Preamplifier Distortion

Chile1 preamplifier for channel 1 shows considerable distortion @2Mhz 600mVpp sine wave input. All other channels on Chile1 preamplifier board are fine.

19.) – Offset voltage in the video chain (unaccounted integrator gain)

The offset voltage seen at the integrator is caused by an unbalanced offset in the invert / non-invert stage just before the integrator. The effect is that the integrator gain is not what one calculates it to be and the offset manifests itself as signal (not cancelled bias) in the pixel data. There are temperature stability concerns because of this fact.

20.) – AFE re-spin should include the ability to reach the higher Vhv power rail, closer to 32V.

HV bias noise testing showed that the HV bias noise increased 10 fold when the HV bias was run at an amplitude close to its upper rail (27.3V). This is probably due to a decrease in the power supply rejection ratio of the HV bias amplifiers as they near saturation. The onset of this effect is in the last .3V below the max output of the amplifier and is not seen at 27V or less (HVbias output voltage).

21.) – Utility Board

There is still an interaction between the temperature telemetry value and heater power. The indicated temperature varies by up to 10 degrees across the heater power range.

22.) – Temperature telemetry channel select

The attribute (htrTempSensorSlct) to select one of two temperature sense channels for heater servo feedback temperature does not function.

23.) – Basic Borg functionality

The ability to disconnect the Borg from the PAN Daemon does not work. The button is available but not enabled. This means that the PAN software cannot be rebooted independently of the Borg.

24.) – Basic Borg functionality

The addition of an exposure time remaining indicator on the Borg Engineering Console might be a valuable addition.

25.) – Basic Borg functionality

The row binning and column binning text boxes of the Borg console do not program the sequencer correctly. Putting a value of 2 in row biining text box sets the values in the rowBin and colBin attributes correctly but the sequencer is put into a 2 x 2 binning mode. The exposure finishes correctly so the data transfer values must be set for the 2 x 2 binning.

In addition, the value of the seqColBin sequencer loop register indicates zero so the sequencer is not actually binning the serials, just producing half a detector worth of data.

Setting a value of row = 1, col = 2 biining factor puts the sequencer back into full frame readout without any binning.

26.) – Basic Borg functionality

If the Image Directory or Image File attributes are changed by a .mod file (after re-initialization, etc.) the engineering console Exposure Parameters text boxes do not reflect the change – This misleads the (poor) operator as to which and where the files are put.

27.) – Basic Borg functionality

After running collector during startup, the Borg connects to the PAN software but does not show a connected status for the PAN or the DHS on the engineering GUI.

28.) – Collector functionality

The sysname_SetVoltages.mod file should not contain the !delay=1000, pwrUpAfeSupplies, !delay1000 statements. The afe is powered up when the DefaultSetup.mod is loaded. In addition, the last statement in this .mod file (afeClkStateReg=0xffffffff) should also be removed.

29.) – Basic Borg functionality

The Borg should load the sysname_SetVoltages.mod file as part of the initialization process.

30.) – Basic Borg functionality

The Borg should load the enable the correct bias and clock banks as part of the initialization process. If this is not considered appropriate, then they should be enabled when either the sequencer is enabled or through a separate button.