MONSOON Image Acquisition Systems

TORRENT

Data Sheet Rev 4.1

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www.ctio.noao.edu/noao/content/monsoon-image-acquisition-system

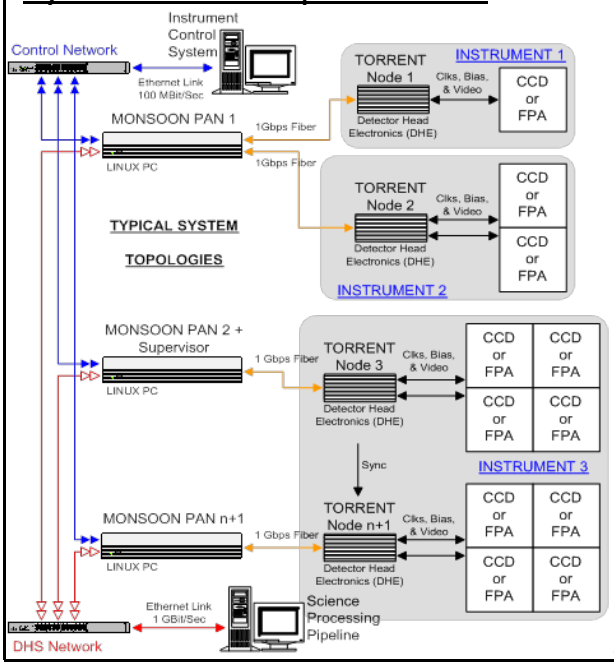
features

- Common architecture for NIR, CCD, and CMOS detector technology
- Clean software interface for command, status and data handling
- Scalable to accommodate single or mosaics of detectors
- Calibrated hardware to assure consistent and known performance
- Open source technology – Constant peer revision and enhancement – All documentation available
- Detector limited performance

applications

- Replacement for aging high maintenance technology
- Small mosaic focal planes
- Replacement of obsolete detector controller technology
- Technical cameras

system components



description

MONSOON is an NOAO "full open-source" development effort that addresses the need for detector-limited image acquisition for current and future generations of astronomical instruments.

Torrent is a second generation implementation of the MONSOON architecture. The Torrent controller has been specifically developed from the proven 'Orange' architecture as a cost effective new or retrofit detector controller. The role as a replacement controller fits existing instrumentation where the original detector controller hardware has become obsolete or difficult to maintain. The Torrent controller provides equivalent or improved performance possibilities with heritage detector technologies through the use of state of the art electronic devices. Improvements to power dissipation, package size, dynamic range, thermal stability, and overall system noise can be expected.

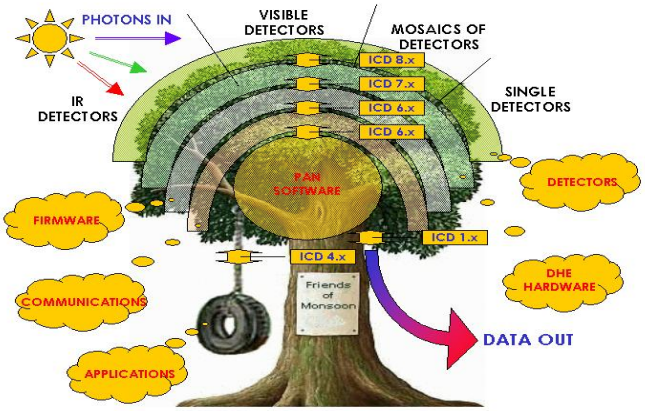
Torrent is completely compatible with existing MONSOON software, PAN computers, and communication link technology. This detector controller is also highly suitable for applications using small mosaics of detectors and for new science or technical cameras that require fast and clean image acquisition from between one to four detector elements.

Efforts have been made in the design to use true generic COTS components to maximize the life cycle and maintainability of the hardware. The design follows the MONSOON edict of using truly technology independent solutions for the system design whenever possible.

In developing Torrent, the original MONSOON architecture for image acquisition systems has been retained. The architecture provides a modular, scalable architecture, which addresses the observatory systems data pipeline and control information flow issues, rather than providing just another proprietary device interface.

system architecture

MONSOON is based upon a stack of functional layers that are separated by concise interface control documents (ICDs). This architectural model allows a high degree of commonality between systems that support the requirements of different detector technologies. The top layer and control layer of the stack is the Pixel Application Node (PAN) computer which runs the MONSOON application on the LINUX operating system.



hardware

The hardware architecture of Torrent is physically manifested in two electronic modules that are supported by the core firmware and software suites. These functionally complimentary modules are mated together to form the detector head electronics (DHE) enclosure that completely supports the detector and instrument specific requirements. The two electronic modules are:

• The Transition Module (TSM) which is designed to permanantly attach to the detector cryostat. The TSM module adapts the detector video and temperature sensing signals from a specific detector application to interface to the generic part of the DHE. The TSM also provides detector protection features and a small memory store to identify the detector system attached to the DHE.

• The Controller (CNTLR) is generic module that physically plugs into the TSM and forms the complete DHE. It is configurable by software to adapt to the requirements of the attached TSM and detector application. The controller module supports the communication to the Pixel Acquisition Node (PAN) computer, Analog circuitry control, power supply control, voltage telemetry, and detector clock sequencing. All calibration values are contained in the DHE modules to allow interchange and common sparing of the controller modules between instruments of the same detector type (NIR, CCD).

firmware

This layer supports the hardware functionality and defines the interface to the software control layer. All hardware functions are mapped to an address space within the DHE. This allows the software to control the DHE through a simple protocol that uses basic read and write commands. Firmware source code is written in VHDL and supplied as part of the open source license. An application specific micro controller is embedded within the CNTLR to deterministically control sequencing of detector control signals. This sequencer efficiently executes code that is downloaded to the DHE at system configuration time. The sequencer has the ability to control all hardware functions within the DHE i.e. clock and bias voltage levels, clock states, acquisition modes and timing, etc. Configuration and calibration is achieved using values stored in the CNTLR and TSM modules.

communications

Interface Control Document group 6 (ICD 6.1) defines the protocol that is used for the Pixel Acquisition Node (PAN) to communicate with the firmware of the DHE. The currently implemented physical layer is a 1 Gbit fiber link module that interfaces to the DHE hardware via the serial FPDP standard protocol. An alternate Gigabit Ethernet based interface using GIGe protocol is available. An RS232 port is available for diagnostics.

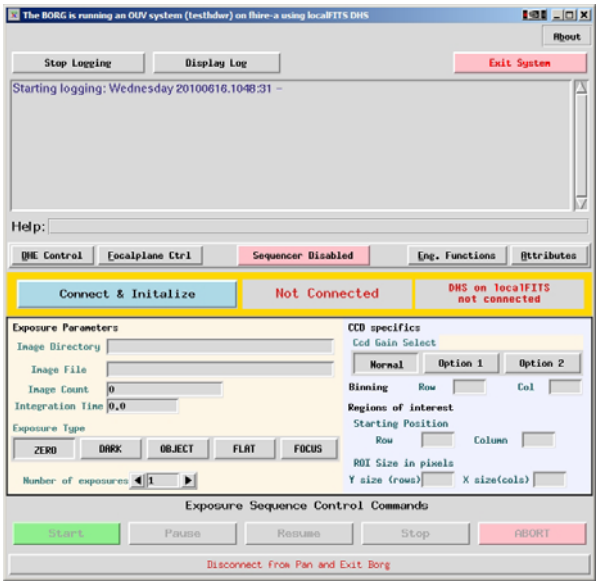
software

All control functions for the system are performed by the PAN software suite. The software layer, called the Generic Pixel Server (GPX) and written in C, handles the system configuration tasks, client communications, pixel data acquisition, post acquisition processing and pixel data transfer transactions. For larger focal planes using more than one DHE node a supervisor task acts as coordinator and command / message distributor. In all cases the client application, usually the Instrument Control System (ICS), sees one coherent focal plane at its disposition. All functions and parameters of the system are assigned to attribute name/value pairs by the software during an initial configuration process. The defined attributes are then manipulated to set and optimize system parameters to support different detectors and/or operational modes. This is done at a high level by commanding an ASCII mode file to be loaded by the system. To customize GPX to suit alternate detector types, it is only necessary to modify one library module that defines the detector specific functions.

toolsets

A small extensible application written in Python is available to provide stand alone control over any MONSOON system. This application, called the Basic Operator Response Gui (BORG), employs the same communication protocol (ICD 4.1) as that used by a normal client (e.g. the Instrument Control System). This provides a solid example during client development. The BORG supports the full capabilities of the MONSOON system and includes provision for scripting and logging. The BORG can be efficiently used to script and control test programs during detector characterization work.

A Configuration Management Toolset is available to manage the complexity of connecting and configuring a DHE to any focal plane. These applications generate the documentation, run time configuration files, and calibration coefficients for MONSOON systems.



specifications

MONSOON / Torrent product information can be found at http://www.noao.edu/ets/monsoon

DHE Enclosure

Size	12.5 x 8 x 6 inches (32 x 20 x 15 cm)
Weight	< 12 lb (5.5 Kg)
Power	external 24 VDC @ < 60 Watts (Nominal CCD system is < 25 Watts)
Detector cabling	Clear access via customer specified connectors on bottom or front of TSM assembly.
Operating conditions	-10 → +40°C 95% humidity non-condensing
DHE → PAN distance	> 300 meters with 1Gbps fiber interface

Control Functions

PAN command execution time	120ns
Sequencer type and memory depth	Application specific MPU in FPGA, 4K code store, 1.5K pattern store
Sequencer clock resolution	25ns
Integration timer resolution and capacity	1ms resolution – 100ns repeatability – 32-bit count up register
Pixel data rate	36 Mpixel/sec - limited by AFE performance
Diagnostic channels	Temperature, serial number, synthetic pixel generator, firmware rev.
Auxiliary functions	Master/Slave DHE sync logic, 2 x temperature monitor + current sources, 1 x temp controller, shutter control and sense

CCD Detector Performance

Video signal inputs	8 single ended AC coupled - P and N channel device compatible
Video signal dynamic range and sensitivity	0. 3v → 3.0v pk/pk, configurable between 1.0µv → 10µv / ADU
Video signal acquisition process	Dual slope CDS with DC restore
Video signal channel acquisition rate	Maximum 500 Kpixel/channel/Sec with 18 Bit conversion
Video signal channel noise and linearity	< 2 ADU rms @ 100Kpix/sec/chan with 2K Ohm source impedance and 2 µVolt / ADU system gain. < 0.01% INL @ 500K Pixel/Sec

CCD Detector Performance (cont)

Pixel data dynamic range	Configurable for 18 Bit or 16 Bit pixel results
Clock signals	32 x Bi-level clocks, four clocks per groups, eight clock groups
Clock signal voltage adjustment range	Adjustable between -17v ⇔ +17v swing relative to gnd.
Clock signal voltage setting resolution	8 mv – Voltage adjustment via software command
Clock signal current source/sink	30ma - Provision for detector protection scheme
Clock signal noise (BW < 20MHz)	< 80µv rms 0 - 20MHz bandwidth
Clock rise / fall time	minimum 110ns tr/tf
Bias signals	32 biases in two groups of sixteen + backside bias potential (VBB)
Bias signal voltage adjustment range	Group 1 configurable for -17v ⇔, +17v Bipolar Group 2 configurable for 0v ⇔ 30.0v or -30.0v ⇔ 0v VBB configurable for 0v ⇔ -65v or 0v ⇔ +65v
Bias signal current source / sink	35 ma for biases. 10ma for VBB
Bias signal voltage setting resolution	< 8mv. Voltage adjustment via software command
Bias signal noise (BW < 20MHz)	< 20µv rms 0 – 20 MHz bandwidth
Diagnostic channels	Power + reference voltages + clocks voltages + biases voltages and currents + board temperature + serial number + firmware rev. etc.

Near-Infrared Detector Performance

Video signal channels	36 single ended or quasi-differential inputs, DC coupled
Video signal dynamic range and sensitivity	0.25v → 2.5v pk/pk, configurable between 4µv → 38µv / ADU
Video signal common mode voltage range	+/- 6v with respect to ground
Video signal channel acquisition rate	1 Mpixel/channel/sec.
Video signal channel noise and linearity	< 1.7 ADU rms, < 0.01% INL @ 800Kpixel/channel/sec.
Digital dynamic range	16-Bit ADC, 32-bit data for digital average and co-add
Digital filtering	1 → 64 digital averages per pixel, 1 → 16 image co-adds
Clock signals	32 x Bi-level clocks + 8 x 256-level fast bias DAC channels
Clock signal voltage adjustment range	Unipolar 0v⇔ 8.0v, -8.5v ⇔ 0v or Bipolar +/- 8.0v
Clock signal voltage setting resolution	2/4 mv – Voltage adjustment via software command
Clock signal current source/sink	30ma - Provision for detector protection scheme
Clock signal noise (BW < 20MHz)	< 80µv rms 0 – 20MHz bandwidth
Clock rise / fall time	Configurable, minimum 30ns
Bias signals	24 individually adjustable voltage + 36 x Video chan. current sinks
Bias signal voltage adjustment range	Unipolar 0v⇔ 8.0v, -8.0v ⇔ 0v or Bipolar +/- 8.0v
Bias signal current source / sink	30 ma - Provision for detector protection scheme
Bias signal voltage setting resolution	< 4mv. Voltage adjustment via software command
Bias signal noise (BW < 20MHz)	< 20µv rms 0 – 20MHz bandwidth
Diagnostic channels	Power + reference voltages + clocks voltages + biases voltages and currents + board temperature + serial number + firmware rev. etc.